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FPGA Based Multiobject Feature Extraction For Object Recognition

M.Monica dhana ranjini[#1], P.Gnana skanda parthipan[#2],G . Prabhakar[#3]

[1]M.E Embedded system, Syed Ammal Engineering college, Ramanathapuram, Tamil Nadu, India

[2]Department of EEE, Syed Ammal Engineering college, Ramanathapuram, Tamil Nadu, India

[3]Department of EEE, Syed Ammal Engineering college, Ramanathapuram, Tamil Nadu, India

ABSTRACT— In the arrival of today's highly integrated multimedia device and fast emerging applications, image processing have become more important than any others. These devices require complex image processing tasks lead to a very challenge design process as it demands more efficient and high processing systems. The scope of the project is to extract locations and features of multi objects in an image for object recognition. For low power consumption and better performance we design a proposed system in FPGA. In existing system an cell based multi object feature extraction algorithm is used to extract simultaneously autocorrelation feature of objects. It is calculated using zeroth order and first order moments to obtain the size and location of multiple objects. To reduce computational complexity and memory consumption, Local Binary Pattern (LBP) and Local Ternary Pattern (LTP) is used to extract the feature of multiple objects are proposed. In the local binary pattern, the LBP value is computed by comparing a gray level value of centre pixel in an image with its neighbors. The local ternary pattern is extended from LBP to three-valued code in which gray values are quantized to zero,+1,-1. The proposed architecture is designed using verilog HDL, simulated using Modelsim software and synthesized using Xilinx project navigator.

KEYWORDS—object recognition,local binary patterns,local tetra patterns,error detection and data recovery,similarity measurements.

I. INTRODUCTION

The problem of extracting the features of single object in images is used in applications such as object recognition. The methods used for these tasks are not applicable for extracting the feature from multiobject in an image. A recent development in image segmentation for multiobject extraction leads to several approaches. The Rosenfeld algorithm [1] was developed to extract and label connected components in a binary image. It takes two or more times to scan an entire image. Unsupervised video segmentation based watershed transformation [2] is used to detect and segment newly appearing objects by increasing computational efficiency. In medical image segmentation it is limited due to over segmentation and sensitivity to noise. By using Improved k-means clustering algorithm [3] an image is partitioned into k-clusters. It has problems when clusters are of different sizes, densities and non globular shapes. A watershed cut [4] localizes with better accuracy the contour of objects in digital images. It is proved through their optimality in terms of minimum spanning forests. This method is difficult to predict or analyze and also at minimization stage imperfection occurs. Graph cuts [5] are used to find interactively the globally optimal segmentation of N-dimensional image. It suffers from problem of efficiency, in which interactive extraction of a foreground object in complex environment whose background cannot be trivially subtracted. Grab cut method [6] combines hard segmentation by iterative graph-cut optimization with border matting to deal with mixed pixels on object boundaries. It has several iterations because the parameters of the regional bias can be iteratively re-estimated. Graph cut and efficient N-D image segmentation [7] use graph cuts based approaches to extract object are used with earlier segmentation methods whose energies optimized by graph cuts combine boundary regularization with region-based properties. It may leads to multi-way cut problems. In the spatiotemporal segmentation [8] a number of consequent frames of the image sequence are analyzed simultaneously in order to segment the images into regions. This higher order segmentation implicitly solves the problem of correspondence of objects between consequent frames. Following region separation, and depending on the application, knowledge-based methods may be used to decide whether a separated region corresponds to a specific semantic object. It is slower due to complexity of statical formulas. In remote sensing

image segmentation [9] incorporating some prior information, a novel single point iterative weighted fuzzy C-means algorithm is proposed for multidimensional data clustering and image classification but it has difficulties with hard clusters. Conventional multiobject extraction methods are not suitable for FPGA based system because of their over segmentation, empty clusters and iterative process that are applied to all pixels in an image.

In this paper, we focused on multiobject feature extraction based on texture descriptors and we propose a Local Binary Pattern (LBP) and Local Ternary Pattern (LTP) to extract the feature of multiple objects. These methods will reduce computational complexity and memory consumption. A proposed architecture is used as hardware implementation in FPGA. In the local binary pattern, the LBP value is computed by comparing a gray level value of centre pixel in an image with its neighbors. The local ternary pattern is extended from LBP to three-valued code in which gray values are quantized to zero, +1,-1.

II. RELATED WORK

Many connected component labeling algorithm such as the rosenfeld algorithm [1], number of times to scan an entire image for extracting a label map of connected components in a image is high. Several multiscan labeling algorithms have been proposed to reduce number of scanned pixels for labeling. In bidirectional scanning [10], will require high memory consumption. Two scan labeling [11] has disadvantage in accelerating labeling process. One-scan labeling algorithm [12] will track the contours in binary image which are not suitable for hardware implementation because of their irregular image memory access in tracking the contour of connected components.

In recent years, FPGA is implemented in connected component labeling algorithms to accelerate multiobject feature extraction due to high performance and flexibility to tackle most tasks through parallelism. However, most of these FPGA-based implementations cannot extract all the connected components when there are thousands of complex-shaped objects in a binary image. Thus, high memory consumption in connected components labeling often makes difficulties in accelerating multiobject extraction by implementing a connected components labeling algorithm on hardware. To reduce such computational complexities and memory consumption in connected components labeling, a cell based labeling algorithm [13] to extract the zeroth and first order moments of multiple objects in a binary image; this can reduce the number of scanned pixels for labeling and memory size to store label equivalences without accuracy degradation in space resolution by dividing an image into sub image regions of a certain size as cells. These moments are not always sufficient for shape-based blob analysis to identify multiple complex-shaped objects in a binary image. Thus the cell-based labeling algorithm is expanded as a cell-based multi object feature extraction algorithm [14] that can obtain higher-dimensional shift-invariant features of labeled objects in an image as well as their zeroth and first-order moments.

III. METHODOLOGY

A. Local binary pattern(LBP)

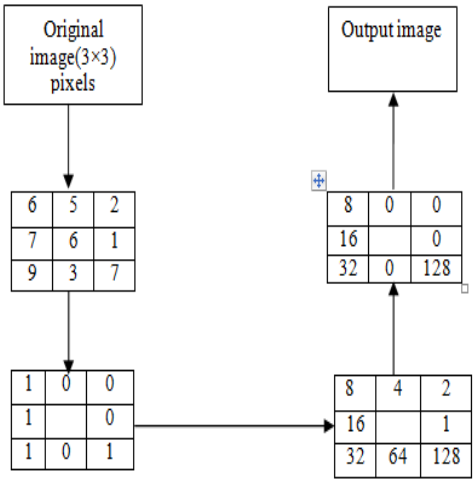
Local binary pattern is used in object recognition because it shows excellent result in terms of discriminative power and computational complexity. Local binary pattern texture analysis operator is a gray scale invariant texture measurement derived from a general definition of texture in a local neighborhood. In LBP method, an original 3x3 neighborhoods are threshold by value of centre pixel and results are considered in binary number. The corresponding decimal value of generated binary number is the LBP number as show in fig.1 the Computation of LBP is given in equation (1) and (2)

$$LBP_{P,R} = \sum_{P=1}^{P} 2^{(P-1)} \times f_1\,(g_p - g_c) \quad (1)$$

$$f_1\,(x) = \begin{cases} 1, x \geq 0 \\ 0, else \end{cases} \quad (2)$$

where

g_c is gray level of centre pixel
g_p is gray level of neighbors
P is number of neighbors
R is radius of the neighborhood



Binary no: 10111000
Decimal value: 184

Fig.1. Example of local binary pattern operator

B. Local Ternary Pattern(LTP)

The extension of local binary pattern is local ternary patterns(LTP) which is three-valued texture operator. In this method instead of thresholding the centre pixel of neighborhood a threshold say t is defined and any gray value in the zone of width ±t around g_c are quantized to zero, those values above (g_c+t) are quantized +1 and those below (g_c- t) are quantized to -1 where t is a user specified threshold. The computation of LTP is given in equation (3)

$$f_1(x, g_c, t) = \begin{cases} +1, & x \geq g_c + t \\ 0, & |x - g_c| < t \\ -1, & x \leq g_c - t \end{cases} \quad (3)$$

Where x = g_p

In the LTP, the obtained ternary pattern is further coded into right and left binary patterns. The right pattern is coded by replacing -1 with 1 and 0 for 1 and 0. The left pattern is obtained by retaining 1 and replacing 0 for 1 and 0.the calculation of LTP operator is shown in fig 2.

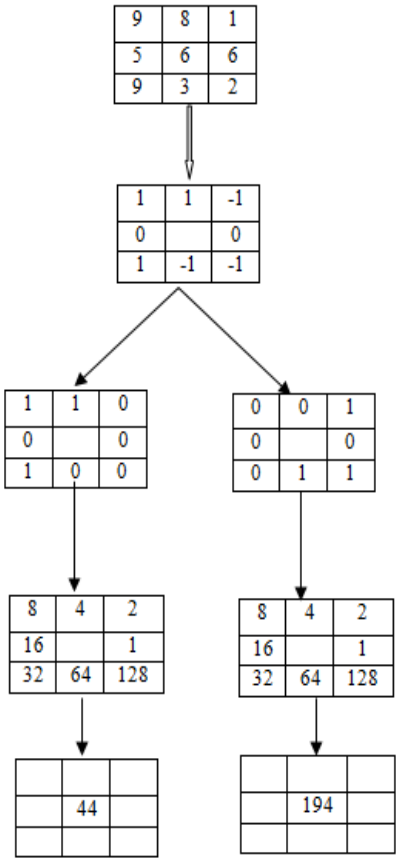


Fig.2. Calculation of LTP operator

IV. PROPOSED SYSTEM MODEL

The complete architecture of proposed system is shown in fig.3

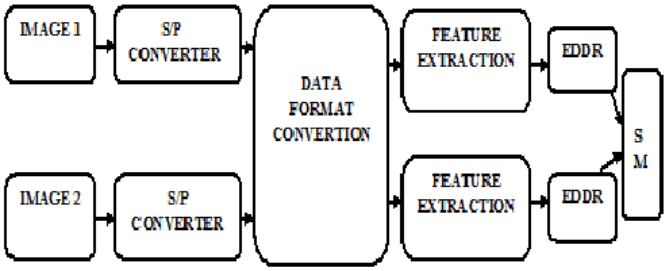


Fig.3.Block diagram of proposed system

The proposed system consist of two serial image data from two camera heads of gray scale image. these are converted into 48-bit parallel data(8 bits/pixel) with six pixels per block by using serial to parallel converter. These conversions are executed for the two images from two camera head in parallel. The data format converter is used to convert 48-bit parallel data for six pixels into 40-bit parallel data for four pixels to synchronize with timing for rows and columns of an image. The conversion are executed in parallel for two images and 96-bit parallel data are converted into 80-bit parallel data for eight pixels. These 80-bit data are computed using local binary and ternary pattern texture operators to extract the features of the image. The feature extracted are processed in Error Detection Data recovery (EDDR) circuit and compared to the features of query image using similarity measurements (SM).

V. EXPERIMENTAL RESULTS

The proposed architecture is implemented with Verilog HDL and simulated using modelsim XE 5.5e for functional verification. It is synthesized using Xilinx ISE 9.2i and their device utilization summary are analysed.

A. Simulated output

The original gray scale image is subdivide into several 3x3 sub image, each subimage has gray values which are thresholded by center pixel to get binary number. The results are obtained by converting binary number into LBP and LTP codes using texture operators. The simulation output of LBP operator is show in fig.4 and the simulation output of LTP operator is show in fig.5. These are applied to EDDR to get final simulation result as show in fig.6

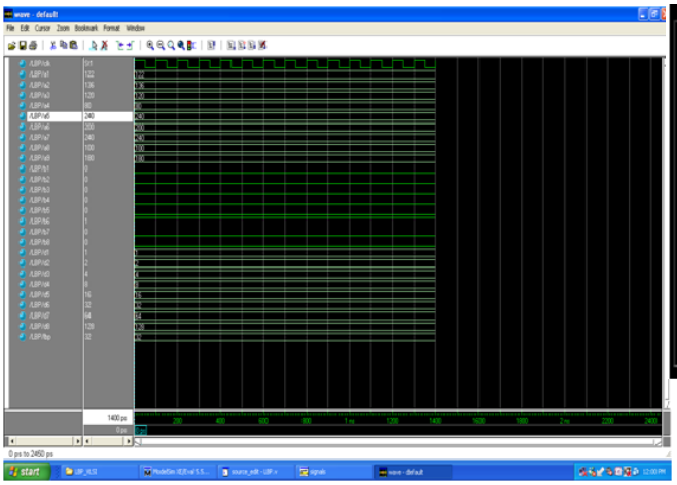


Fig.4 simulation result of LBP operator

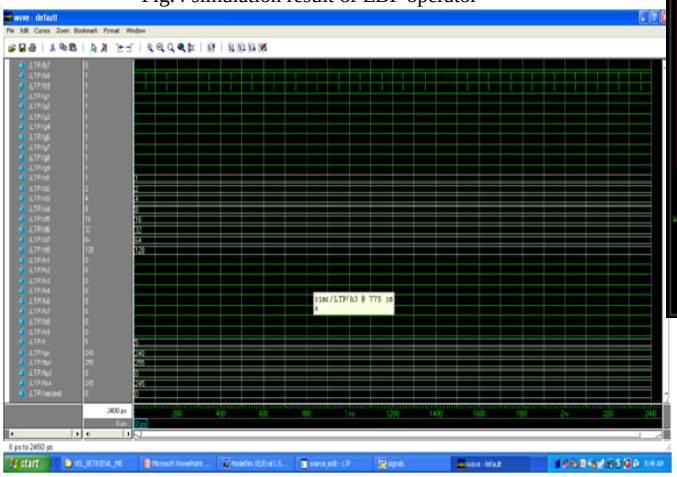


Fig.5 simulation result of LTP operator

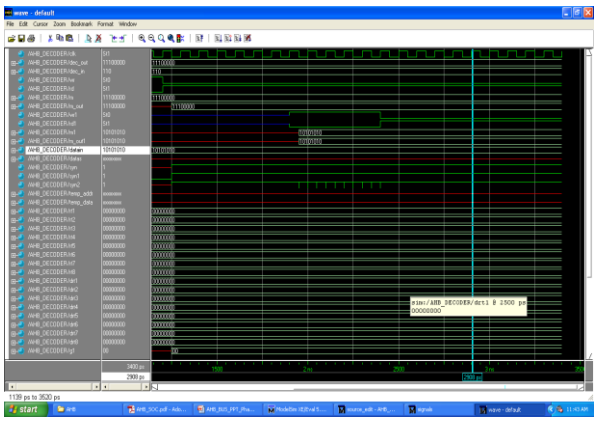


fig.6 Simulation result of proposed architecture

B. *Schematic of proposed architecture*

The RTL (register transfer level) hardware circuit for implementing the proposed architecture are shown in fig 7 and the technology schematic view for proposed architecture is shown in fig 8.

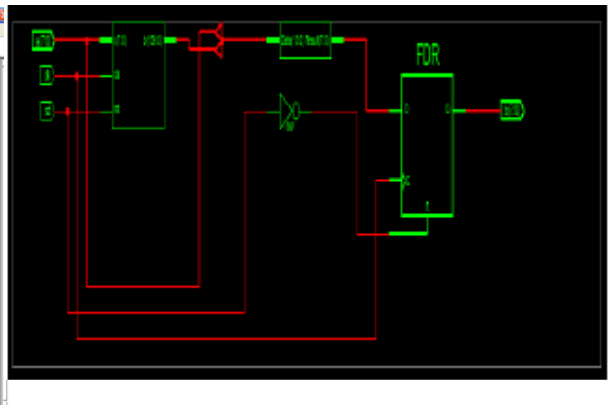


fig.7 RTL view of proposed architecture

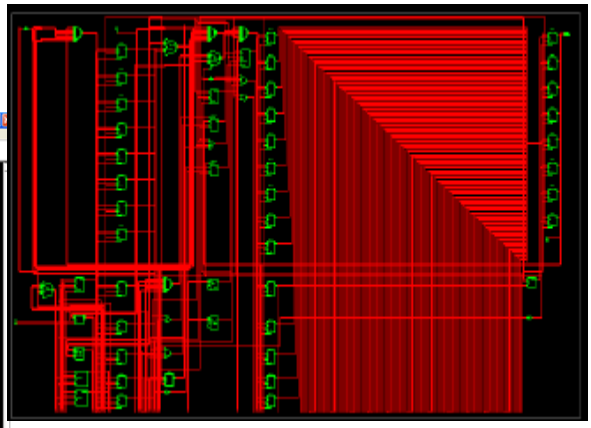


Fig.8 Technology schematic of proposed architecture

C. *Device utilization summary*

The device utilization summary on Xilinx XC3S1600E-FG320 FPGA platform is given in table I. As by power report the power consumption using the hardware implementation of proposed architecture in FPGA is measured as 203 mill watts.

TABLE I. DEVICE UTILIZATION SUMMARY

RESOURCE	USED	AVAILABLE	PERCENTAGE(%)
No of slices	682	9312	7
No of 4 input LUTs	1987	21	9312
No of bounded IOBs	18	232	21
No of GCLKs	1	24	4

VI. CONCLUSION

Thus the methodologies for computation of LBP and LTP operator for extracting the features of images are

described and simulation outputs are viewed using modelsim. The proposed architecture is implemented using Verilog HDL and simulation output is viewed using modelsim. The computational simplicity of the proposed architecture is seen using device utilization summary. The power report shows the power consumption used by the architecture is 203 mill watts, which proves the image processing algorithm are suitable to work in low power FPGA. Thus we plan to extend the proposed architecture using multiobject tracking and object recognition to various embedded applications such as motion capture and blob analysis in factory automation.

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