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Performance Analysis of VLSI Based Multilevel Inverter

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Abstract—This paper compares two different topologies of three phase inverter (i.e. diode clamped followed by cascade H-bridge) which includes five level and seven level inverters. The selection of topology and control techniques may vary according to power demands of inverter. The comparison is done with respect to THD & number of components. The switching pattern for inverter is explained well. For each inverter IGBT's are used as switching devices to make the comparison more accurate. The FFT spectrums for the outputs are presented to study the reduction in the harmonics. This paper deals with selection of multilevel inverter as a trade of between number of components, complexity & THD. The circuit is simulated using MATLAB/SIMULINK.

Keywords— Multilevel inverter, neutral clamped, cascaded H-bridge, THD, VSI

I. INTRODUCTION

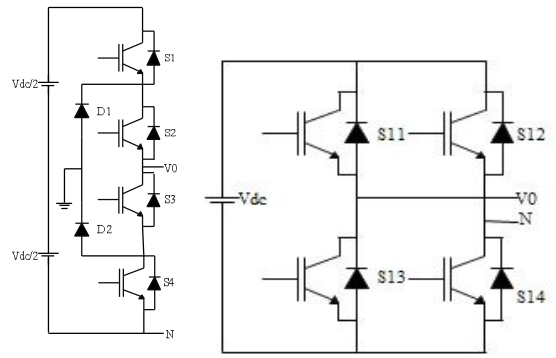


Fig. 1. Multilevel inverter topologies: (a) three-level DC-MLI, (c) three-level CHB-MLI.

The preliminary studies on multilevel inverters (MLI) have been performed using three-level inverters. In recent years, multilevel inverters have gained much attention due to their various advantages such as lower common mode voltage, lower voltage stress on power switches, lower dv/dt ratio to supply lower harmonic contents in output voltage and current. Comparing two inverter topologies at the same power ratings, MLIs also have the advantages that the harmonic components of line-to-line voltages fed to load are reduced owing to its switching frequencies. The most common MLI topologies classified into three types are neutral/diode clamped MLI (DC-MLI), flying capacitor MLI (FC-MLI),and cascaded H-Bridge MLI (CHB-MLI). The two of them are shown in Fig. 1.and compared.

II. INVERTER TOPOLOGIES

Two major multilevel inverter structures applied to industrial applications listed as diode clamped, and the cascaded H-bridge inverter with separate DC sources. In addition to this, many hybrid multilevel inverters have been developed by using these basic types mentioned above. Among the three types of multilevel inverters, the cascade inverter has the least components for a given number of levels. Cascade multilevel inverters consists of a series of H-bridge cells to synthesize a desired voltage from several separate DC sources. All these properties of cascade inverters allow using various pulse width modulation (PWM) strategies to control the inverter accurately.

A. Neutral/Diode clamped multilevel inverter

The neutral clamped inverter, also known as diode clamped inverter. The basic architecture of this inverter discussed in references [5], [6]. The neutral clamped inverter delivers the staircase output voltage using several levels of DC voltages developed by DC capacitors.

If n is the number of level, then the number of capacitors required on the DC bus are (n-1), the number of power electronic switches per phase are 2(n-1) and the number of diodes per phase are 2(n-2). This design formula is most common for all the neutral clamped multilevel inverters.

The DC bus voltage is split into five levels using four capacitors C_1, C_2, C_3 and C_4, for seven level using six capacitors C_1, C_2, C_3, C_4, C_5, and C_6. The voltage across each capacitor is $V_{dc}/4$ and $V_{dc}/6$ for five level and seven level MLI and the voltage stress across each switch is limited to one capacitor voltage through clamping diodes. The switching sequences of three phase 7-level neutral clamped multilevel inverter are shown in table.1.

As the number of levels increase the harmonic distortion decreases and efficiency of the inverter increases because of the reduced switching losses. The number of levels in multilevel inverters is limited because of the large number of clamping diodes required. The reverse recovery of these diodes is especially with multicarrier PWM techniques in a high voltage application is a major design challenge.

B. Cascaded H-Bridge multilevel inverter

An alternative multilevel inverter topology with less power devices requirement compared to previously mentioned topologies is known as cascaded H-bridge multilevel inverter (CHB-MLI) and the topology is based on the series connectionof H-bridges with separate DC sources.

Since the output terminals of the H-bridges are connected in series, the DC sources must be isolated from each other. The resulting AC output voltage is synthesized by the addition of the voltages generated by different H-bridge cells. Each single phase H-bridge generates three voltage levels as $+V_{dc}$, 0 & $-V_{dc}$ by connecting the DC source to the AC output by different combinations of four switches S_{a1}, S_{a2}, S_{a1}^1 and S_{a2}^1 as seen in first cell of fig. 1. For the seven level CHB-MLI, three separate DC sources per phase and generates an output voltage with seven levels. To obtain $+V_{dc}$, S_{a1} and S_{a2}^1 switches are turned on, whereas $-V_{dc}$ level can be obtained by turning on the S_{a2} and S_{a1}^1. The output voltage will be 0 by turning S_{a1} and S_{a2} switches or S_{a1}^1 and S_{a2} switches. If m is assumed as the number of modules connected in series, then the number of output levels n in each phase is given by equation (1). The switching states of a CHB-MLI can be determined by using equation (2)

$$n = 2m+1 \tag{1}$$

$$sw = 3^n \tag{2}$$

The first leg phase voltage (V_{an}) is constituted by multiplying V_{a1} and V_{a2} values of series connected H-bridge cells and will generate a stepped waveform. The fourier series expansion of the general multilevel stepped output voltage is shown in equation (3) and transform is applied in equation (4), where H is the harmonic number of the output voltage of inverter. The switching angles that are indicated as α1….α5, in equation (3) can be chosen to obtain minimum voltage harmonics and several fundamental frequency switching techniques have been evaluated such as selective harmonic elimination PWM or active harmonic elimination PWM.

$$(\omega t) = \frac{4Vdc}{\pi}\sum_{H=1,3,5,\dots}^{\infty}\left(\cos(H\alpha_1) + \cos(H\alpha_2) + \cdots + \cos(H\alpha_5)_{,}\right)\sin\frac{(H\omega t)}{H} \tag{3}$$

$$V(\omega t) = \frac{4Vdc}{\pi}\sum_{H=1,3,5,\dots}^{\infty}\left(\cos(H\alpha_1) + \cos(H\alpha_2)_{,}\right)\sin\frac{(H\omega t)}{H} \tag{4}$$

The modulation index is defined as M.I. can be calculated as in equation (5)

$$M.I. = \frac{(\pi V_1)}{4V_{dc}} \tag{5}$$

Since, the values of Eq. (4) are non-linear, the calculations are obtained by using Newton–Raphson Iteration.

III. CARRIER BASED DISPOSITION PWM METHOD

Carrier based disposition PWM methods were first proposed by Carrara et al[2]. For an *n*-level inverter, *n*-1 carriers with the same frequency $f_c$and the same amplitude $A_c$are disposed such that the bands they occupy are contiguous. The reference waveform has maximum amplitude A_m, a frequency f_m, and its zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the IGBT corresponding to that carrier is switched on and if the reference is less than a carrier signal, then the IGBT corresponding to that carrier is switched off [3].

Previous works on PWM techniques shows that disposition technique for diode clamped and PSCPWM for cascaded inverter five rises to same harmonic profile for the same number of total switch transition. Hence these techniques can be efficiently applied for Diode Clamped and Cascaded Multilevel Inverter.

Carrier Disposition method arrange N-1 carrier waveform of same amplitude and frequency in continuous bands to fully occupy the linear modulation range of the inverter. The reference or modulating wave is positioned at the center of the carrier set, and continuously compared with the carriers to obtain the necessary gating pulses [3].

In multilevel inverters, the amplitude modulation index (M.I.) is the ratio of reference amplitude (R_a) to carrier amplitude (C_a).

$M.I. = R_a / (m-1)C_a$ (4)

The frequency ratio (R_f) is ratio of carrier frequency (f_c) to reference frequency (f_r).

$R_f = F_c/F_r$. (5)

IV. Simulation Results

The SPWM for the three-phase five level & seven level CHB-MLI &Neutral clamped MLI is implemented on a MATLAB SIMULINK model. The simulated results for five & seven level are compared for different modulation indexes with the input voltage 600V.

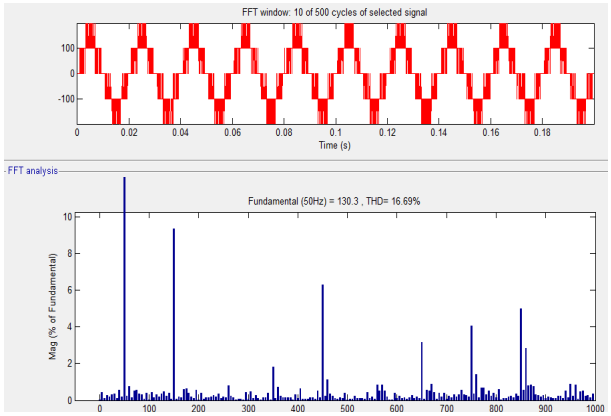


Fig. 2.Five level CHB-MLI Line to Ground voltage without filter

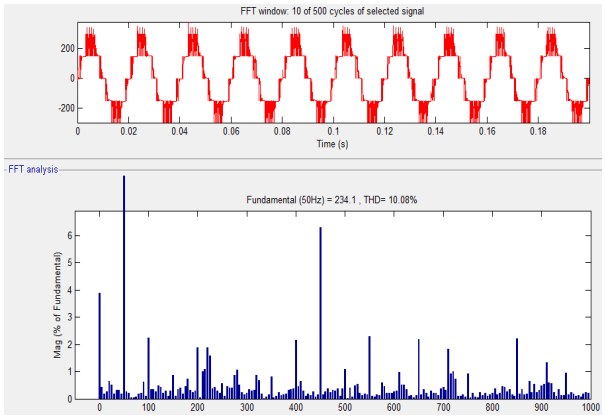


Fig. 3. Five level neutral clamped MLI Line to Ground voltage without filter

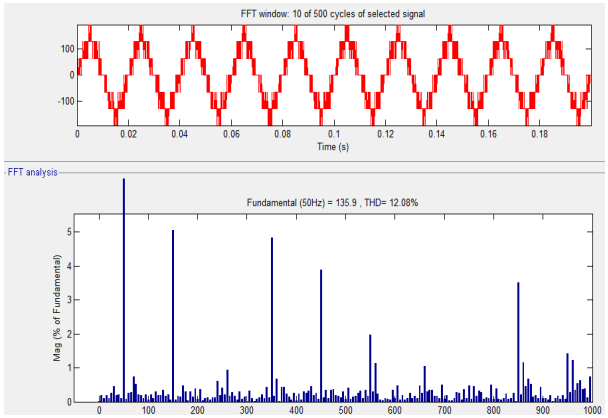


Fig. 4.Seven level CHB-MLI Line to Ground voltage without filter

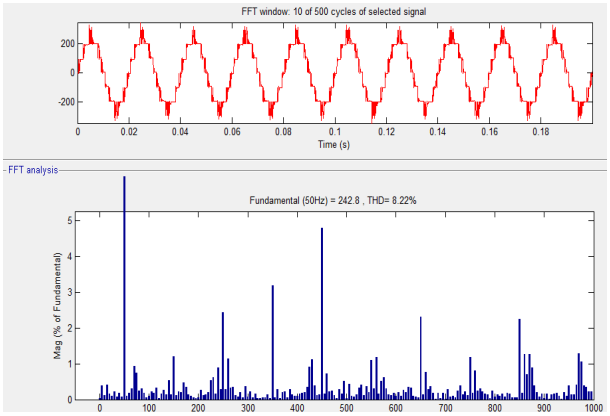


Fig. 5. Seven level neutral clamped MLI Line to Ground voltage without filter

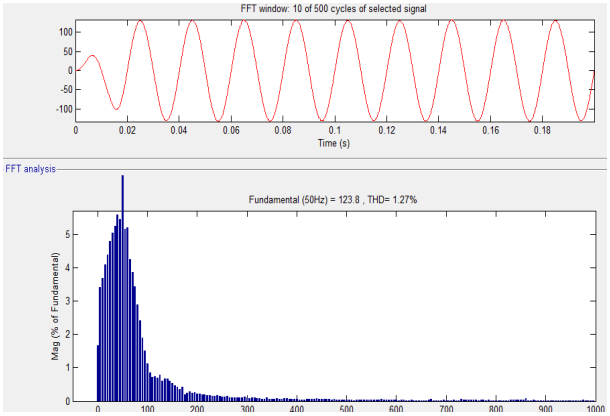


Fig. 6.Five level CHB-MLI Line to Ground voltage with filter

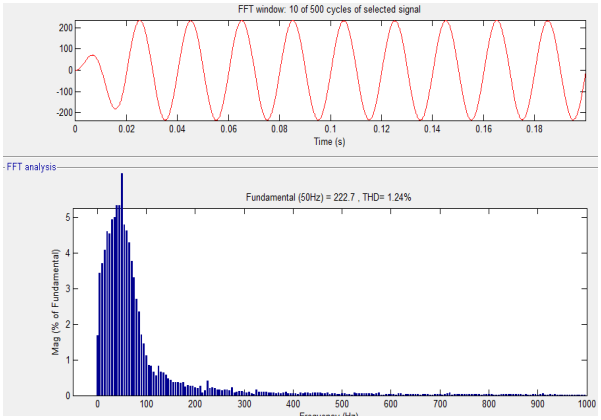


Fig. 7. Five level neutral clamped MLI Line to Ground voltage with filter

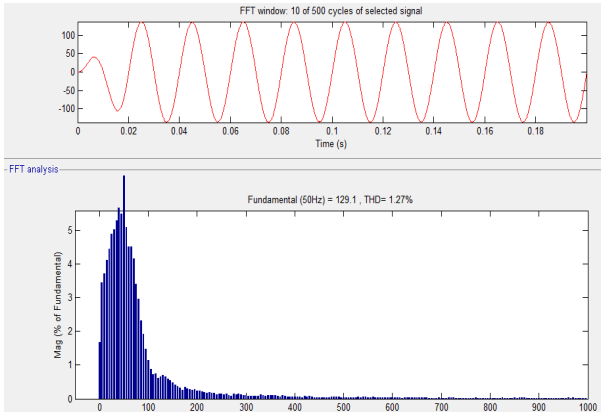


Fig. 8.Seven level CHB-MLI Line to Ground voltage with filter

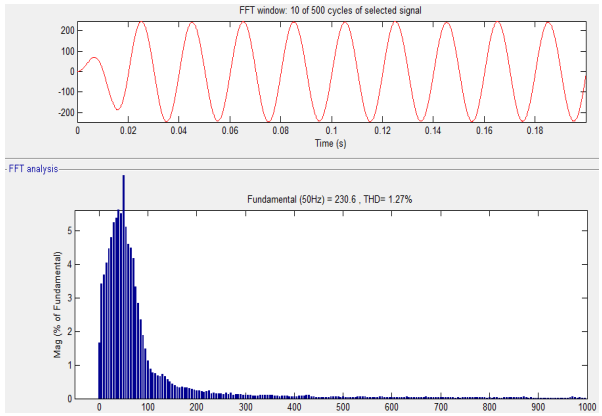


Fig. 9. Seven level neutral clamped MLI Line to Ground voltage with filter

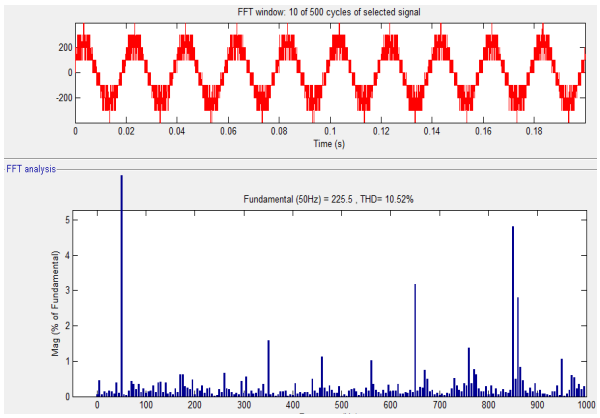


Fig. 10.Five level CHB-MLI Line to Line voltage without filter

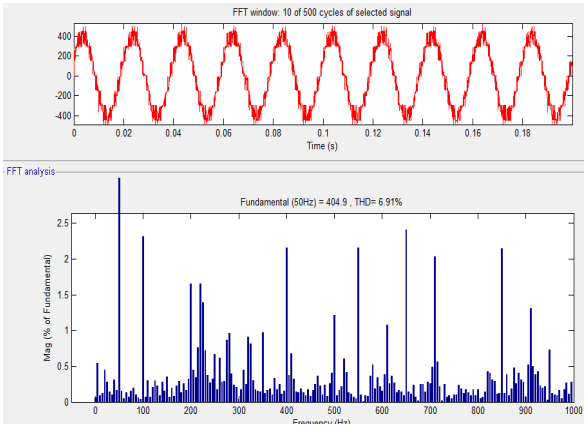


Fig. 11. Five level neutral clamped MLI Line to Line voltage without filter

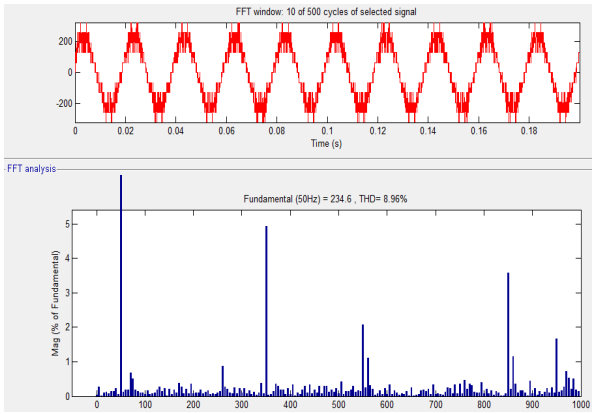


Fig. 12.Seven level CHB-MLI Line to Line voltage without filter

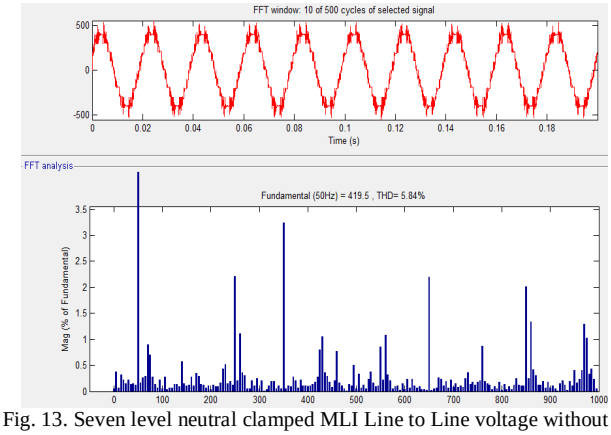


Fig. 13. Seven level neutral clamped MLI Line to Line voltage without filter

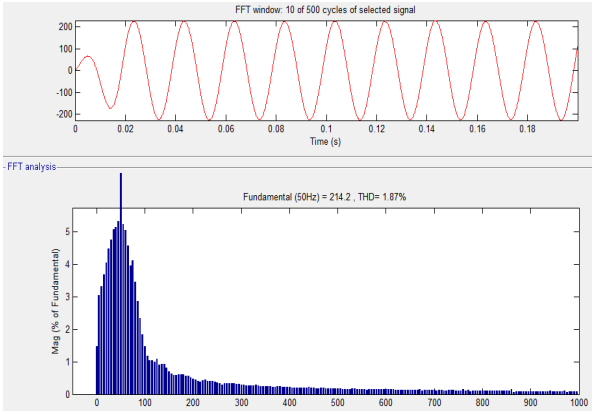


Fig. 14.Five level CHB-MLI Line to Line voltage with filter

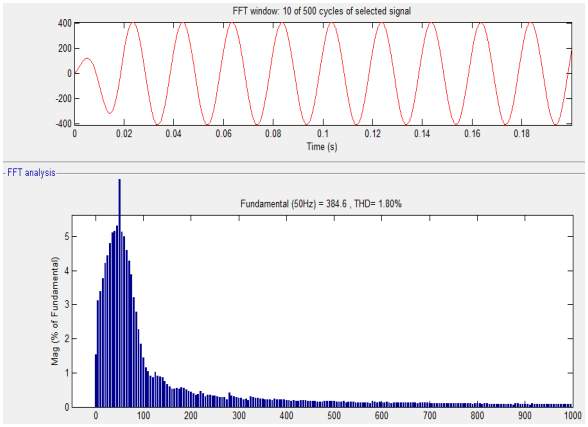
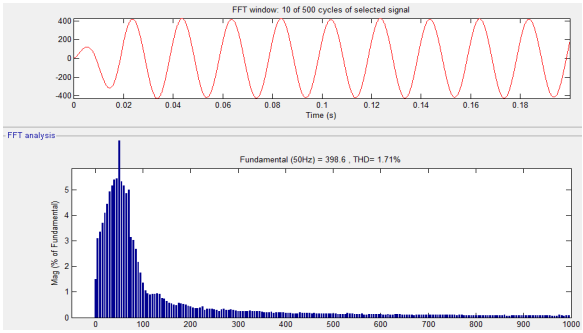


Fig. 15. Five level neutral clamped MLI Line to Line voltage with filter.



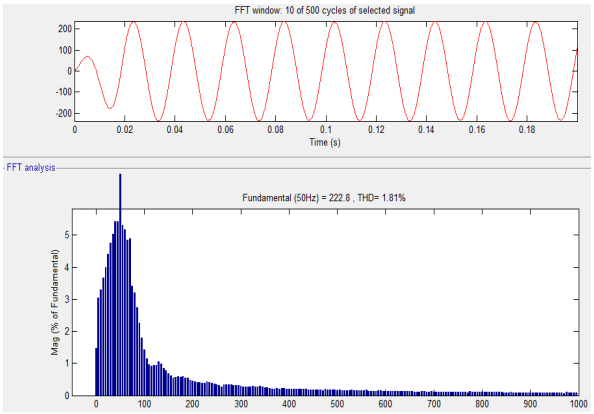


Fig. 16.Seven level CHB-MLI Line to Line voltage with filter

Fig. 17. Seven level neutral clamped MLI Line to Line voltage with filter

Table 1: Output voltages & %THD for different modulation index

Neutral Clamped	5 level				7 level				CHB MLI	5 level				7 level			
M.I.	0.6	0.7	0.8	0.9	0.6	0.7	0.8	0.9	M.I.	0.6	0.7	0.8	0.9	0.6	0.7	0.8	0.9
V_o without filter	166	207	234	280	188	208	242	268	V_o without filter	82.3	108	130	144	95.1	116	135	156
THD (%)	15.3	14	10	9.7	8.5	7.6	8.2	6.2	THD (%)	18.0	22.6	12.1	14.54	14.5	10.9	12.1	9.39
V_o with filter	158	197	223	266	179	198	230	268	V_o with filter	78.2	102	123	137	90.32	111	129	148
THD (%)	1.2	1.3	1.2	1.3	1.3	1.2	8.3	1.3	THD (%)	1.25	1.28	1.27	1.26	1.26	1.25	1.27	1.24

VI. CONCLUSION

The neutral clamped and cascaded 3-phase 5 & 7 has been designed and simulated in *MATLAB / Simulink* environment With SPWM for different modulation index & results are tabulated in this paper. From the result as shown in the table we can conclude that as we increase the modulation index THD reduces and voltage performance reduces for both 5 level and 7 level inverter

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