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# A High Step-Up DC-DC Converter Using Coupled Inductor With Fuzzy Logic Control

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ABSTRACT—In this paper, a high step-up converter using coupled inductor with Fuzzy Logic Control is analyzed and simulated. The converter uses a coupled inductor and a switched capacitor circuit to achieve high voltage conversion ratio. Two capacitors and diodes constitute the switched capacitor circuit. The two capacitors are charged in parallel during the switch-off period and are discharged in series during the switch-on period by the energy stored in the coupled inductor to achieve a high step-up voltage gain. Switch voltage stress and the circulating current are reduced by a clamp circuit which is composed of a diode followed by a capacitor. Thus the efficiency of the converter is improved. The operating principle and the steady state analysis are discussed in detail. A Fuzzy logic controller is designed such that it eliminates the Voltage Drift problem.

**INDEX TERMS**—Coupled Inductor, FLC, Switched Capacitor circuit.

## I. INTRODUCTION

Renewable energy sources (RES) have experienced a fast development in recent years. These systems employ with micro sources like PV, fuel cells etc. Though PV cells can be made into array and connected in series to produce high voltage there exist serious problems like shadowing effects, short circuit which drastically reduces its efficiency. In order to overcome such adverse effects this micro source energy is utilized by the high step up converter to produce high voltage and satisfy the demands. Conventional boost converters can't provide such a high DC voltage gain for extreme duty cycle.

Thus high step up dc-dc converters are used as front comp Copyright to IJIRSET www.ijirset.com

end converters to step from low voltage to high voltage which are required to have a large conversion ratio, high efficiency and small volume [1].In some converters active clamp circuit is used to overcome voltage spikes caused by the leakage inductance of the coupled inductor. Though ZVS technique is employed for soft switching it can't sustain light loads [2]. Different switching structures are formed either two capacitor or two inductor with twothree diodes. Both the step up and step down operations can be performed in this topology, Performance of hybrid converters are better than classical converters but still its costlier to implement [3]. Low level voltage from the PV, fuel cells is connected to Kilo watt level using step up dcdc converter and inverter circuits. Voltage spikes and switching losses are eliminated by active clamping. In dc-ac, inverter always tends to draw ac ripple current at twice the output frequency. Resonant inductors cost and circuit volume is high [4]. In some converters high voltage conversion is obtained by changing transformer turns ratio which will increase the overall efficiency but still the operation of main switch involves hard switching and also EMI noise gets raised [5]. Impacts of SiC (silicon carbide) MOSFETS on converter, switching and conduction losses are reduced even though fast switching is done. Si diodes have ideal, but sill SiC devices processes large amount of ringing current at turn OFF relatively to other devices. Package of external diode and the diode itself have more parasitic capacitances that are added to the devices parasitic aggravating the ringing [6]. Here, the voltage step is done without a transformer and a high voltage gain s achieved without an extremely high duty ratio but still the circuit becomes more bulky as more number of passive components are used [7]. Though this converter provides

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a non-pulsating current by using an auto transformer, duty ratio is limited by 0.5 and not suitable for non-linear loads [8].Here voltage stress of the active switch is reduced thereby the conversion efficiency is improved. This converter requires a multi winding transformer which makes the circuit design complex [9]. This converter avoids extremely narrow turn off period, ripples and switching losses are eliminated by ZVS technique. It uses two coupled inductors which makes the circuit complex [10]. In this converter no additional magnetic components used, switching losses are minimized by adopting a regenerative snubber circuit. As the circuit uses more switches controlling is complex [11]. In this converter high voltage gain is obtained but the circuit has more passive components [12]. It employees single ended scheme cost is reduced. Galvanic isolation is needed, but suitable only for low power and frequency applications [13], [14]. In this converter no need of extreme duty ratio but if conduction losses or switching losses occurs the efficiency is reduced [15]. It is possible to generate the non-isolated dc-dc converters but the major drawback is that switching frequency must be maintained constant and the turn ratio of the auto transformer must be unity [16]. Some converters operate at very high frequency with fast transient response. The main switch is fabricated from an integrated power process, the layouts can be changed to vary the parasitic, however design of switch layout is complex, fixed frequency and constant duty ratio must be maintained [17]. This converter provides high voltage gain and can be employed for high power applications however the duty ratio is limited to 0.85 [18], [19]. In this, the energy of the leakage inductor is recycled to the output load directly, limiting the voltage spike on the main switch. To achieve a high step-up gain, it has been proposed that the secondary side of the coupled inductor can be used as flyback and forward converters [20], [21].In some converters voltage gain is improved through output voltage stacking [22].

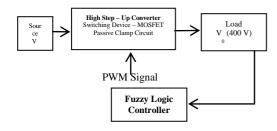


Fig. 1 Block Diagram.

The main objective is to improve the Voltage Gain of the Step-up Converter and also to reduce Voltage stress of the circuit. Further the Voltage Drift problem is reduced using closed loop control of the proposed converter with fuzzy logic controller. From Fig.1, The output voltage from the converter is fed as feed back to the FLC; there it compares the feedback voltage signal and the reference voltage signal to produce PWM pulse which triggers the main switch of the converter.

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#### II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

Fig. 2 shows the circuit configuration of the proposed converter, which consists of a boost converter, coupled inductor, switched capacitor circuit and a clamp circuit. The equivalent circuit of the coupled inductor has a magnetizing inductor  $L_m$ , leakage inductor  $L_k$ , and an ideal transformer.  $N_s$  and  $N_p$  is the primary and secondary winding of theideal transformer,  $V_{in}$  DC input voltage,  $V_0$  is the DC output voltage, and S main switch.

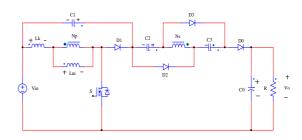


Fig.2 Proposed Converter.

The diodes  $D_2$ ,  $D_3$  and capacitors  $C_2$ ,  $C_3$  forms the switched capacitor circuit. D1, C1 are the clamp diode and clamp capacitor respectively. The operating principle is that when the switch S is ON, the input supply voltage charges the magnetizing inductor  $L_m$  which is in the primary side of the coupled inductor N<sub>p</sub>. This N<sub>p</sub> induces emf to the secondary side of the coupled inductor which makes the capacitors  $C_1$ ,  $C_2$ ,  $C_3$  to discharge in series and delivers to the load resistance. The output capacitor  $C_0$  is in charging state. When the switch S is turned OFF, the energy stored in the magnetizing inductor gets discharged and makes the capacitors C2, C3 to charge in parallel. Meanwhile, the D<sub>1</sub> is turned ON and charges the clamp capacitor C1, thus reduces the switch voltage stress and the circulating current. The energy stored in C<sub>0</sub> is delivered to the load resistance. Fig. 3 shows the typical waveforms.

#### A High Step-Up DC-DC Converter using Coupled Inductor with Fuzzy Logic Control

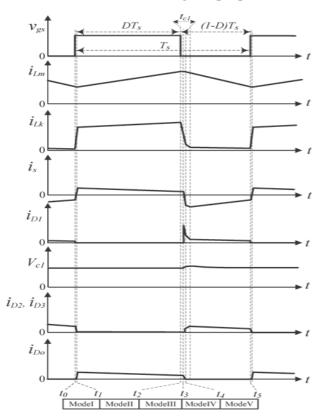


Fig.3 Waveforms of the Proposed converter.

Assumptions to simplify the circuit analysis,

- Capacitors C<sub>1</sub>, C<sub>2</sub>, C<sub>3</sub> and C<sub>0</sub> are large enough. And so, V<sub>C1</sub>, V<sub>C2</sub>, V<sub>C3</sub> and V<sub>C0</sub> are considered as constants in one switching period.
- 2. The power devices are ideal.
- 3. The coupling coefficient of the coupled inductor k is equal to  $L_m/(L_m+L_k)$ , and the turn ratio of the coupled inductor n is equal to  $N_s/N_p$ .

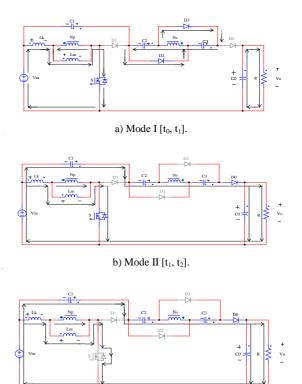
#### A. Mode of Operation

There are five operating modes in one switching period. Fig. 4 shows the current-flow path of each mode of the circuit.

- a) Mode I [t<sub>0</sub>, t<sub>1</sub>]: In this mode, S is turned on. Diodes  $D_1$  and  $D_0$  are turned off, and  $D_2$  and  $D_3$  are turned on. The current-flow path is shown in fig. 4(a).The leakage inductor L<sub>k</sub>chargedby V<sub>in</sub>. Output capacitor C<sub>0</sub>provides its energy to load R.When current i<sub>D2</sub> becomes zero at t = t<sub>1</sub>, this operating mode ends.
- b) Mode II [t<sub>1</sub>, t<sub>2</sub>]: In this mode, S remains turned on. Diode D<sub>1</sub>, D<sub>2</sub>, and D<sub>3</sub> are turned off and D<sub>0</sub> is turned on. The current-flow path is shown in fig. 4(b).Magnetizing inductor L<sub>m</sub>charges by V<sub>in</sub>. The induced voltage V<sub>L2</sub> on the secondary side of the coupled inductor makes V<sub>in</sub>, V<sub>C1</sub>, V<sub>C2</sub>and V<sub>C3</sub>, which are connected in series, discharge to high-voltage

output capacitor  $C_0$  and load R. when switch S is turned off this mode ends.

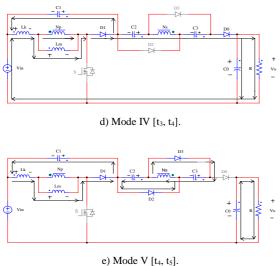
- c) Mode III [ $t_2$ ,  $t_3$ ]: In this mode, S is turned off. Diodes  $D_1$ ,  $D_2$ , and  $D_3$  are turned off and  $D_0$  is turned on. The current-flow path is shown in fig. 4(c). The energies of  $L_k$  and  $L_m$  charge the parasitic capacitor  $C_{ds}$  of main switch S. Output capacitor  $C_0$  provides its energy to load R. At  $t = t_3$ , diode  $D_1$  conducts, and this mode ends.
- d) Mode IV  $[t_3, t_4]$ : In this mode, S is turned off. Diodes  $D_1$  and  $D_0$  are turned on, and  $D_2$  and  $D_3$  are turned off. The current-flow path is shown in fig. 4(d). The energies of  $L_k$  and  $L_m$  charge  $C_1$ . The energy of  $L_k$  is recycled. Secondary-side voltage  $V_{L2}$  of the coupled inductor continues charging high-voltage output capacitor  $C_0$  and load R in series until the secondary current of the coupled inductor is equal to zero. At t = t\_4, this mode ends.
- e) Mode V  $[t_4, t_5]$ : In this mode, S is turned off. Diode  $D_1$ ,  $D_2$ , and  $D_3$  are turned on and  $D_0$  is turned off. The current-flow path is shown in fig. 4(e).  $C_0$  is discharged to load R. The energies of  $L_k$  and  $L_m$  charge the  $C_1$ .  $L_m$  is released via the secondary side of the coupled inductor and charges capacitors  $C_2$  and  $C_3$ . Thus,  $C_2$  and  $C_3$  are charged in parallel and  $L_k$  charges capacitor  $C_1$ . This mode ends at  $t = t_6$ .

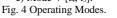


c) Mode III [t<sub>2</sub>, t<sub>3</sub>].

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#### **III. ANALYSIS OF THE PROPOSED CONVERTER**

According to [1], the energy stored in the leakage inductor  $L_k$  of the coupled inductor is released to capacitor  $C_1$ . The energy-released duty cycle  $D_{C1}$  can be expressed as

$$D_{C1} = \frac{t_{C1}}{T_s} = \frac{2(1-D)}{n+1}(1)$$

The equivalent circuit and state definition of the newly designed converter is depicted in fig.2, where the transformer is modeled as an ideal transformer.

The turn ratio of this ideal transformer is defined as

$$n = \frac{N_2}{N_1} (2)$$

From fig. 4.b),

$$V_{L1}^{ON} = \frac{L_m}{L_m + L_{k1}} V_{in} = K V_{in}$$
 (3)

$$V_{L2}^{ON} = nV_{L1}^{ON} = nKV_{in}$$

$$\tag{4}$$

$$V_0 = V_{in} + V_{C1} + V_{C2} + V_{L2}^{ON} + V_{C3}(5)$$

By Voltage Second Balance principle,

$$\int_{0}^{DT_{S}} V_{L1}^{ON} dt + \int_{DT_{S}}^{T_{S}} V_{L1}^{OFF} dt = 0(6)$$
$$\int_{0}^{DT_{S}} V_{L2}^{ON} dt + \int_{DT_{S}}^{T_{S}} V_{L2}^{OFF} dt = 0 (7)$$

V<sub>L1</sub>

By solving (6), (7), we get,

From equations (13), (17), (18) & (19) the values of  

$$= \frac{-Dk}{1-D} V_{in} (8) \qquad \begin{array}{l} L_1 = 1.48 \text{mH}, L_2 = 5.62 \text{ mH are obtained. Here the} \\ L_m \& L_k \text{ values are chosen as } 48 \mu \text{H} \& 0.25 \mu \text{H}. \end{array}$$

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$$V_{L2}^{OFF} = \frac{-nDk}{1-D} V_{in} \qquad (9)$$

As the capacitors are charged during switch OFF mode, the voltage across the capacitors can be obtained from fig.4(e),

$$V_{C1} = \frac{D}{1-D} \cdot V_{in} \cdot \frac{(1+k)+(1-k)}{2}$$
 (10)

$$V_{C2} = V_{C3} = -V_{L2}^{ON}$$

$$= \frac{\mathrm{nDk}}{\mathrm{1-D}} \mathrm{V_{in}} \left(11\right)$$

Substituting (4), (10), (11) in (5), we get,

$$V_0 = \frac{1+nk}{1-D} \cdot V_{in} + \frac{D}{1-D} \cdot \frac{(k-1)+n(1+k)}{2} \cdot V_{in}$$
(12)

$$\frac{V_0}{V_{in}} = \frac{1+nk}{1-D} + \frac{D}{1-D} \cdot \frac{(k-1)+n(1+k)}{2} (13)$$

According to the description of operating modes, voltage stresses on active switch Sand diodes  $D_1$ ,  $D_2$ ,  $D_3$ , and  $D_0$  are given as

$$V_{ds} = \frac{1}{1-D} V_{in} = \frac{V_0 + nV_{in}}{2n+1}$$
 (14)

$$V_{D1} = \frac{1}{1-D} V_{in} = \frac{V_0 + nV_{in}}{2n+1}$$
(15)

$$V_{D2} = V_{D3} = V_{D0} = \frac{n}{1 - D} V_{in}$$
$$= \frac{n(V_0 + nV_{in})}{2n + 1}$$
(16)

Equations (14)–(16) mean that, under the same voltage ratio, the voltage stresses can be adjusted by the turn ratio of the coupled inductor.

IV. DESIGNING OF PARAMETERS

Let:

Input Voltage  $V_{in}$ = 24 V Output Power  $P_0$ = 200 W Switching Frequency f = 50 KHz Load Resistance R = 800 $\Omega$ 

A. Design Of Coupled Inductor

$$\mathbf{k} = \frac{\mathbf{L}_{\mathrm{m}}}{\mathbf{L}_{\mathrm{m}} + \mathbf{L}_{\mathrm{k}}} \tag{17}$$

$$\Delta I_1 = \frac{Dk V_{in}}{L_1 f(2D-1)} (18)$$

$$\Delta I_2 = \frac{nDk \, V_{in}}{L_2 f(2D-1)} (19)$$

 $L_{\rm m} = V_{\rm in} {}^{\rm Vin} {}^{\rm (8)} L_{\rm m} \& L_{\rm k}$  values are chosen as  $48 \mu {\rm H} \& 0.25 \mu {\rm J}$ www.ijirset.com

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#### B. Selection of Switching Device

#### **IV.POWER MOSFET:**

It is chosen as switch as it is cost effective, high commutation speed, low on state resistance, improved gate and high speed power switching.

To verify the performance of the proposed converter, circuit is simulated using MATLAB software. The Converter specifications are as follows:

- 1) Input dc voltage  $V_{in} = 24 V$
- 2) Output dc voltage  $V_0 = 400 \text{ V}$
- 3) Maximum output power  $P_0 = 200 \text{ W}$
- 4) Switching frequency f = 50 kHz
- 5) Capacitors  $C_1 = 56 \ \mu F$  $C_2/C_3 = 22 \ \mu F$  $C_0 = 180 \ \mu F$
- 6) Coupled inductor n = Np:Ns= 1: 4  $L_m\&L_k = 48 \ \mu H\& 0.25 \ \mu H$

#### V. FUZZY LOGIC CONTROLLER DESIGN

The block diagram of fuzzy logic controller (FLC) is shown in fig.5. It consists of three main blocks: fuzzification, inference engine and defuzzification. The two FLC input variables are the error E and change in error E\*. Depending on membership functions and the rules FLC operates.

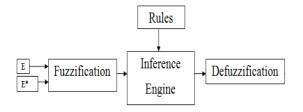


Fig.5 Block Diagram of FLC.

#### A. Fuzzification

The membership function values are assigned to the linguistic variables using seventeen fuzzy subsets. Table-I shows the rules of FLC. E and E\* are input variables, where E is the error between the reference and actual voltage of the system,  $E^*$  is the change in error in the sampling interval.

#### B. Inference Engine

Mamdani method is used with Max-Min operation fuzzy combination. Fuzzy inference is based on fuzzy rules. Rules are framed in inference engine block. The output membership function of each rule is given by MIN (Minimum) operator and MAX (Maximum) operator.

#### C. Defuzzification

The output of fuzzy controller is a fuzzy subset. As the actual system requires a non fuzzy value of Control, defuzzication is required. Defuzzifier is used to convert the linguistic fuzzy sets back into actual value. The membership functions of error (E), change in error (E\*) and Duty ratio (D) are shown in fig. 6, 7, 8.Fig.9 shows the representation of the typical Rule Surface of fuzzy logic controller.

TABLE-I Rule Table for FLC

E E	Ν	Z	Р
N8	N7	N8	N6
N7	N6	N7	N8
N6	N5	N6	N7
N5	N4	N5	N6
N4	N3	N4	N5
N3	N2	N3	N4
N2	N8	N2	N3
N1	N8	Ζ	P2
Z	P1	Ζ	N1
P1	P2	P1	Z
P2	P3	P2	P1
P3	P4	P3	P1
P4	P3	P4	P3
P5	P6	P5	P5
P6	P7	P6	P5
P7	P8	P7	P6
P8	P8	P8	P7

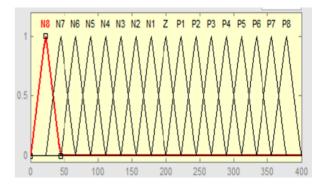


Fig.6 Membership Functions of Error (E).

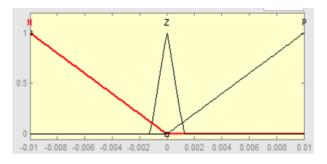


Fig.7 Membership Functions of Change in Error (E\*).

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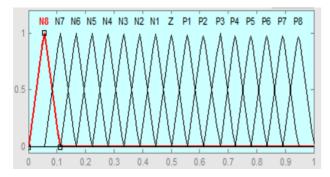


Fig.8 Membership Functions of Duty Ratio (D).

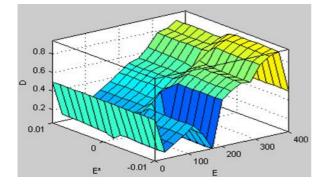


Fig.9 Surface View of Rules of FLC.

# VI.SIMULATION DIAGRAMS

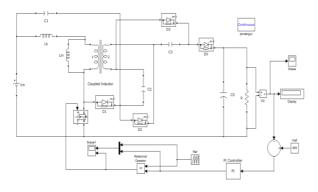


Fig.10 Proposed Converter with PI controller.

Fig.10 shows, A24 V input voltage is fed to the converter, an output voltage of 398.3 V is obtained which is fed back as a feedback voltage to the PI controller; there it compares the feedback and the reference signalfromwhichPWM pulse is generated which triggers the main switch of the converter.

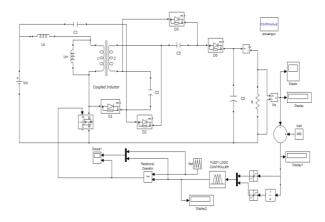


Fig.11 Proposed Converter with FLC.

In fig.11, for the same input voltage the converter is controlled by the newly designed FLC now 399.4 V output voltage sobtained.

#### VII.SIMULATION RESULTS

# A. Simulation Results of Proposed converter with PI controller

Fig. 12 shows the response of the converter with PI controller.

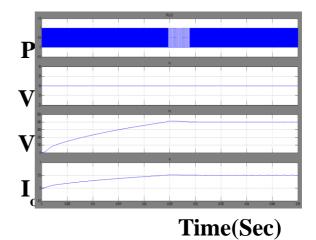
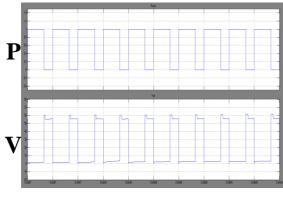


Fig.12 Pulse, Input Voltage,Output Voltage & Output Current ( $V_{in} = 24 V, V_0 = 398.3 V \& I_0 = 0.5 A$ ).

The switch voltage stress of the converter with PI controller is shown in fig. 13.

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Time(Sec)

Fig.13 Pulse, Voltage across Switch ( $V_{ds}$ = 55 – 60 V).

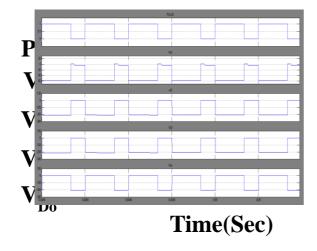


Fig.14 Pulse, Voltage across  $Diodes(V_{D1}=60 \text{ V}, V_{D2}=V_{D3}=V_{D0}=200 \text{ V}).$ 

#### B. Simulation Results of Proposed Converter with FLC

From fig 15, it is clear that for the designed parameters, required output voltage and current is obtained. The duty ratio of the switch is adjusted by FLC to obtain the require output and also the voltage drift problem is eliminated.

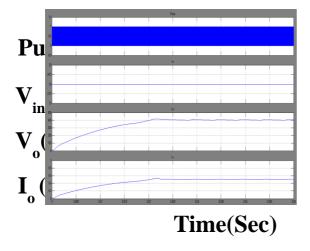
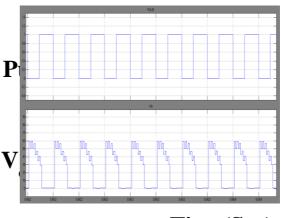


Fig.15 Pulse, Input Voltage Output Voltage & Output Current ( $V_{in} = 24$  V,  $V_0 = 399.4$  V&  $I_0 = 0.5$  A).

Further from fig 16, the voltage stress of switch is much reduced than the circuit with PI controller.



Time(Sec)

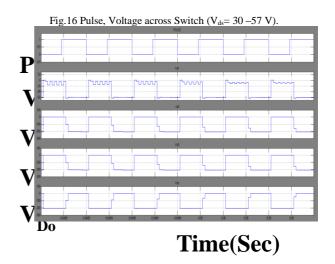


Fig.17 Pulse, Voltage across Diodes.(V<sub>D1</sub>=60 V, V<sub>D2</sub>=V<sub>D3</sub>=V<sub>D0</sub>=200 V).

From fig.17,  $V_{D2}$ ,  $V_{D3}$ ,  $V_{D0}$  equal and so, they are under the same voltage ratio, the voltage stresses can be adjusted by the turn ratio of the coupled inductor.

TABLE.II
COMPARISON BETWEEN PROPOSED CONVERTER WITH PICONTROLLER
&FLC

S.No	Туре	Input Voltage (V)	Output Voltage (V)	Voltage Gain	Switch Voltage Stress (V)
1	Converter with PI controller	24	398.3	16.5	55-60
2	Converter with FLC	24	399.4	16.6	30-57

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### VIII.CONCLUSIONS

Here a high step-up dc–dc converter using coupled inductor with fuzzy logic control is simulated. By the capacitor charged in parallel and discharged in series by the coupled inductor, high step-up voltage gain is achieved. As the output voltage of the converter with FLC has minimum overshoot and produces a constant output current shows the better performance compared to the converter with PI controller. These studies could solve many types of problems regardless on stability because as we know that fuzzy logic controller is an intelligent controller to their appliances. Additionally, the switch voltage stress is reduced, thus a switch with low voltage ratings can be selected.

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