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A Modified UPQC Topology Using Fuzzy Based Control of VSI with Reduced DC Link Voltage Rating

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ABSTRACT—A custom device that mitigates simultaneously the voltage and current concerned Power Quality issues in the power distribution systems, is the unified power quality conditioner (UPQC). This paper presents a modified UPQC topology for three-phase-four wire system. The proposed topology helps in matching the DC-link voltage necessity of shunt and series inverter at reduced rating, without any compromise in the performance. The performance of modified UPQC topology using PI and fuzzy controller has been studied comparatively. The effectiveness of the proposed system is verified using the MATLAB simulations.

KEYWORDS— Direct current (DC), Proportional Integral (PI), Power Quality (PQ), MATLAB/SIMULINK, Unified Power Quality Conditioner (UPQC).

1. INTRODUCTION

With the wide applications of power electronics devices, such as the uninterrupted power supply, adjustable speed drives, etc., in distribution systems, power-quality (PQ) problems, such as flicker, harmonics, and voltage fluctuations are increasing. Various network faults, lightning, and switching of capacitor banks may cause various PQ problems, such as voltage sag/swell [1]. On the other hand, telecommunication, information technology and semiconductor manufacturing industries are more sensitive to PQ problems than before and need high-quality power. Under these circumstances, a new technology called "custom power" emerged, which is applicable to the distribution system for enhancing the reliability and PQ. A unified PQ conditioner (UPQC) is a versatile device which can do the work of DSTATCOM and DVR [2],[3]. The UPQC can simultaneously fulfil different objectives, such as maintaining a sinusoidal nominal voltage at the bus at which it is connected, maintaining voltage when there are voltage sags and swells in the system, eliminating source currents harmonics, correcting the power factor at source side, and balancing load. Recent research focuses on use of the universal power quality conditioner (UPQC) [4] to compensate for power-quality problems. The UPQC performance mainly depends upon how accurately and quickly reference signals are derived. After efficient extraction of the distorted signal, a suitable dc-link current regulator is used to derive the actual reference signals. The controller is the most significant part of the active power filter and currently various control strategies are proposed by many researchers. There are two major parts of the controller; one is the reference current

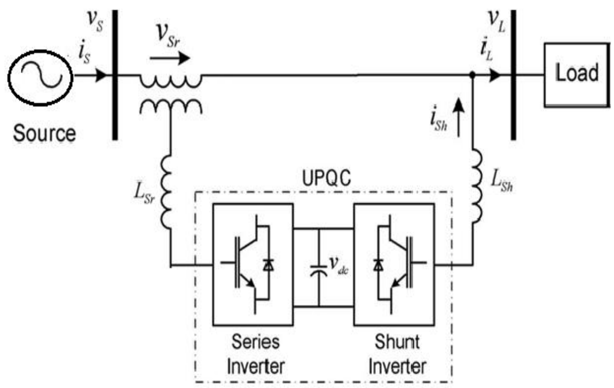


Fig.1UPQC block diagram

extraction from the distorted line current and another is the PWM-current controller to generate switching patterns for inverter. Many control strategies are proposed in the literature to extract the harmonic components.

However, the conventional PI controller requires precise linear mathematical model of the system, which is difficult to obtain under parameter variations and non-linear load disturbances. Another drawback of the system is that the proportional and integral gains are chosen heuristically. Recently, Fuzzy Logic Controllers (FLCs) have been used in various power electronic applications and also in active power filters.The advantage of FLCs over the conventional controllers is that it does not need an precise mathematical model. It is capable of handling nonlinearity and is more robust than conventional PI or PID controllers

II. PROPOSED TOPOLOGYOF UPQC

In this section the proposed modification in the topology of the UPQC is viewed elaborately. Fig. 1 shows the modified UPQCtopology. In this figure, V_{sa}, V_{sb}, and V_{sc}represents phases *a*, *b*, and *c*source voltages respectively. And also, the terminal voltage of the phases is represented by V_{ta}, V_{tb}, and V_{tc}. The voltages injected by the series active filter areV_{dvra}, V_{dvrb}, and V_{dvrc}. The threephase source currentsare represented by i_{sa}, i_{sb}, i_{sc}, and i_{la}, i_{lb}, and i_{lc} are the load currents. i_{fa}, i_{fb},i_{fc}, denote the shunt active filter current andthe current in the neutral leg is i_{ln}. L_s and $R_s$are the inductance and resistance of the feeder, respectively. Also L_f and R_f, are the interfacing inductance and resistance of shunt active filter represented respectively, and the interfacing inductance and filter capacitor of the seriesactive filter are represented by $L_{se}$and C_{se}, respectively. The load may constitute both linear and nonlinear load as shown in this Fig 2.

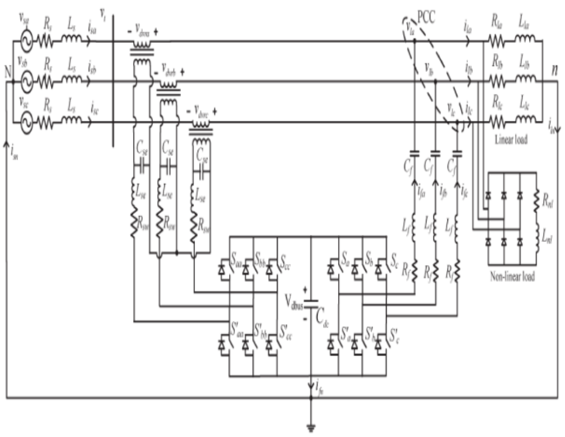


Fig 2: Equivalent circuit of modified UPQC topology

In this topology [11], the system neutral has been attached to the negative terminal of the dc bus along with the capacitor $C_f$in series with the interfacing inductance of the shunt active filter. This topology is referred to as modified topology. The passive capacitor $C_f$is capable of supplying a part of the reactive power needed by the load, the active filter will counterbalance the reactive power and the harmonics present in the load. The addition of series capacitor with the shunt active filters interfacing inductor will significantly decreases the dc-link voltage requirement, therefore reducing the average switching frequency of the switches. This concept is presented with analytic description in the section which follows. The decrease in requirement of the shunt active filters dc-link voltage helps us to the match the dc-link voltage requirement with the seriesactive filter. This topology avoids the over rating of the seriesactive filter of the UPQC compensation system. This topology uses a single dc capacitorunlike the neutral-clamped topology and consequentlyavoids the need of balancing the dc-link voltages. Each leg ofthe inverter can be controlled independently in shunt active filter. Unlike the topologies mentioned in the literature [5],[6],[8], this topology does not require the fourth leg in the shunt active filter for three-phase four-wire system.

III. CONTROL STRATEGY

Among the several control strategies of Active Power Filtergiven in the literature [7],[9], the Synchronous Reference Frame-based control method is the conventional and the most practical methods. The SRF method [10] poses excellent characteristics but it requires decisive Phase Lock Loop techniques. The SRF control method uses $a-b-c$ to $d-q-0$ transformation equations, filters, and the modified PLL algorithm shown in Fig. 2. The proposed method is simple andeasy to implement and offers reduced current measurement, therefore it is efficient in DSP platforms. Hence under unbalanced and distorted load conditions the proposed control strategy can drastically improve the performance of the modified UPQC topology.

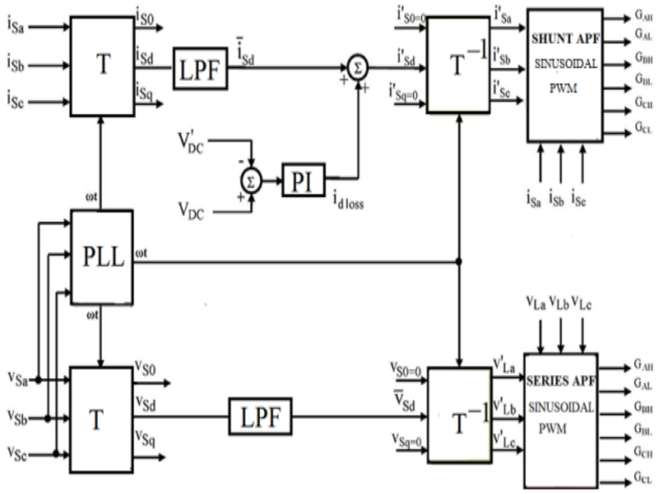


Fig 3: Proposed SRF based UPQC control block diagram

A. Reference-Voltage/Current Signal Generation for Voltage Source Inverter

The series inverter reference-voltage signal-generation is shown in Fig. 3. In (4), the supply voltages V_{Sabc} are transformed $d-q-0$ by using the transformation matrix **T** given in (1). Inaddition, the modified Phase Lock Loop conversion is utilized in reference voltage calculation.

$$T=\sqrt{\frac{2}{3}}\begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ \sin(\omega t) & \sin(\omega t-2\pi/3) & \sin(\omega t+2\pi/3) \\ \cos(\omega t) & \cos(\omega t-2\pi/3) & \cos(\omega t+2\pi/3) \end{bmatrix} \quad (1)$$

$$T^{-1}=\sqrt{\frac{2}{3}}\begin{bmatrix} 1/\sqrt{2} & \sin(\omega t) & \cos(\omega t) \\ 1/\sqrt{2} & \sin(\omega t-2\pi/3) & \cos(\omega t-2\pi/3) \\ 1/\sqrt{2} & \sin(\omega t+2\pi/3) & \cos(\omega t+2\pi/3) \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} v_{s0} \\ v_{sd} \\ v_{sq} \end{bmatrix} = T \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \quad (3)$$

The instantaneous source voltages ($V_{Sd}$and V_{Sq}) include both oscillating components ($\widetilde{V_{sd}}\, and \widetilde{V_{sq}}$) and average components($\overline{V_{sd}}\, and \overline{V_{sq}}$) under unbalanced source voltage with harmonics. The oscillating components of $\widetilde{V_{sd}}$ and V_{sq} consist of theharmonics and negative-sequence components of the source voltages under distorted load conditions. An average component includes the positive-sequence components of the voltages. The zero-sequence part (V_{S0}) of the source voltage occurs when the source voltage is unbalanced. The source voltage in the *d*-axis (V_{Sd}) given in (4) includes average and oscillating components.

$$V_{sd} = \overline{V_{sd}} + \widetilde{V_{sq}} \quad (4)$$

The load reference voltages (V'_{Labc}) are calculated as given in (6). The inverse transformation matrix $\mathbf{T}^{-1}$ in (2) is applied for developing the reference load voltages by the average component of sourcevoltage and ωtproduced in the modified PLL algorithm. The source-voltage positive-sequence average value (V_{sd}) in the *d*-axis is calculated by Low Pass Filter, as shown in Fig. 3. Zero and negative sequences of source voltage are set to zero so that load voltage harmonics, unbalance, and distortion can be compensated, as shown in Fig. 3

$$\begin{bmatrix} V'_{La} \\ V'_{Lb} \\ V'_{Lc} \end{bmatrix} = T^{-1} \begin{bmatrix} 0 \\ V_{sd} \\ 0 \end{bmatrix} \quad (5)$$

The switching signals for insulated-gate bipolar transistor (IGBT) are generated by comparingthe produced load reference voltages (V'_{La}, V'_{Lb}, and V'_{Lc}) and load voltages (V_{La}, V_{Lb}, and V_{Lc}) in the sinusoidal pulse width modulation controller. So as to compensate all voltage-concerned issues, such as voltage harmonics, sag, swell, voltage unbalance, etc., at the Point of Common Coupling (PCC).

The similar operation carried out for shunt inverter, in which the voltage of series inverter is replaced by current. Hence, used in compensating the current harmonics generated by the nonlinear load and the active power is injected to the power system by the series active power filter so that the active power losses of the UPQC power circuit, which causes dc-link voltage reduction, is compensated. Some active power should be absorbed from the power system by the shunt active power filter to regulate dc-link voltage. With this intention, comparing the dc-link voltage with its reference value (V_{DC}), and the required active current (i_{dloss}) is found by a PI controller. By adding to the required active currentand source current average component (i_{Sd}), which is obtained by a low pass filter, as given in (6), the fundamental referencesource current component is computed.

$$i'_{sd} = i_{dloss} + \overline{i_{sd}} \quad (6)$$

1)PI-Controller: The DC-side capacitor voltage is detected and compared with voltage reference. The obtained result of the voltage error e = $V_{dc,ref}$– V_{dc}at the particular sampling instant is the input for Proportional Integral (PI)-controller. The error signal passes through Low Pass Filter (LPF) to filter the higher order componentsand passes only the fundamental. It transfer function is defined as [8],

$$H(s) = K_P + K_I/s. \quad (7)$$

The proportional gain is derived using $K_P = 2\zeta\omega_{nv}C$ [K_P= 0.1]. It determines the dynamic response of the voltage at the DC-side. Thedamping factor $\zeta = \sqrt{2} / 2$ and natural frequency ω_{nv}shouldbe chosen as the supply fundamental frequency. Similarly, theintegral gain is derived using $K_I= C\omega_{nv}^2$[K_I= 1] that determinessettling time and eliminates steady state error in the DC-side capacitor voltage. This controller estimates the magnitude of peak reference current $I_{max}$and controls the dc-side capacitor. This estimated magnitude of peak current multiplies with output of unit current vector, which generates the required reference currents tocompensate the harmonic components.

2) Fuzzy logic controller: Fuzzy logic control is inferred from fuzzy set theory, which was introduced by Zadeh in 1965 [12]. The fuzzy set theory develops a transition between membership and non-membership function. Therefore, limitation or boundaries of fuzzy sets can be undefined, ambiguous and useful for approximate systems design. In order to implement the fuzzy logic control algorithm the dc-bus capacitor voltage is sensed and compared with the desired reference value. This computed error signal (e =V_{DCref}– V_{DC})is passed through a LPF.

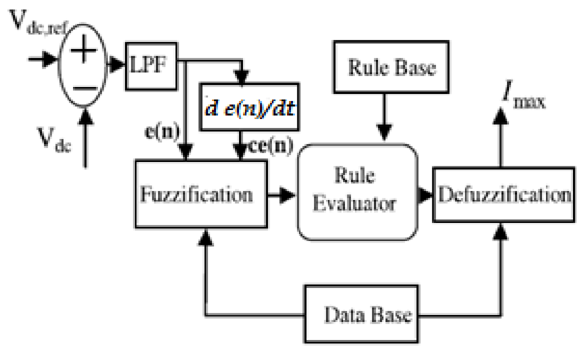


Fig 4: Fuzzy logic controller

The error signal e(n) andintegration of error signal or change of error signal ce(n) are taken as inputs for fuzzy processing as shown in Fig. 4.Fuzzy logic is characterized by (1) Seven fuzzy sets (NB, NM, NS, ZE, PS, PM, PB) for each input and output variables. (2) Triangular membership function is usedfor the simplicity (3) Implication using Mamdani-type min -operator. (4) Defuzzification

TABLE I
RULE BASE TABLE

e(n)	C e(n)						
	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NM	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

The 49-rules are used in this proposed controller as given in Table 1. The output of the fuzzy controller measures the amplitude of peak reference current I_{max}. The current I_{max}takes response of the active power demand for harmonics and reactive power compensation. This estimated magnitude of peak-current multiplies with output of unit current vector and generates the required reference currents. These reference currents compared with actual currents to generate the inverter switching patterns using sinusoidal PWMcontroller.

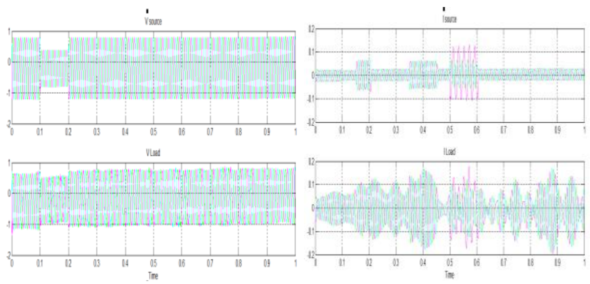
IV. RESULTSAND DISCUSSION

An ideal three-phase sinusoidal supply voltage of 33kV, 50Hz is applied to the non-linear load injecting current harmonics into the system.

TABLE II
SIMULATIONPARAMETERS

Source	Voltage	3ϕ, 33Kv, 50Hz
	Impedance	R=1Ω;L=3.3mH
DC-link	Capacitor	C=80µF
	Reference Voltage	V=12.5Kv
Inverter parameters	MOSFET	3-arm, 6 pulse
	Carrier frequency	f=30KHz
	Sampling time	t=5µsec
Series Inverter	Filter	R=1Ω;L=3.3mH;C=0.1µF
	Transformer	3ϕ-linear transformer,33/15Kv
Shunt Inverter	Filter	R=1Ω;L=3.3mH;C=4700µF
	Transformer	3ϕ-linear transformer, 33/3.3Kv
PI Controller	Series inverter	K_p =0.1;K_i =1
	Shunt inverter	K_p =0.1;K_i =1

Fig. 5(b) shows supply current in three phases before compensation, and after compensation from. Shunt inverter is able to reduce the harmonics from entering into the system. The Total Harmonic Distortion (THD), which was 20.02% (Fig. 9) before compensation was effectively reduced to 8.74 % (Fig. 11 (b)) after compensation using PI controller. Fig 5 shows the voltage in three-phase before and after compensation. Here the sag originating in the supply side is mitigated by the series inverter.THD in source side is 1.49% is very less than in the supply side of 13.98% Fig. 10



(a) (b)

Fig 5: (a) Three phase voltage and (b z) Three phase current

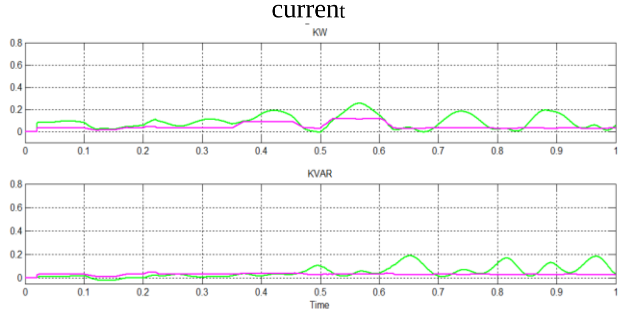
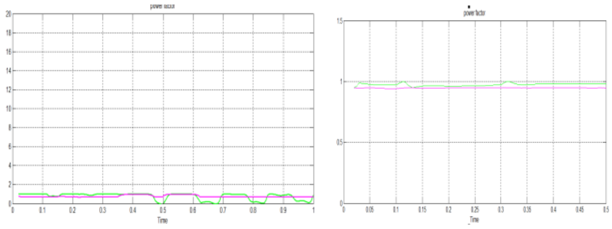


Fig 6: Real and reactive power of modified upqc with PI controller

Fig. 6 and shows the active power and reactive power through the line with modified UPQC connected to a distribution system. The custom device introduced controls the active power flow through the line and the existing capability of the transmission line is appreciably improved with the presence of modified UPQC. This is due to the decrease in transmission losses, which are minimized with the help of the modified UPQC. It also helps in improving power factor of the transmission line. As shown in Fig. 7(a) without UPQC, power factor of the transmission line is 0.8944 but as modified UPQC is switched, the power factor is enhanced to 0.977 Fig. 7(b). The transmission capability enhancement is also observed from the simulation results.



(a) (b)

Fig.7 (a) Power factor without and (b) with modified upqc using PI controller

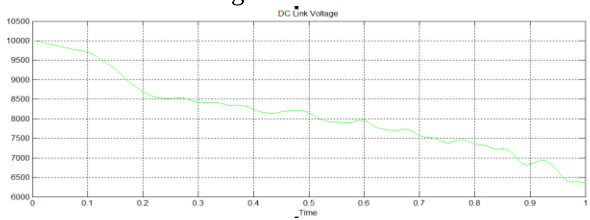


Fig 8: DC-link voltage rating of modified upqc with PI controller

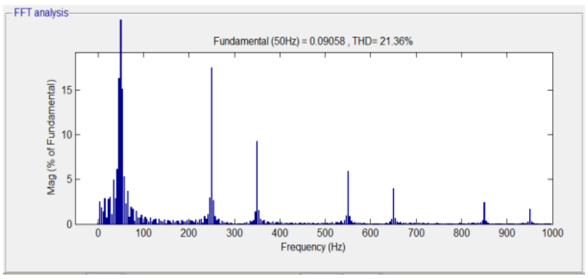
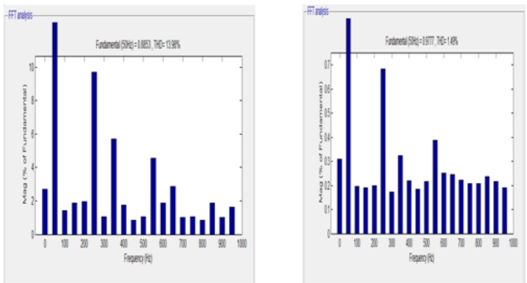
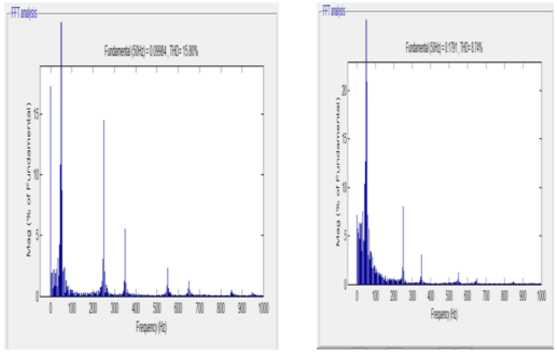


Fig 9: Current THD without Compensator



(a) (b)

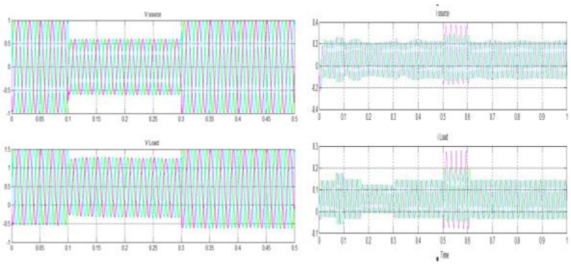
Fig 10: THD of (a) load voltage (b) source voltage



(a) (b)

Fig 11: THD of (a) load current (b) source current of modified upqc using PI controller

Now the fuzzy controller is implemented instead of traditional PI controller.Fig.12 (a) and (b) show the source voltage and source current respectively.



(a) (b)

Fig.12 Three phase (a) voltage (b) current waveform using FLC in modified upqc topology

Fig. 14(a) is the dc link voltage (voltage across the dc capacitor) that feeds both the shunt and series inverters. Drawing the charging current from the supply, the capacitor is effectively charged to the reference voltage(V_{dc}). Fuzzy controller holds V_{dc} constant once the capacitor is charged to required value.Further there is drop in the capacitor voltage when it feeds shunt inverter is not significant, because shunt inverter compensating the load current harmonics, supply only reactive power.

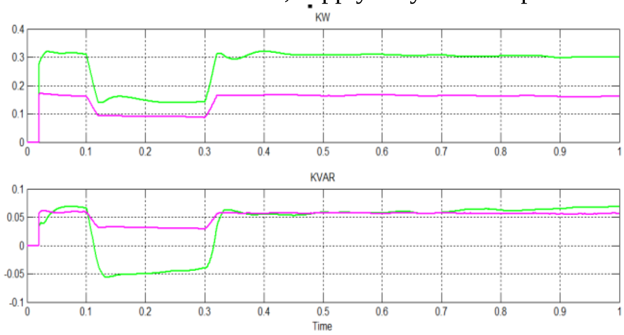
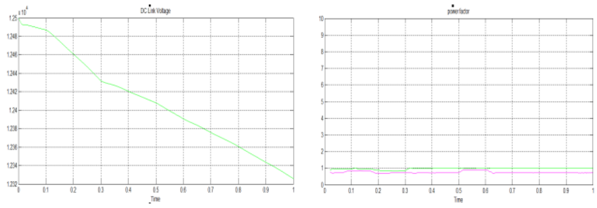


Fig 13: Real and reactive power using FLC in modified upqc

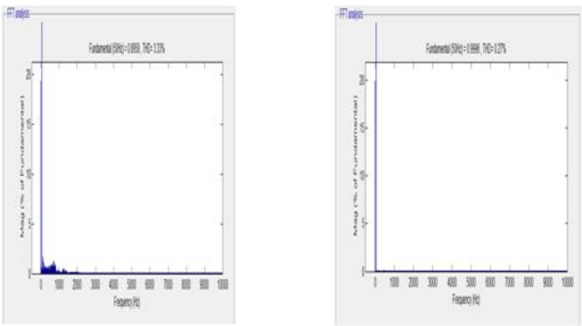
It also helps in improving power factor at the source side. As shown in Fig. 7 (b), power factor of the transmission line is 0.977 for UPQC with PI controller. But as UPQC is switched with fuzzy logic controller, the power factor increases to 0.998 Fig 14 (b), which is close to unity at the source side.



(a) (b)

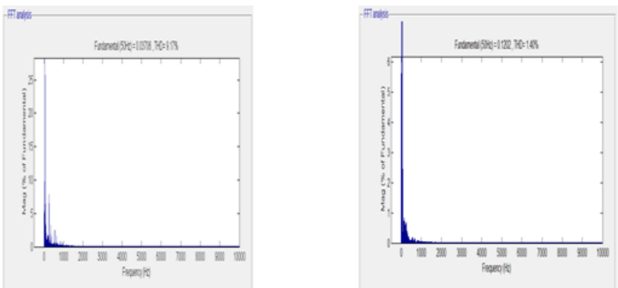
Fig 14: (a) Dc-link voltage (b) power factor of modified upqc using FLC

After switching on the modified UPQC using FLC, source current becomes sinusoidal and from Fig. 16(b) theTotal Harmonic Distortion of compensated source current is 1.40% which is less compared to traditional PI controller. The source voltage THD is 0.27% as shown in Fig. 15(b).



(a) (b)

Fig 15: THD of (a) load voltage (b) source voltage



(a) (b)

Fig 16: THD of (a) load current (b) source current of modified upqc using FLC

VI. CONCLUSION

Table 3 shows simulated performance parameters of PI controller and fuzzy logic controller. It isclearly evident from Table 3 that fuzzy logic control having an edge over PI controller. Results shown in Table 3 are verified one by one.

TABLE III
SIMULATIONRESULTSOBTAINED

S.no	Factors	PI Controller	Fuzzy Controller
1	Source current THD	8.74%	1.40%
2	Dynamic Response	Slow (0.2s)	Fast (0.10s)
3	Capacitor Charging	Slower	Faster
4	Capacitor Voltage balance under unbalanced load condition	Less stable	More stable
5	Source voltage THD	1.15%	0.27%

Results obtained from the simulation show better performance of modified UPQC when fuzzy logic controller is used than that of the PI controller in terms of harmonic compensation, capacitor charging and dc capacitor voltage balancing under unbalanced load conditions. Under the unbalanced load condition the dynamic response of PI controller is not good enough as Fuzzy logic controller, it is proved to be faster. Further time consumption is less and it is more accurate method than PI controller as it does not require frequent tuning. Hence it is proved that fuzzy logic controller is superior to PI controller.

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