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Sub-Threshold Logic and Standard Cell Library

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Abstract: This paper presents the sub-threshold logic and standard cell library for it. Standard cell library consists of basic gates as well as universal gates (INVERTER, EX-OR, NAND, NOR gate) in sub-threshold logic. The components of this library can be used to design any complex combinational circuit utilizing less power as compared to super-threshold one. Impact of sizing of nmos and pmos is also given in this paper. There is also a comparison between sub-threshold and super-threshold logic.

Keywords: Sub-threshold logic, standard cell library, sizing of mos.

I. INTRODUCTION

The demand for low power electronics is rising day by day. In this era of hand held devices long battery life is a very important criterion for electronics industries. Everyone wants long battery life for their device. This all started from the Moore's Law. In 1965, Gordon Moore observed that the number of transistors that can be placed on a single IC (Integrated Circuit) of the same area has been doubling every two years [1]. It affected the semiconductor industry positively. Transistors shipped per year have increased exponentially as the average price per transistor has dropped off exponentially with the minimum feature size. An additional benefit of this scaling is the increased performance of circuits. From there The Integrated Circuits (ICs) world is accustomed till this point to following Moore's Law. But unexpectedly process scaling has a number of problems which blocks to move on exponentially. Some of them are

- Increased power dissipation
- Increased complexity etc.

Main concern which hampers the further scaling of transistors is the issue of power dissipation. A chip consist of many energy storage elements, mainly capacitors, some that are required for computation (MOSFET device capacitances) and some that are a hindrance to circuit operation (parasitic capacitances). These capacitors are continually charged and discharged through resistive elements during circuit operation, resulting in energy dissipation in the form of heat. The amount of heat dissipated puts a restriction on the computational performance of the circuit. While shrinking of devices has reduced the amount of parasitic capacitance and this alleviates power dissipation problems. But the number of devices (dissipating power somewhat less) accommodated has been increased due to process scaling which results in more power dissipation as compared to previous one. As the more number of transistors are placed on a single chip, the sub- threshold leakage current becomes dominant factor of total power dissipation. Sub-threshold leakage current occurs when transistor is off. So the leakage current dissipates power, even when it is not doing any useful computations, in the form of heat. The MOS-FET threshold voltage V_T decreases with increase in the device junction temperature caused by this heat dissipation. The sub-threshold leakage currents are exponentially dependent on V_T , increasing with decrease in V_T . Thus increased on-chip temperatures cause more power dissipation due to increased leakage currents and increased dissipation of heat. Another problem with aggravated on-chip temperature is that they can result in reduced operating life spans for the chip [2].

II. SUB-THRESHOLD LOGIC

As seen above the sub threshold current is present in our circuit, but is of no use. So let us use these sub-threshold current for operation of our circuit. The idea of using sub-threshold current for circuit is known as sub-threshold logic. Here the V_{DD} of the circuit is set at a value lower than or equal to the threshold voltage of that particular process technology, i.e. $V_{DD} \leq V_T$. Figure 2.1 shows the dependence of drain current (I_D) on applied Gate to Source voltage (V_{GS}). This can be seen that below threshold voltage the current through the transistor is exponential in nature. The circuit will thus operate with only sub-threshold leakage currents, since the transistors in the circuit will

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never be in the linear or saturation region. This approach not only results in very low power consumption but it also utilizes leakage currents for computation.

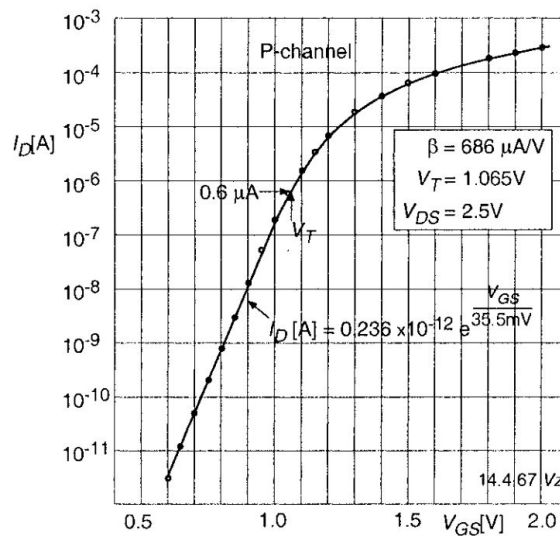


Fig. 2.1: I_D versus V_{GS} plot, for 0.18 μ m process with $V_{DD} = 1.8V$

The current through transistor in sub-threshold region for low V_{DS} roll-off can be given as [3]:

$$I_{D \text{ Sub-threshold}} = I_0 \exp\left(\frac{V_{GS} - V_T}{\eta V_{th}}\right) \left(1 - \exp\left(-\frac{V_{DS}}{V_{th}}\right)\right)$$

Where I_0 is the drain current, with $V_{GS} = V_T$, given as :

$$I_0 = \mu_0 C_{ox} \frac{W}{L} (n-1) V_{th}^2$$

Making V_{DD} lower reduces the current significantly. This reduced current is not sufficient to charge the load capacitance fast enough. Due to this slow charging of load capacitance the circuit as a whole works becomes slow.

To make the circuit fast we have to increase the current significantly upto a level enough to charge the load. For increasing the current, size of transistors are increased. Increasing the transistor size reduces the channel resistance upto certain extent but after this again the channel capacitance increases which becoming dominant factor for the fast operation of the circuit. This results in increased RC time constant of the circuit, Due to this increased RC time constant again circuit becomes slow. A proper sizing of transistor becomes very important because of the reasons given above.

III. STANDARD CELL LIBRARY

This section describes the design of various digital logic cells in sub-threshold. A methodology for designing a standard cell library in sub-threshold is discussed. All the logic cells are verified for their performance characteristics. One of the primary reasons to form a standard cell library is to use these cells as basic building blocks for larger circuits.

The standard cell library created consists of basic CMOS gates designed using 0.18 μ m technology. First, the basic CMOS inverter, shown in Figure 3.1, is analysed in detail and then, based on this analysis, the NAND and the NOR gates are designed.

A. Sub-threshold Inverter

The inverter is truly the nucleus of all digital designs. Once its operation and properties are clearly understood, designing more intricate structures such as NAND gates, adders and multipliers is greatly simplified. The analysis of

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inverters can be extended to explain the behaviour of more complex gates such as NAND, NOR, or XOR, which in turn form the building blocks for modules such as multipliers and processors.

Figure 3.1 and 3.2 show the schematic and dc characteristics of inverter respectively.

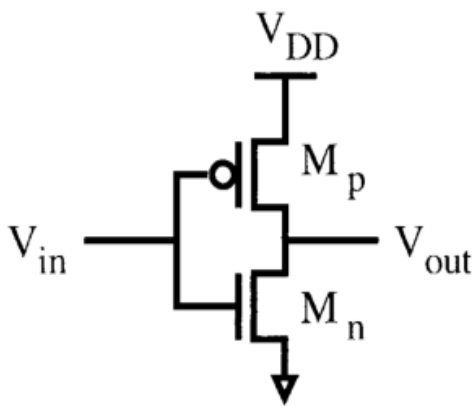


Fig 3.1: Schematic of inverter.

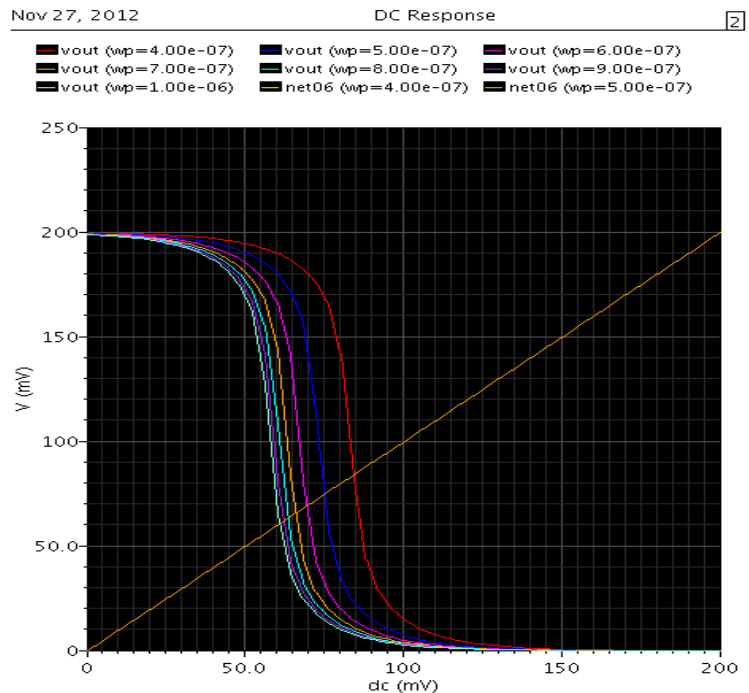


Fig. 3.2: DC characteristics of an inverter for different W_p and $W_n = 400\text{nm}$ at $V_{DD} = 200\text{mV}$.

As seen from figure 3.2 the DC response is same as far as shape is concern. So now the question arises that what should be the width of PMOS and NMOS. We will see this now that how to decide the width.

B. Sizing of inverter

Traditionally, the PMOS is sized so that the drive strength is large enough to pull the output node up to a desired output high voltage level. Figure shows two cases where the decreased supply voltage, transistor sizing and process variations affect the inverter operation assuming an output swing of 10% to 90% of V_{DD} [4].

Case 1: When 0 is applied to the input, then the PMOS is sized to pull-up the output node to 1. However, as the voltage supply of the inverter decreases, the idle current becomes significant. This results in a decreasing I_{on}/I_{off} , and causes the output node to drop. The I_{on}/I_{off} ratio is used to indicate if a logic gate will function properly. I_{on} is defined to be the drive current of the devices and decreases exponentially as supply voltage is lowered in sub-threshold operation. I_{off} is defined as the idle current. The ratio is further reduced when considering process variations. The worst case corner for the inverter is the fast NMOS/slow PMOS (FS) because the fast NMOS is leakier than the slow PMOS. Figure 3.3 shows at the FS corner, where is the minimum allowable PMOS width that still drives the output to $0.9 V_{DD}$ [4].

Case 2: When 1 is applied to the input, the minimum sized NMOS pulls the output node to 0. A large W_p leads to a large PMOS idle current compared to the drive current of the NMOS. Therefore, there is a maximum bound on W_p , to allow the output to be driven low. The slow NMOS/fast PMOS (SF) corner sets in Figure 3.3. The intersection of the curves at these two process corners indicates that the inverter is only guaranteed to operate down to 195 mV by sizing the PMOS to be $5.4\mu\text{m}$, which is 13 times the minimum width. However, for a typical transistor process corner, the inverter can operate below 100 mV [4].

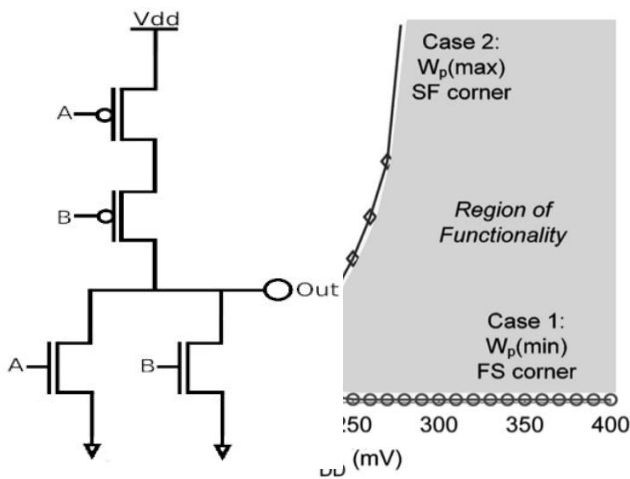


Fig 3.3: Determination of transistor width for minimum voltage operation.

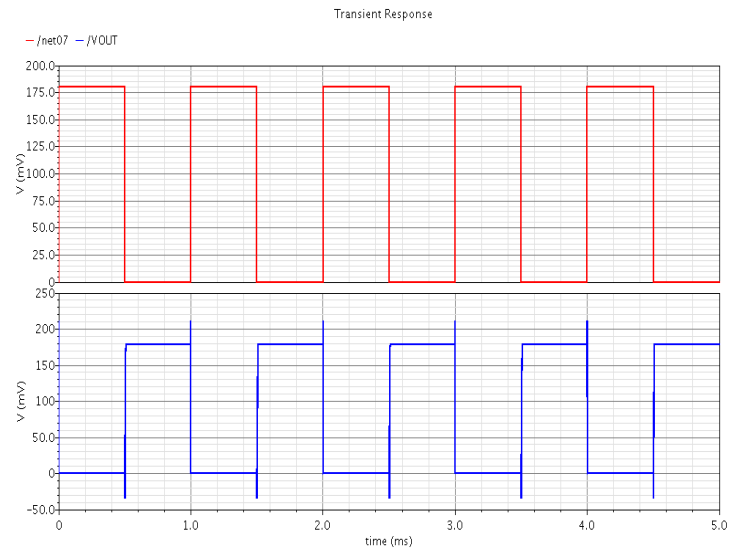
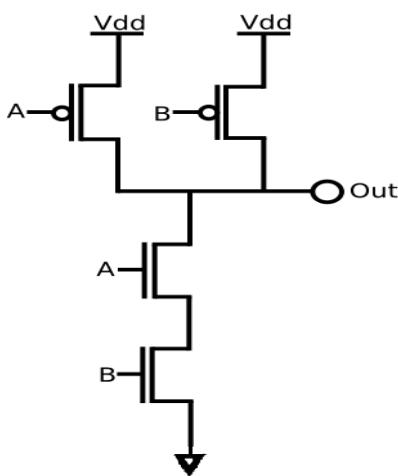


Fig 3.4: Transient response of inverter for $V_{DD}= 180mV$.

C. NAND Gate

Figure 3.5 shows the schematic of NAND gate and figure 3.6 shows its transient response.



inverter for $V_{DD}= 180mV$.

Fig 3.5: Schematic of NAND Gate.

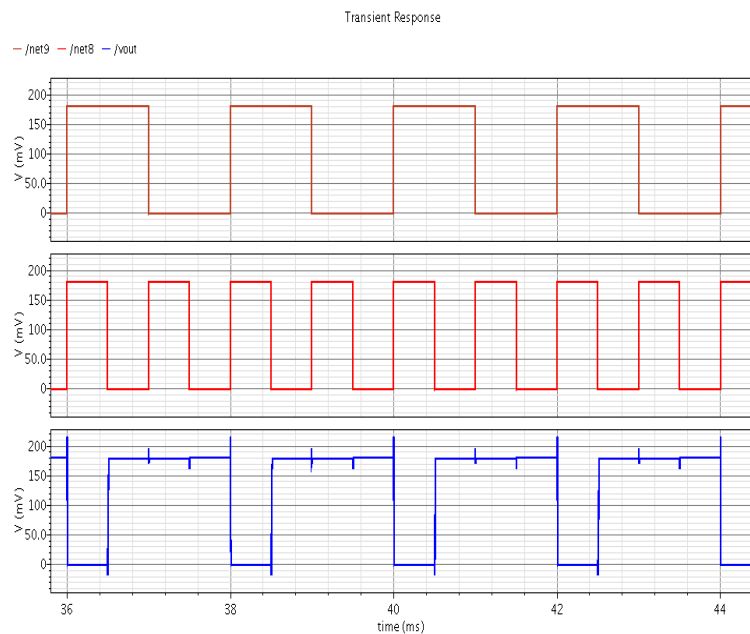


Fig 3.6: Transient response of

D. NOR Gate

Figure 3.7 shows the schematic of NOR gate and figure 3.8 shows its transient response.

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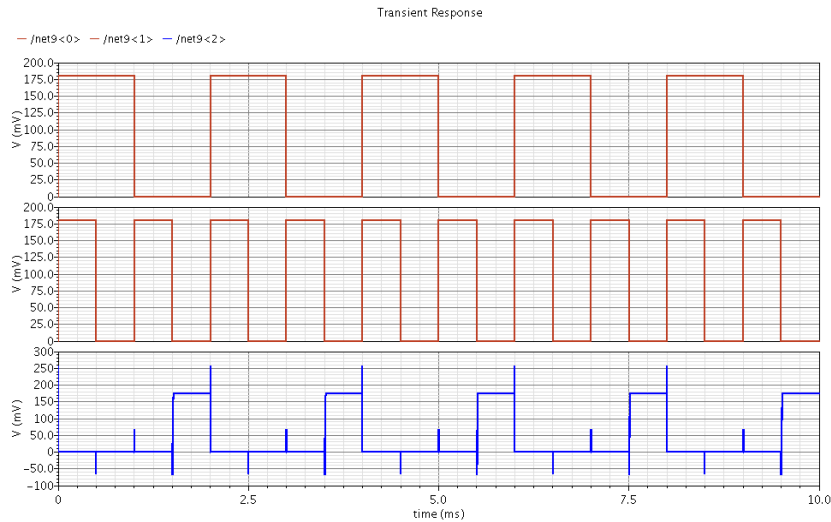


Fig 3.7: Schematic of NOR Gate.

Fig 3.8: Transient response of NOR Gate for $V_{DD} = 180mV$.

E. X-OR Gate

For designing a sub-threshold XOR logic cell, first we analyse traditional logic at low voltages. When the drives of this gate are lowered to the point that the on currents become comparable with the leakage currents then parallel leakage, stacked transistors, and sneak leakage effects affect functionality during low-voltage operation [4] [5]. Here we will see the methodology to minimize the implication of these effects.

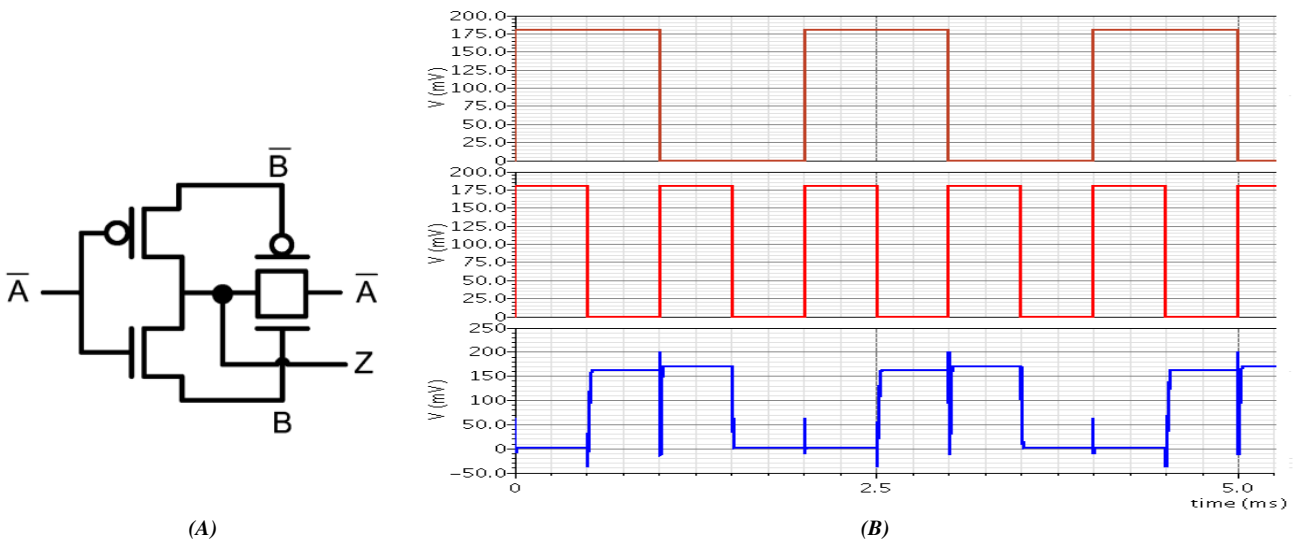


Fig 3.9: (A) Schematic of Tiny X-OR Gate and (B) Transient response of Tiny X-OR Gate for $V_{DD} = 180mV$.

Figure 3.9 shows the schematic and transient response of the tiny XOR gate commonly found in standard cell libraries.

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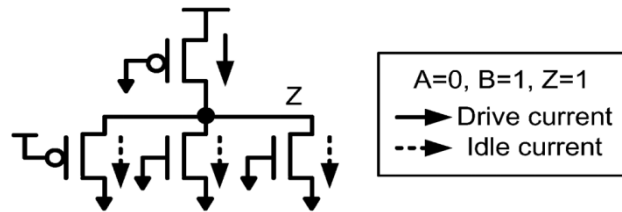


Fig 3.10: Tiny XOR Gate showing the parallel leakage with inputs A=0 and B=1.

Here since multiple devices are connected in parallel to a single circuit node, parallel leakage occurs in some cases. Parallel leakage occurs when the idle current of parallel devices reduces I_{on}/I_{off} . Specifically, several parallel off transistors effectively increase the I_{off} of the gate and degrade the I_{on}/I_{off} ratio. This degraded ratio can impact the functionality of the gate. Figure 3.10 show the case when A=0 and B=1. In this particular case there are 3 ‘off’ devices and only 1 ‘on’ device. This results in degradation of I_{on}/I_{off} ratio [4][5]. That’s why for case (A=0, B=1) output Z = 163mV and for (A=1, B=0) output Z= 170mV.

A transmission gate XOR (Figure 3.11) is a circuit where the number of parallel devices are minimized (or balanced) for minimum voltage operation. Because there are two devices pulling the output node high and two devices pulling low, I_{on}/I_{off} ratio is not degraded and the XOR is fully functional as shown in the simulation.

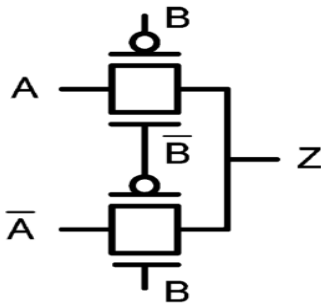


Fig 3.11: schematic of transmission XOR Gate.

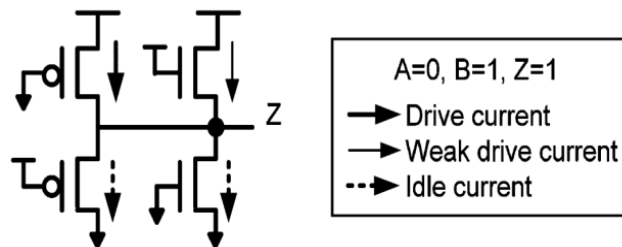


Figure 3.12: Transmission gate XOR Gate under the condition A=0, B=1.

Also, because both NMOS and PMOS are in the pull-up and pull-down path, the effects of process variations are mitigated [4] [5]. The transient response of this transmission gate XOR is as shown in figure 2.19. As can be seen this gives the output Z = 174mV.

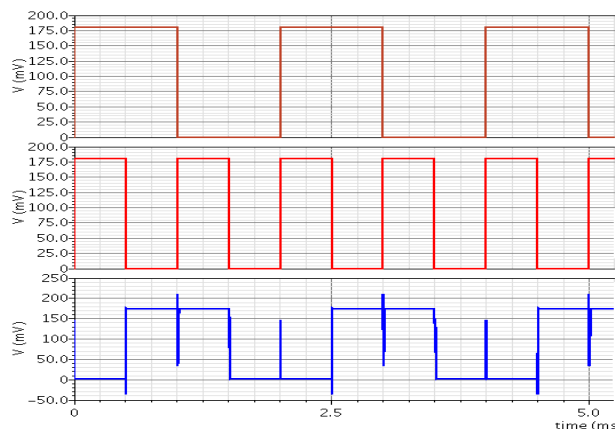


Figure 2.18: Transient response of transmission gate XOR Gate for $V_{DD} = 180$ mV.

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IV. PERFORMANCE COMPARISON

A. POWER

The total power in a CMOS circuit is given by equation:

$$P_{Total} = P_{Static} + P_{Dynamic}$$

$$= \frac{1}{2} C_L V_{DD}^2 \alpha f + I_{SC} V_{DD} + I_{Static} V_{DD}$$

Where C_L is the load capacitance, f is the frequency of operation, I_{SC} is the direct path short circuit current arises when both NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground [6]. α is the activity factor. As can be seen from Equation the total power consists of two major components: dynamic power and leakage power. Both these components reduce in magnitude as the supply voltage reduces.

Figure 4.1 shows the dependence of power dissipation upon supply voltage (V_{DD}) for both sub-threshold as well as super-threshold region.

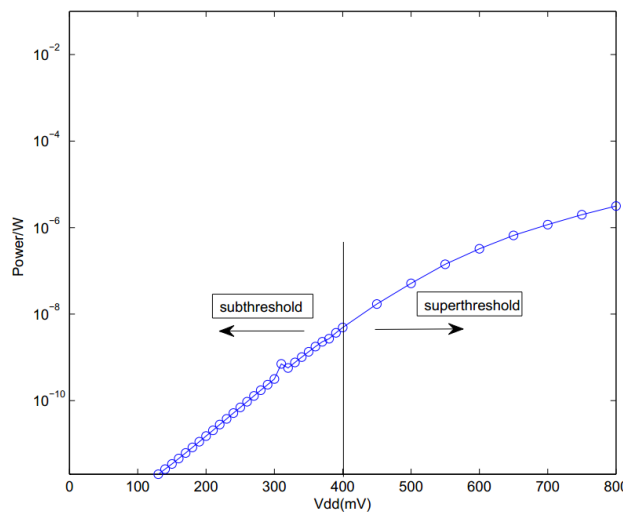


Figure 4.1: Dependence of power on V_{DD} .

B. ENERGY

Energy is one of the important design metrics in digital circuits. The energy estimation in these circuits is given by Equation

$$E_{Total} = E_{Static} + E_{Dynamic}$$

$$= \frac{1}{2} C_L V_{DD}^2 \alpha + I_{Static} V_{DD} t_p$$

Where C_L is the load capacitance, t_p is the circuit delay and α is the activity factor. The important observation in above equation is the dependence of leakage energy on delay t_p . Since t_p is high in sub-threshold, the leakage energy is greater than the dynamic energy. As the supply voltage is increased, the delay and hence the leakage energy, reduces. Therefore, at super-threshold the dynamic energy is the more dominant of the two. Short circuit energy is negligible at sub-threshold and can be ignored [7].

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C. Frequency

To understand the variation in frequency and power characteristics in super-threshold and sub-threshold regions, simulations of a seven-stage ring oscillator using an inverter chain were performed in IBM 65 nm technology node. Figure 4.2 shows the operating frequency dependence upon supply voltage (V_{DD}) scaling.

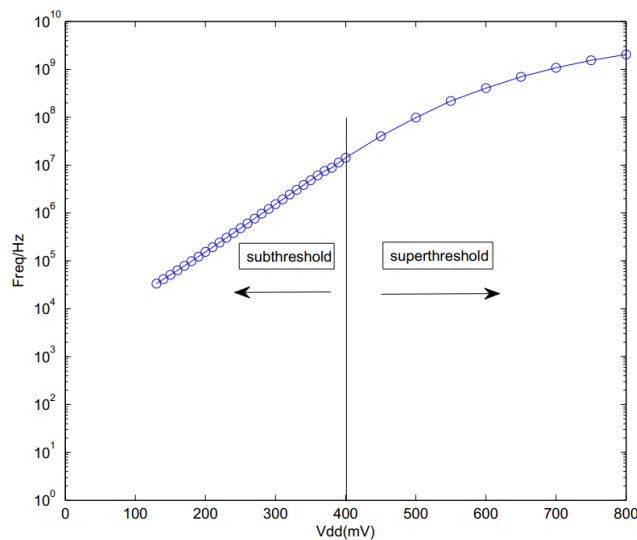


Figure 4.2: Dependence of frequency on V_{DD}

V. RESULT & CONCLUSION

As seen from the equation for the power and energy they are dependent on supply voltage (V_{DD}) as a square function. So scaling the supply voltage will definitely reduce the power as well as energy. By observing the comparison we have seen that this reduction of supply strongly affects the speed of operation of the circuit.

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