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Energy Efficient and High Speed Charge-Pump Phase Locked Loop

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ABSTRACT: This work implements an energy efficient and high speed phase locked loop (PLL) . The main block of PLL is Phase Frequency Detector (PFD), Charge Pump (CP), Low pass filter and a Voltage controlled Oscillator (VCO). The Phase frequency detector used here has been implemented with True Single Phase Clocked logic (TSPC) D flip-flop. This PFD is used to increase the locking performance and to reduce the dead zone. Charge pump is used for the DC-DC conversion. The proposed charge pump avoids charge injection, clock feed through effects and this reduces the ripples in the output. Ring oscillator is used as Voltage Control Oscillator which requires less layout area and has a wide frequency tuning range. Supply voltage of 3V is used and the power dissipated is 11.409 mW. TSMC 0.35- µm technology is used to implement the proposed phase locked loop.

KEYWORDS: Phase locked loop, TSPC, charge pump, charge injection, Ring oscillator.

I. INTRODUCTION

Phase locked loop is a frequency control system which produces output frequency based on the difference between input frequency and feedback frequency. The main blocks of PLL are Phase Frequency Detector (PFD) Charge Pump (CP) , loop filter and Voltage controlled oscillators Fig 1.1 shows the simplified diagram of the phase locked loop.
PLL are widely used in radio, computers, microprocessors for the application including clock recovery, de skewing, clock generation, speed spectrum, clock distribution and frequency synthesis

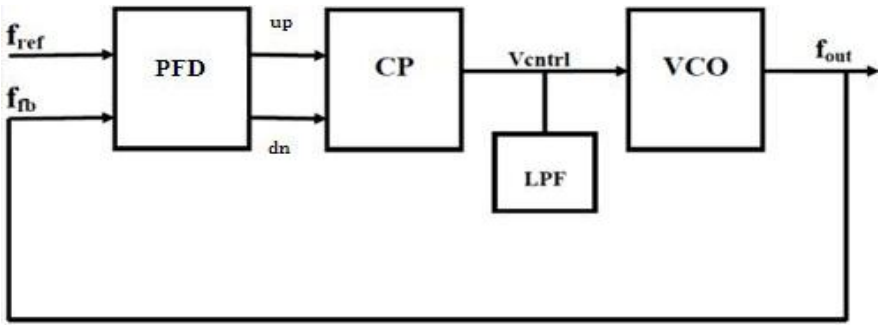

Fig.1.1 PLL Basic Block Diagram

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Phase Frequency Detector measures the difference in phase and frequency between reference & feed back signals. It will produce UP and DDOWN signals. A good phase detector should be free from phase noise and should have the ability to detect lead and lag in the phase and frequency of the input signals [1]

Charge pump consists of current sink, current source and switching circuits. If error signal from PFD is an UP signal, then the CP pumps charge onto the low pass filter capacitor, which increases the control voltage to VCO. But if it is a DOWN signal, then the CP removes charge from the low pass filter capacitor, which decreases the control voltage to VCO.

Voltage controlled oscillators produce output frequency in accordance with input voltage. A ring oscillator structure is frequently used as the basis for the VCO design because it does not require any inductor and can be implemented in CMOS technology [3]

II. PHASE FREQUENCY DETECTOR

The circuits used to implement the PFD are shown in Fig.2 and Fig.3. In this design, signal edges are detected by the flip-flops. The flip-flops are capable of providing a high-accuracy detection and performing at a high-frequency operation. The proposed phase/frequency detector uses a NOR gate to reset the flip flops in order to minimize the dead zone. Initially when circuit is at reset and signal on F1 at low state, transistors M1 and M2 are turned on and the drain of M3 is pre-charged to a logic high state. The rising edge of signal at F1 will turn on the transistor M5. Here, transistor M3's drain is pre-charged to a logic high state and the transistor M4 will be in OFF state and hence the transistor M4's drain will be at a logic low state. NOT gate inverts the signal to generate the UP signal. Since both latches produce the inverse of the desired logic outputs, a NOR gate being used instead of a NAND gate [1].

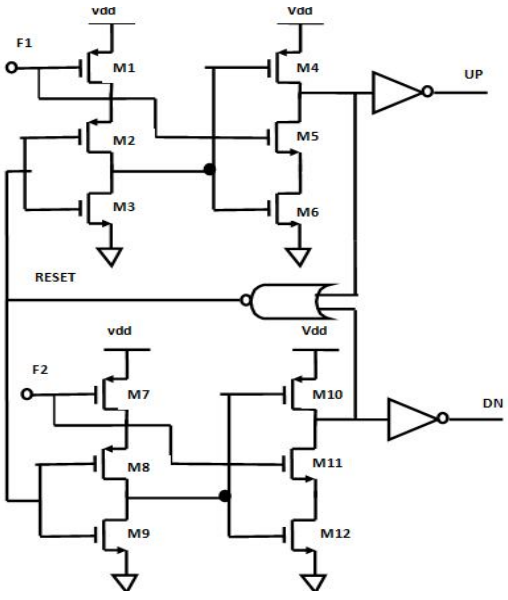

Fig.2.1 PFD circuit with TSPC D flip-flops

In addition, a XNOR and two AND gates are applied to eliminate two output signals being logic high simultaneously. Hence, the short-circuit effects at the charge pump can be avoided [3].

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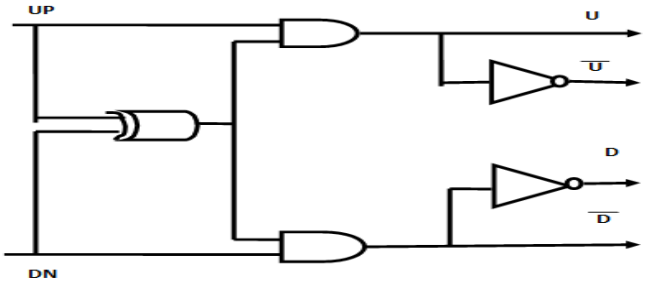

Fig.2.2 Additional circuit to reduce short-circuit

III. CHARGE PUMP

Charge pumps are used to convert the UP and DOWN signal into analog quantities for controlling the voltage controlled oscillators. The CP consists of a current sink, a current source, and the switching networks. The UP/DOWN pulse determine how long the CP will source or sink the current to the loop filter. Charge injection and clock feed through are the major problems while designing a Charge pump. When the current source or sink switches are on, there are charges present under the gate of the transistor. When the switch is turned off, the charge under the gate of transistor will be injected to the drain and the source of the transistor. But when the switch is placed next to the output pin, the injected charges will cause ripple at the output. This is called Charge injection. The clock feed through effect is the clock leakage through the parasitic capacitance of the gate-to-drain capacitance and the gate-to-source capacitance. Fig 3.1 presents a charge pump which avoids all these effects because the placement of the switch away from the output node or to place the switch at the source [5]

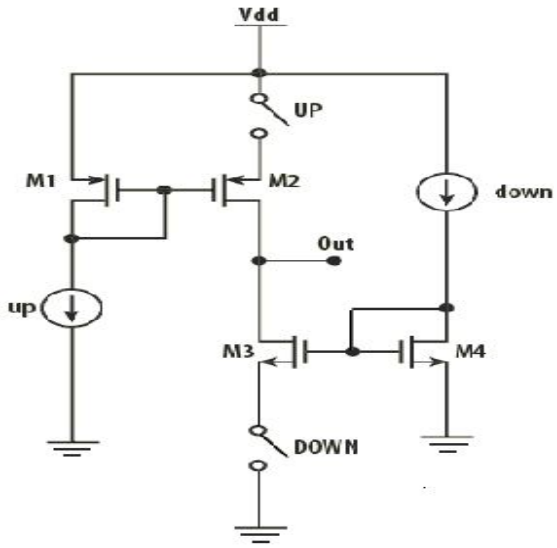

Fig.3.1 Proposed Charge Pump circuit

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IV. RING OSCILLATORS

Ring oscillator can be implemented with odd number of not gates whose output oscillates between two voltage levels. The inverters are attached in a chain structure and the output of the last inverter is feds back into the first. The ring oscillator used in this circuit can be implemented by an odd number of inverters with voltage-controlled delay elements each of which includes a voltage-controlled nMOS transistor and a capacitor [3]

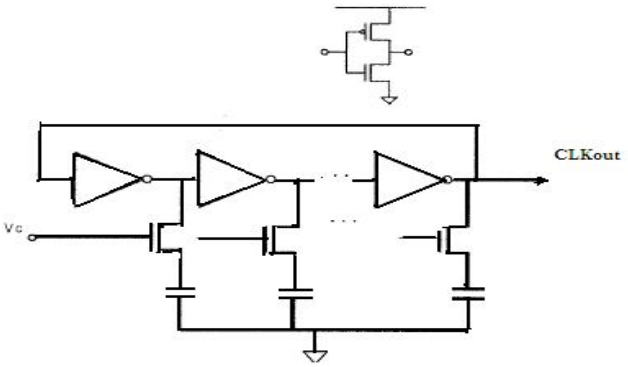

Fig. 4.1 Voltage controlled oscillator

V. IMPLEMENTATION

The Phase Locked Loop circuit has been implemented in Mentor Graphic's Pyxis Custom IC Design Platform. TSMC 0.35-µm technology is used to implement the circuits. Supply voltage is 3 V and power dissipation is 11.4098 mW, which is optimum compared to the other PLL implementations

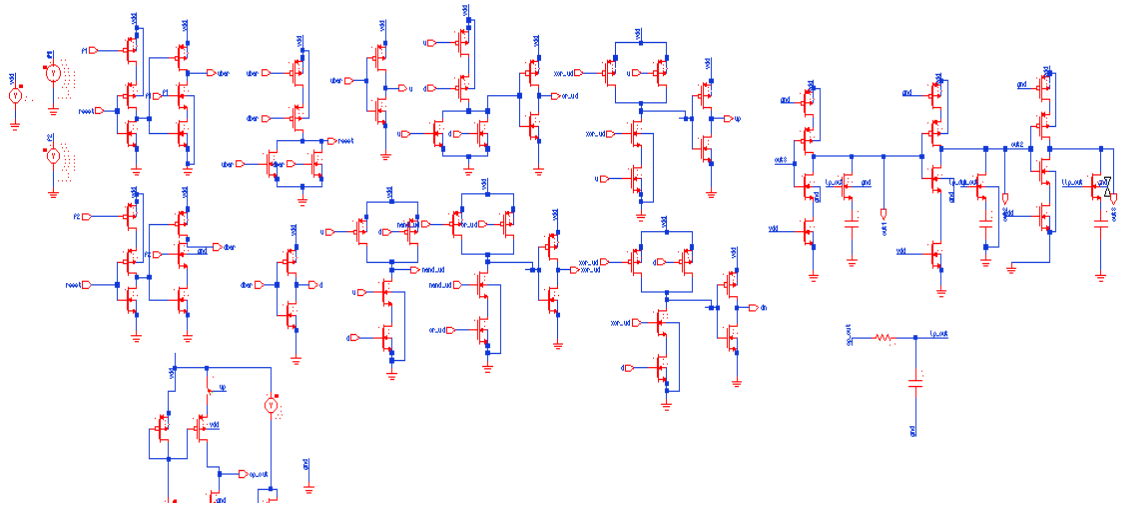

Fig.5.1

Proposed schematic of PFD

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VI. SIMULATION RESULTS

A. *Phase frequency detector*

The UP and DOWN output signals of conventional phase/frequency detector may contain the periodical step and pulse functions which are undesirable. There is a chance for the UP and DOWN signals to go high at the same time. This leads to a short circuit in the charge pump. The output signals of the proposed phase/frequency detector are shown in Fig. 6.1 and Fig 6.2 There are no simultaneous UP and DOWN pulses in both leading and lagging condition, thus the modified circuit prevents a short circuit in the charge pump [1]

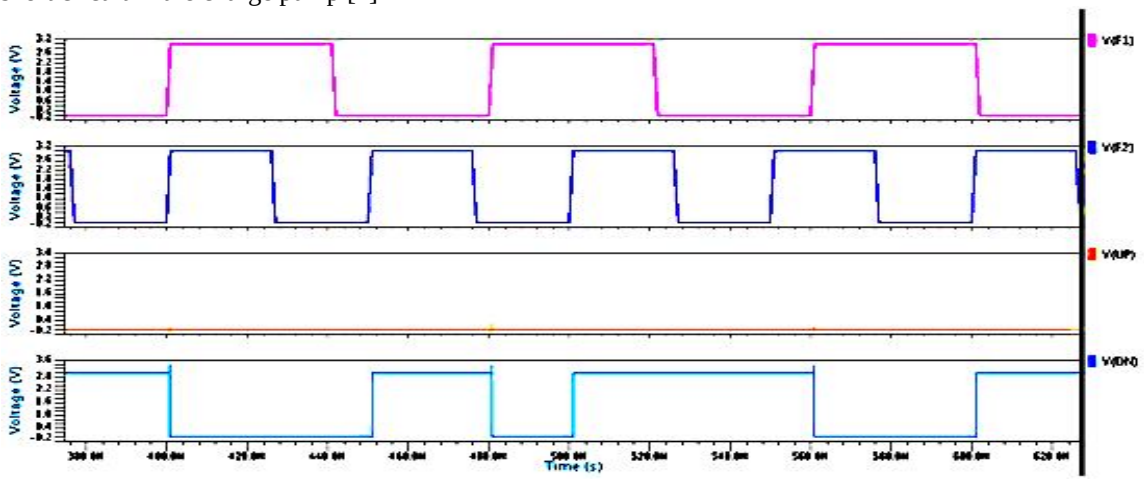

Fig.6.1. Simulated output signals of the proposed phase/frequency detector with DOWN

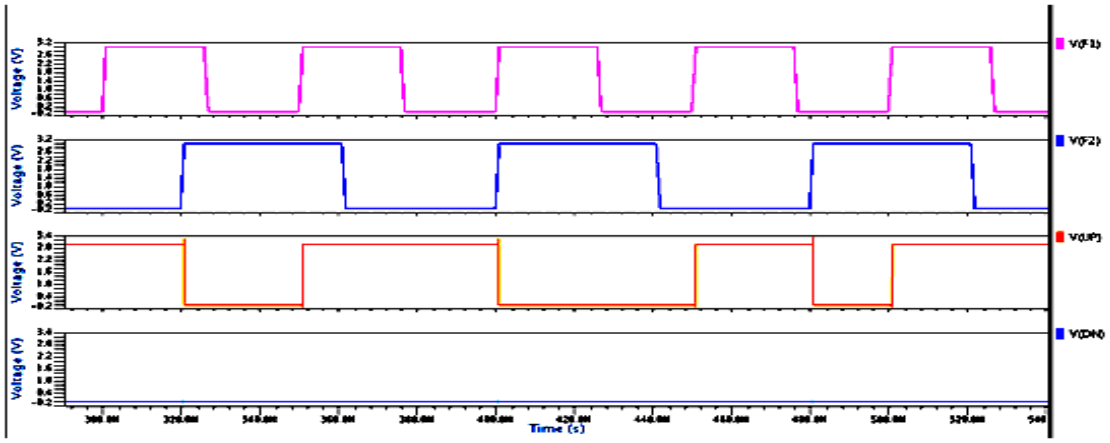

Fig.6.2. Simulated output signals of the proposed phase/frequency detector with UP pulse

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B. charge pump

Figure 6.3 and 6.4 shows that the charge pump yields the output signal without any ripple, thereby stabilising the PLL system relatively easily

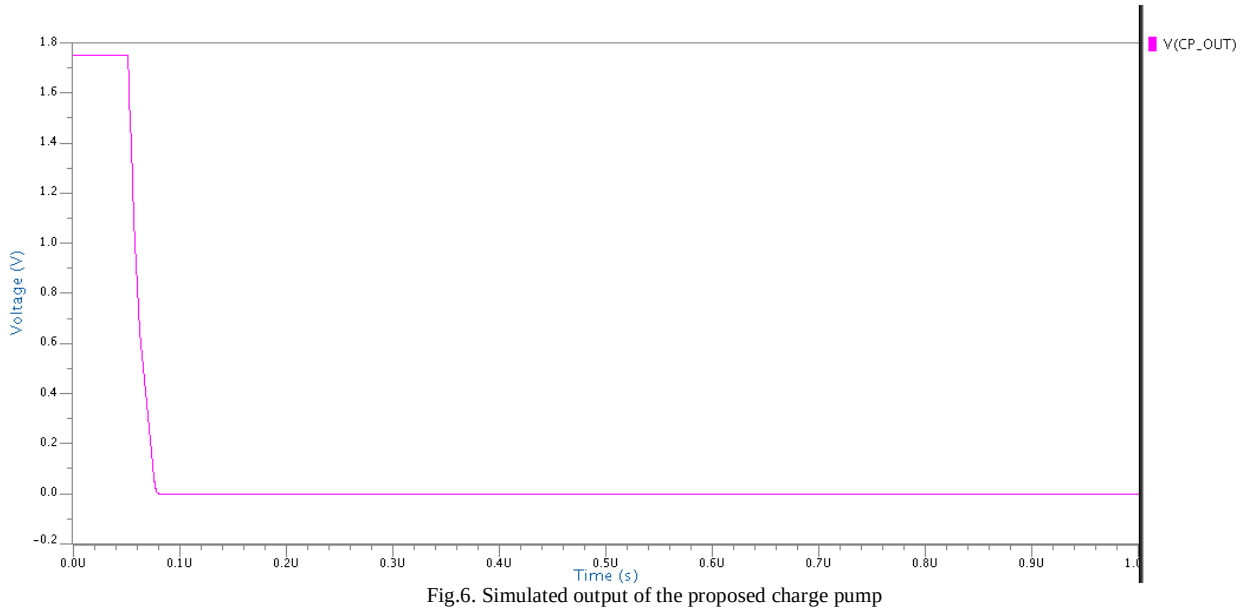

Fig.6. Simulated output of the proposed charge pump

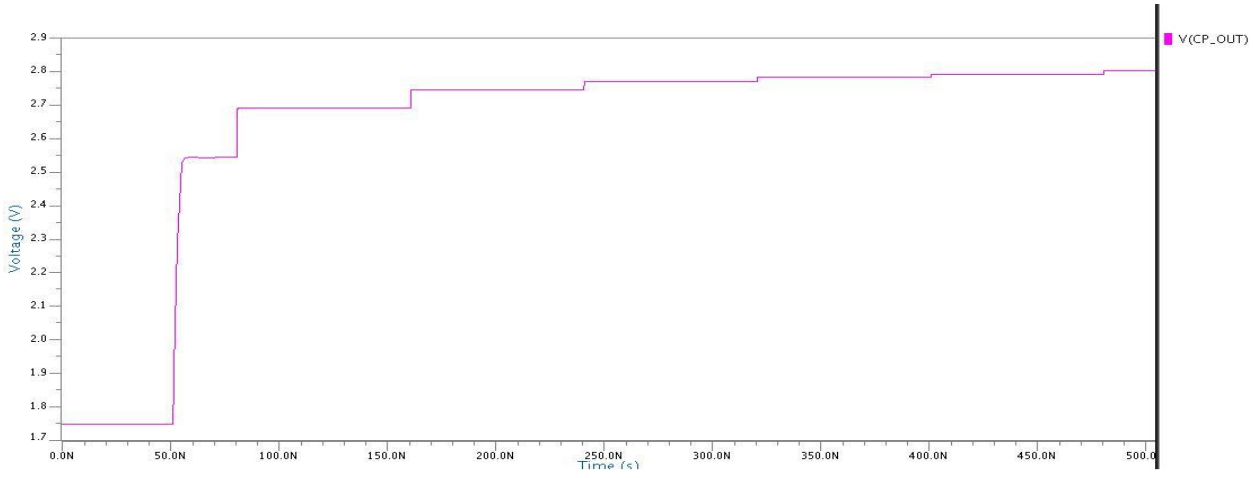

Fig.6.4 Simulated output of the proposed charge pump

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C. *Phase locked loop*

Figure 6.5 shows the simulation results of the Phase locked loop circuit using the proposed phase frequency detector, charge pump and ring oscillator circuits

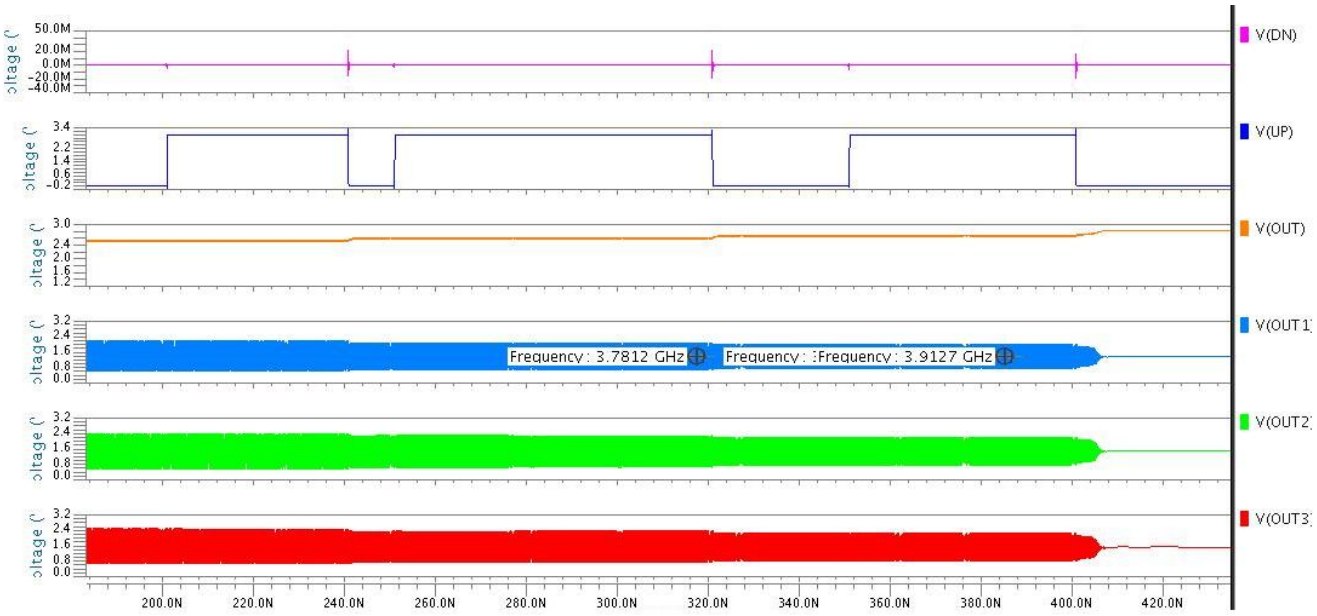

Fig.6.5 Simulated output of the Phase Locked Loop

VII. CONCLUSION

The proposed phase locked loop can operate in GHz frequency range with minimum power dissipation. Therefore it can be used for various industrial applications in a power-efficient manner.

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