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## Low Power and Area Efficient ALU Design

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**ABSTRACT:** Today, the entire device's in electronics needs to be realized with low power and optimized Area architectures because of power consumption and Area are of main consideration along with other performance parameters. Low power consumption helps to reduce heat dissipation, increases battery life and also reliability. Arithmetic and Logic Unit (ALU) is one of the frequent and the most fundamental component in the processor design. In ALU, based on the observation, that if one functional unit is working other functional units remain idle, but they are connected to clock and all units consuming significant amounts of power. By using clock gating technique, a significant amount of power saving can be achieved at high frequencies. The clock gating reduces the power but increases the overall area. Anti symmetric product coding (APC) and odd-multiple storage (OMS) are the techniques that used for area efficient design. This entire architecture captured using VHDL and has to be implemented on FPGA using Xilinx tools.

**KEYWORDS:** APC and OMS, clock gating, Low power, FPGA.

### I.INTRODUCTION

Semiconductor products are composed of electronic circuit arrangements. With the decrease of feature sizes and increase of clock frequencies in integrated digital circuits, power consumption has become a major concern for reliability problem of semiconductor product. In today's world the demand is more functional, energy efficient and optimized power devices. With modern day computers becoming faster and faster and by extension consuming more and more power there is a drive to design new computers with lower power consumption. To develop low power processor, low power ALU is developed since ALU is a basic integral part of any processor. Clock power is a major component of microprocessor power mainly because the clock is fed to most of the circuit blocks in the processor, and the clock switches every cycle. Thus the total clock power is a substantial component of total microprocessor power dissipation. Most of the power dissipation is of the dynamic type which necessities the reduction in switching power dissipation. Fig 1 shows the power distribution among different units of a recent high-performance CPU. The clock is the largest power consuming component which includes clock generator, clock drivers, clock distribution tree, latches, and clock loading due to all the clocked elements. Out of these, clock loading shares bulk amount of power. The main effect of power dissipation is the heat dissipated by the device. The increase in temperature results in decrease in life time of the transistors. This affects the reliability of the devices. .

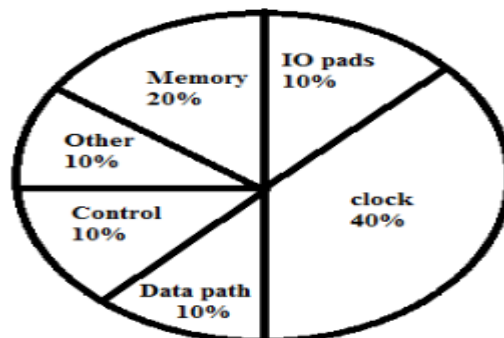


Fig1: Processor Power Distribution

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In the earlier designs, the designers thought that the clock signal is a clean signal and should not be disabled. But it is one of the major sources for power dissipation because clock signal is feed to most of circuit blocks in the architecture. It leads to unnecessary dynamic power consumption. Large VLSI circuits such as processors [1] contain register files, arithmetic units and control logic. The register file is typically not accessed in each clock cycle. Similarly, in an arbitrary sequential circuit, the values of particular registers need not be updated in every clock cycle. If simple conditions that determine the inaction of particular registers can be determined, then power reduction can be obtained by gating the clocks of these registers. When these conditions are satisfied, the switching activity within the registers is reduced to negligible levels. The same method can be applied to “turn off” or “power down” arithmetic units when these units are not in use in a particular clock cycle. In this architecture a clock gating technique is used such that all the blocks are not operated at the same and a chance to reduce the power consumption of unused block. It increases energy efficiency of target design and fulfill our obligation for green computing. This technique also reduces dynamic current and junction temperature of ALU design. The functionality of proposed architecture is verified using Xilinx and power is analyzed using Xpower power analysis tool.

The arithmetic logic unit is one of the main components inside a microprocessor. It is responsible for performing arithmetic and logic operations such as addition, subtraction, multiplication, increment, and decrement, logical operations, rotate operations, shifting operations. Arithmetic and Logic Units (ALU) also contributes to one of the highest power-density locations on the processor as it is clocked at the highest speed and is kept busy most of the time. Therefore, this strongly motivates energy-efficient ALU designs that satisfy the high-performance requirements, while reducing peak and average power dissipation. In several real time applications for multiplication area to be optimized for less memory occupancy. Here the proposed design includes combination of two multiplication techniques named anti symmetric product coding (APC) and odd multiple storage (OMS).

## II. BACKGROUND WORK

### A. Conventional ALU:

The existing method includes a simple Arithmetic and Logic Unit design with different arithmetic and logic operations. The existing basic design consists of a conventional type of arithmetic and logic circuits that perform various arithmetic and logic operations which are required shown in Fig2. Here clock signal can be applied to the ALU directly along with the input signal.

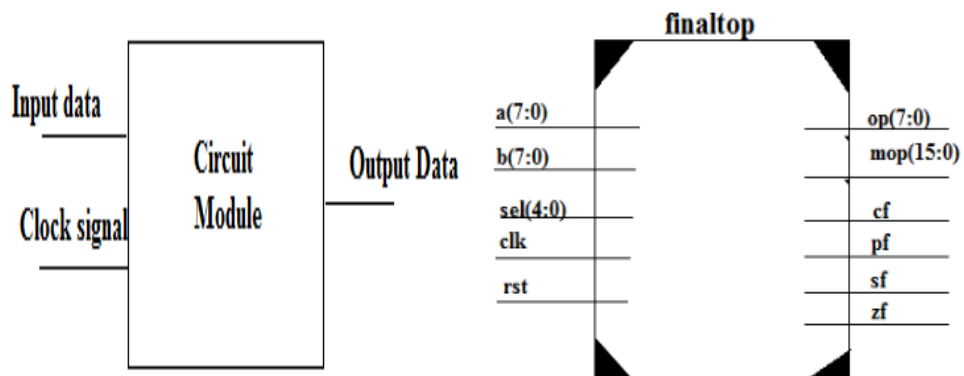


Fig2: Circuit module without clock gating technique

Fig3: Conventional ALU

When the architecture is simulated, it is found to consume more power and it is the main disadvantage of the existing systems. The Fig 3 indicates the top level diagram for the 8 bit ALU. Here a, b, sel are the three input signals and clock is fourth input as shown in Figure. Op, mop returns the result of the ALU operation. Input Sel line determines which

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operation is performed. The ALU generates four flags-Zero (Z), Carry (C), Sign (S), and Parity (P). In ALU, the power calculation showed in Table I when the device is operating at different frequencies, without applying clock gating.

Table I: Power consumption of ALU without clock gating.

Frequency	Clock(W)	Logic(W)	IO(W)	Signal(W)
100 MHz	0.01093	0.00321	0.01558	0.00448
500 MHz	0.05466	0.01605	0.07805	0.02242
1000MHz	0.10932	0.01605	0.04446	0.04446
10GHz	1.09319	0.08982	1.22533	0.22533

### B. Clock gating:

Several techniques to reduce the power consumption have been developed, of which clock gating is predominant. It is the most popular method for power reduction of clock signals and functional units. Clock signals are synchronizing signals that provide timing references for computation and communication in synchronous digital systems. The clock gating techniques [2][3][4] have been developed to avoid unnecessary power consumptions, The basic principle behind this power optimization technique is if the clock signal is gated with the enable signal, if both the signals are active then only the output will come otherwise not. So whenever the output of the particular operation is not needed, unwanted switching activities will be suppressed and hence the power reduces. So Clock-gating is a technique where the clock signal is prevented from reaching the various modules of the ALU. Here enable signal acts as the control signal which is shown in figures 4 and 5. But Clock gating does not come for free.

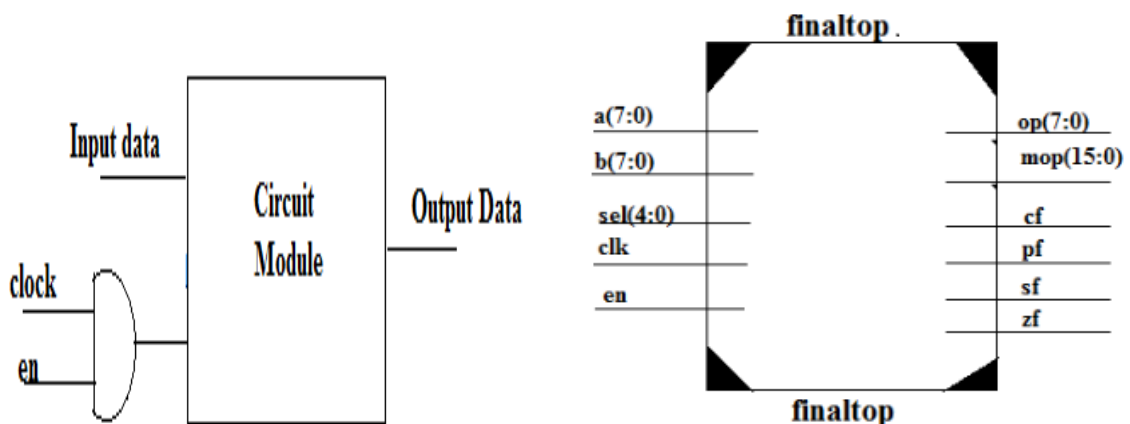


Fig4: Circuit module with Clock gating technique

Fig5:ALU with Clock gating

Clock gating is achieved by ANDing the clock signal with a control signal to form a gated clock, which is then applied to different components of the circuit. To which module the gated clock should be applied is decided based on the control signal. Hence based on the enable signal and clock, if both the signals active then only particular operation will be done and the other operations remain idle. The enable signal is controlled by the selection control in the present design. This is shown that the clock-gating technique help in reducing the power consumption of the ALU, this

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technique i.e clock gating help in reducing the power greatly at high frequencies. Extra logic and interconnects are required to generate the clock enabling signals, and the resulting area overhead must be considered. After implementation of clock gating technique in ALU, the power calculation shown in below table II when the device is operating at different frequencies.

Table II: Power consumption of ALU with clock gating

Frequency	Clock(W)	Logic(W)	IO(W)	Signal(W)
<b>100 MHz</b>	0.01077	0.00295	0.01598	0.00397
<b>500 MHz</b>	0.05385	0.01476	0.07605	0.01983
<b>1 GHz</b>	0.10771	0.02929	0.15051	0.03943
<b>10 GHz</b>	0.07707	0.08269	0.57343	0.21024

The following Fig 6, 7 shows the graphical representation of the power calculation of ALU with and without the clock Gating. The power calculation includes the clock power, logic power, input output power and signal power. The power calculations are taken by the help of the power analyzer tool, by applying different clock frequencies.

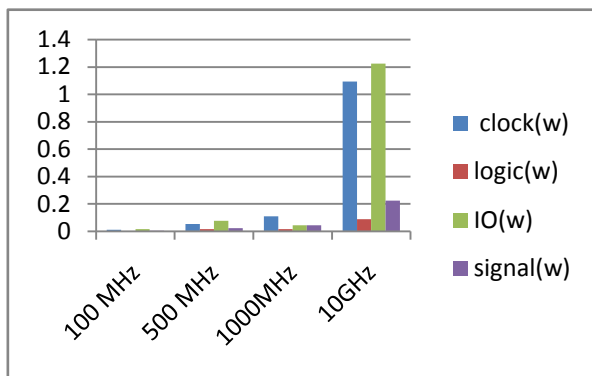


Fig6: Power consumption without Clock gate

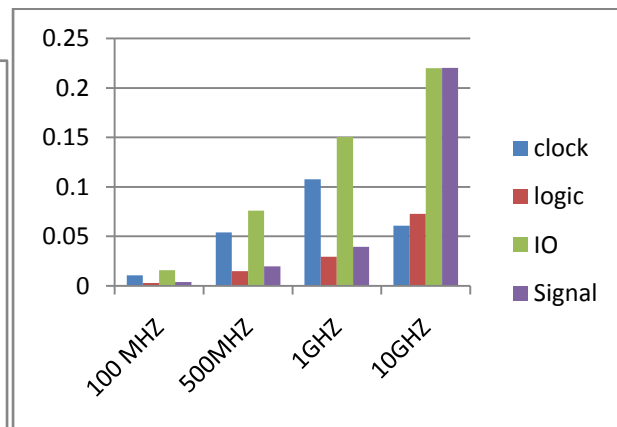


Fig7: Power consumption with Clock gating

### C.ALU Temperature analysis:

There is no change on Effective TJA(C/W) when we varying the device operating frequency. It is independent of clock gating techniques. Junction Temperature is directly proportional to frequency. It is shown that the junction temperature of the ALU is reduced when applying clock gating. So it may be concluded that the clock gating technique can be suitable to the heat efficient designs. The following Table III gives the junction temperature readings of ALU with and without clock gating. The following graph the gives the junction temperature comparisons of ALU which is shown in fig 8.

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Table III: Temperature analysis.

Frequency	Junction temperature Without Clock gating.	Junction temperature With Clock gating.
100MHZ	55.4	54.8
500MHZ	55.7	55.0
1GHZ	56.0	55.2
10GHZ	61.1	59.0

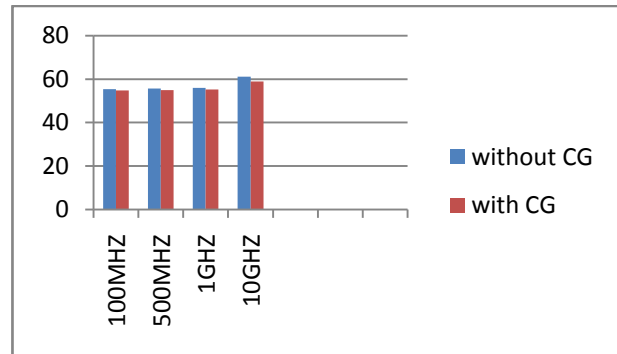


Fig8: ALU temperature with and without clock gating

### D.ALU device utilization summary:

The following table IV describes the device utilization summary of ALU with and without clock gating.

Table IV: Device utilization summary

	Used without clock gate	Used with clock gate	Total available
slices	80	82	301448
Slices flip flops	80	82	301448
4 input LUT	192	234	150720
Bonded IOB	41	51	600

## III.PROPOSED WORK

Clock gating technique saves power but increases over all area of the Architecture of the ALU. In order to obtain the optimized power and area of the ALU design a combined approach of APC and OMS technique is used for the lookup table optimization for the multiplier design because the multiplier is the most power consuming and more area occupied part in the ALU design. Comparing to traditional direct arithmetic, Distributed Arithmetic will save considerable hardware resources by using LUT. A conventional look-up table[5] based multiplier is shown in Fig 9, where A is a fixed coefficient, and X is an input word to be multiplied with A. Assuming X to be positive binary number of word length L, there can be  $2^L$  possible values of X, and accordingly, there can be  $2^L$  values of product  $C = A.X$ . therefore, for memory-based multiplication, an LUT of  $2^L$  words, consisting of pre computed product values corresponding to all possible values of values of X, is conventionally used. The main objective is to propose a new scheme for optimization of LUT with lower area and time overhead.

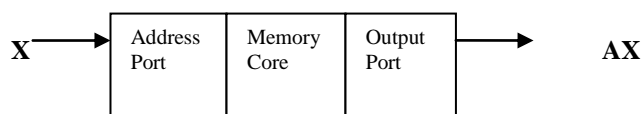


Fig 9: Conventional LUT-based Multiplier

In the new approach of look up table design, only the odd multiples of the fixed coefficient are required to be stored, which we have referred to as the odd-multiple-storage (OMS) scheme. In addition, it is also shown that, by the Anti symmetric product coding (APC) approach, the product words are recoded as anti-symmetric pairs. This multiplier uses

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four blocks. The first block converts the given input to address d0d1d2d3, which is produced by combining both the APC and OMS method. The second block converts the address d0d1d2d3 to LUT address. The third block is a stored LUT and fourth block converts the LUT output to the desired output which is shown in the Fig 10.

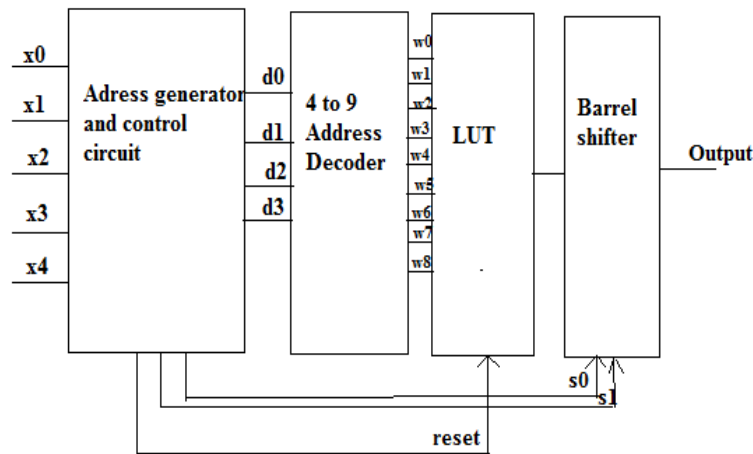


Fig10: APC-OMS combined design for multiplication of W-bit fixed coefficients

### A. APC and OMS device utilization summary

The following table V shows that by using the combined Anti Symmetric Product Coding (APC) and odd Multiple Storage (OMS) with the clock gating technique an optimized power and Area can be achieved in the ALU design.

Table V: Proposed APC and OMS Device utilization summary.

	APC &OMS	Total available
<b>slices</b>	74	301448
<b>Slices flip flops</b>	74	301448
<b>4 input LUT</b>	181	125720

## IV.CONCLUSION

Thus the power consumption is optimized in the modified design using the clock gating technique and it is found to be efficient. With the conventional type of arithmetic and logic unit that executes all the operations at the same time, the power dissipation gets uncontrolled. Hence to discover an alternative, this clock gating logic was taken as a base, the performance analysis clearly shows that the arithmetic and logic unit designed using clock gating logic helping to obtain a near optimum power for arithmetic and logic circuit. But there is the problem of Area overhead. To optimize this problem the combined approach of APC and OMS technique is for optimum area. The proposed approach be achieves a near optimum area for arithmetic and logic unit. Hence the proposed Arithmetic and Logic Unit design can be used in various other low power and area applications.

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