

Design and Analysis of Low Power VCO Based ADC for Ultrasonic Applications

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ABSTRACT: This work presents the concepts of a low power time based ADC. The time based ADC is a new architecture which uses frequency to digital conversion concept. A multi-phase ring oscillator is adopted in order to increase time resolution. The resolution of time based ADCs depends on time and hence, they are highly accurate. The ADC is designed with an input signal band width of 500 KHz and sampling frequency of 50MHz in UMC 180 nm CMOS technology with a supply voltage of 1.8V. The simulation results shows the proposed architecture achieves 10bit resolution with low power dissipation of 1.92mW and 62dB SNR.

KEYWORDS: Band width, sampling frequency, Multi-phase ring oscillator, time resolution, Time based ADC

I. INTRODUCTION

Nowadays highly accurate Analog to Digital Converters (ADC) are very important in the field of advanced electronics systems. ADC is a device used to convert analog signal to digital data. ADC is an inevitable component in all equipments which are used for measurements and signal processing. Conventional ADCs are based on analog building blocks in which the input voltage is quantized in voltage domain. Due to technology scaling the supply voltage decreases so data processing in analog domain became more difficult. Lower signal swing and lower SNR are also disadvantages of traditional ADCs [6]. The design of conventional analog ADCs are difficult because of technology scaling [4]. So for a low power and high resolution ADC we can choose another architecture which is based on time domain quantization. Continued innovation in mixed signal circuits leads to a new architecture of ADC. The new architecture is based on Voltage Controlled Oscillator (VCO) and these ADCs are called as time based ADCs.

The resolution of VCO based ADC is depends on time but in conventional ADCs it depends on voltage. It is usually represented in terms of transition time. At 180nm and below technologies the transition time is getting reduced in the order of picoseconds [4]. Thus the resolution will increases with decrease in gate length.

Conventional Single channel ADC architecture is usually a successive approximation (SAR), flash and pipeline structure. SAR is widely used mainly for merits of stable and simple algorithm, whereas its drawback is large input capacitance, mismatch nonidealities between capacitors. Flash is fast, but it consumes a large area and power. Pipeline is popular for its high speed and accuracy, but its bottleneck is the operational amplifier (OPAMP) inside. OPAMP consumes a large amount of power, furthermore the designing difficulty enlarges as technology proceeds and voltage supply lowers.

II. RELATED WORK

Matthias Voelker et al., [1] proposed a technique to linearize the output of ring oscillator. The regularity technique uses a feedback loop which controls the current flowing through the ring oscillator to linearize the VCO output. ADC is designed in CMOS 180nm technology with narrow band width input signal and 50MHz over sampling frequency. The Spurious Free Dynamic Range (SFDR) of 83.8dB for a 500K band confirms the improvement of linearization and the design implemented in a die area of .03mm². X. L. Zhang et al., [2] proposed a continuous time (CT) delta Sigma ($\Sigma\Delta$) ADC with a design of 4 bit, 15 stage VCO based quantizer. The total area used by this ADC is 0.4mm². The CT delta sigma ADC has been designed in Standard 0.18um CMOS process. The total power

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consumption and average current usage of the circuit is 17.64mW and 9.8mA respectively. Ruihao Si et al., [3] proposed the time interleaved and VCO based ADC architecture. The time interleaved ADC is designed in CMOS United Microelectronics Corporation (UMC) 180nm technology with an input band width of 1.037GHz. The limitation of this design was less sampling frequency compared with the input signal frequency. Simulation results shows the ADC architecture can achieve 7 bit output resolution at a sampling frequency of 100MHz.

III. TIME BASED ADC

The time based ADC architecture also called VCO based ADC or VCO based quantizer that converts analog input signal $x(t)$ in to digital data $Y[n]$. VCO produces a continuous time based signal whose frequency is directly proportional to the average analog input signal $x_{avg}(t)$. A quantizer that follows the VCO that quantizes the signal on each sampling period and generates the corresponding digital output. Resolution is directly depends on the number of phases of VCO. Hence the drawback of single phase architecture can be rectified by using multiphase VCO based ADC.

There are mainly two types of architectures for VCO based ADCs. Counter based architecture and phase detector based architecture..

A. COUNTER BASED ARCHITECTURE

The ADC architecture using multi-phase VCO is shown in fig.1. In this architecture an N phase voltage controlled ring oscillator together with N number of reset counters and registers are used. The counters counts the rising edges at each phases and all the values added together. The register stores the added value which is the quantized estimate of input signal. Even this architecture also facing many issues like reduced noise shaping property due to counter reset issue, high power consumption and area.

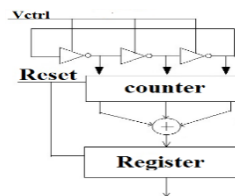


Figure.1 Multiphase VCO-ADC and quant process

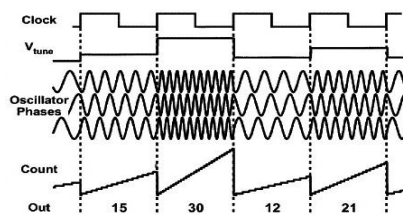


Figure.2 wave forms of counter based architecture

When an output edge occurred at the close proximity of the reset signal the counter fails to count that edge, so it leads to incorrect output or in other words less accuracy. The output wave form of this architecture is shown in fig.2.

B. PHASE DETECTOR BASED ARCHITECTURE

One method used to avoid counter reset problem is to use 1 bit quantizer instead of counter. The counter is replaced with two D flip flops and an XOR gate, these circuits are enough for performing 1 bit quantization in each phases of VCO.

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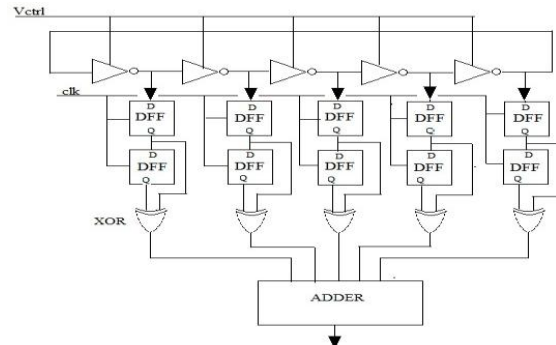


Figure. 3. ADC using 1 bit quantizer

The output of one bit quantizer will be a thermometer code and they summed to get the digital word corresponding to the analog input signal. The ADC using 1 bit quantizer is shown in fig.3, in this circuit the present and previous states of VCO were compared using XOR gate during a sampling interval. If any phase difference is present in the two states the XOR gate will give a logic high output otherwise logic zero.

IV. FIRST ORDER NOISE SHAPING PROPERTY

First order noise shaping is done in all architectures of VCO based ADCs by quantization of phases. By counting the number of rising or falling edges of VCO output and then the phase of output is quantized by either 2π or π . From this the Least Significant Bit (LSB) can be identified as either $2\pi/N$ or π/N for single phase architecture and $2\pi/N$ or π/N for multiphase architecture [5].

The first order noise shaping can be obtained by considering the phase quantization of VCO output. Since a VCO contains multiple stages, the quantization error of the previous state will be the initial phase of a next state. From this the output of the quantizer can be expressed as,

$$y[n] = \frac{N}{2\pi} (\Phi_x[n] + \Phi_e[n-1] - \Phi_e[n]) \quad (1)$$

Where, N: number of phases in VCO, $\Phi_x[n]$: VCO phase change due to analog input signal, $\Phi_e[n-1]$: quantization error of previous phase. By taking Z transform we will get,

$$Y(Z) = \frac{N}{2\pi} [\Phi_x(Z) + (Z-1)^{-1} \Phi_e(Z)] \quad (2)$$

The second term of this equation indicating that the quantization error of the VCO quantizer is first order noise shaped. For a multiphase VCO ADC [3], the resolution formula directly depends on the number of phases (N). So it can be expressed as

$$\text{Resolution} = \log_2 \left(\frac{f_{tune}}{f_{sample}} * N \right) \quad (3)$$

V. CIRCUIT DESIGN

A. VCO DESIGN

A five stage ring oscillator is introduced, the reason are: Ring oscillator has a larger tuning range comparing to LC oscillator [3] and multi-phase output increases the output precision. . In terms of tuning frequency range, SNR and power consumption current starved VCO is a better choice. The circuit diagram of a current starved VCO is given in fig 3. So current starved VCO is chosen for the proposed ADC

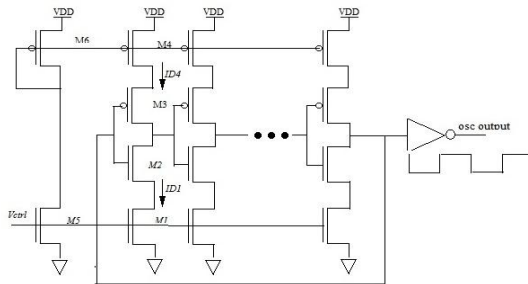


Figure 4. Current starved VCO

The central portion of the circuit is a simple ring oscillator. The MOSFETS M2 and M3 acts as an inverter, while MOSFETS M1 and M4 will act as current limiters to control the current flowing through the ring oscillator part. In other words the M1 and M4 are acting as current sources, they will the current passing through the inverters and this implies that the inverter is starved for current. MOSFET's M5 and M6 operates as a control circuit [7].

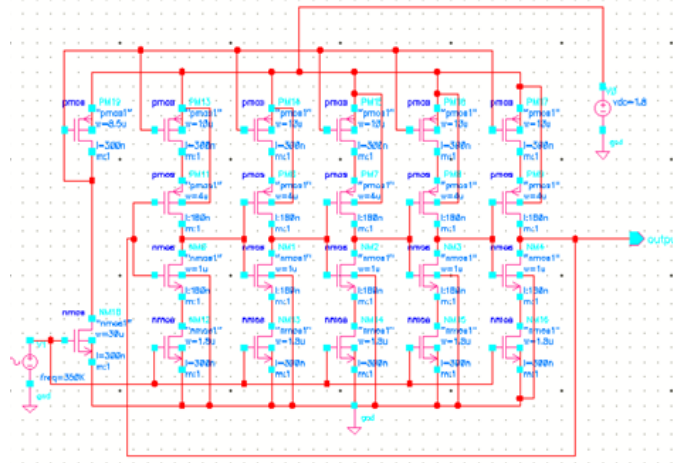


Figure 5. Schematics of Current starved VCO

The current flowing through the transistors M5 and M6 are same and directly depends upon the control voltage applied at the gate of M5. The current in M5 and M6 mirrored to each of the inverter stages. Hence the current flowing through the inverter stages are controlled by the input control voltage [7].

B. QUANTIZER

The most common example of a phase detector is the XOR gate. The XOR gate compares the two input signals and it provides a DC level proportional to the input phase difference [8]. 1 bit quantizer is used in the proposed architecture which mainly contains a phase detector.

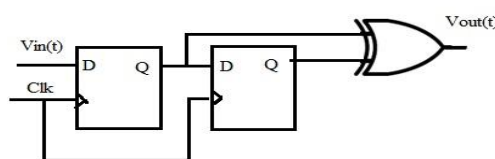


Figure 6. One bit quantizer [12]

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Two DFFs and an XOR gate is operate as phase detector. A 5T TSPC DFF is used in this circuit which is a level triggered DFF. 5T TSPC DFF consumes lesser power and area, compared with other DFF topologies like 9T and 11T TSPC. Standard cells are used in case of XOR gate. The schematics of 5T DFF is shown in fig 7. The schematic shows a 5T TSPC DFF which contains 3 NMOS and 2PMOS transistors. When the clock input is high whatever is the input that will becomes the output. One major advantage of 5T TSPC DFF is reduced area and power.

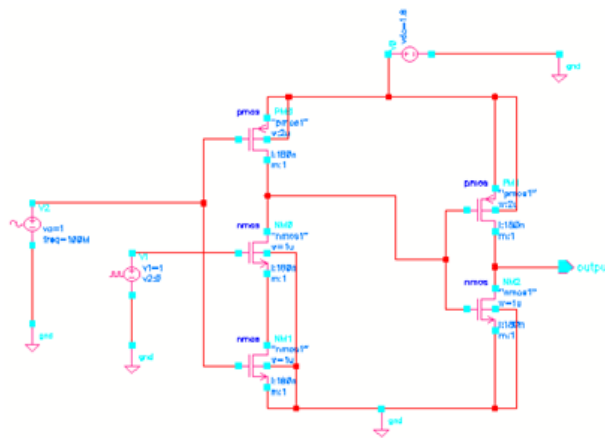


Figure 7. TSPC D Flip-flop

The adder will count number of ones (thermometer codes) at the output of 1bit quantizer. A new concept of adder is used in this ADC architecture, which will count number of ones and gives output in the form of digital data. Since the previous architecture using a lookup table for the conversion of adder output to digital data.

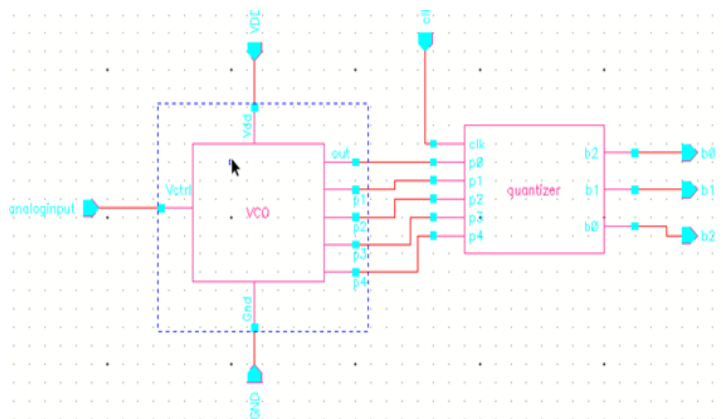


Figure 8. Final ADC block

In the adder designing, an optimization of the critical path is realized. The adder circuit consists of two half adders and two full adders. All the above is done in binary format and stored in a group of registers

VI. SIMULATION RESULTS

The transient response of 5 stage current starved VCO is given below. The outputs from all the 5 stages are shown in fig 9. The average current and power consumption at the min-max frequency range are calculated using the inbuilt calculator in the cadence tool. An input voltage varies from 0.5 V to 1.75 V for the calculation of tuning frequency and average power consumption.

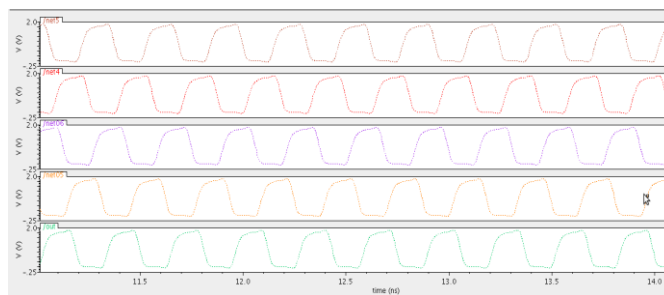


Figure 9. Transient response of a 5 stage VCO

A full scale of 0.75 V Peak-Peak (P-P), 400 MHz input signal is used for the transient response and power analysis is done for the output wave form. Fig 10. Refers to the simulation result of 5T DFF in which the clock signal was 50 MHz sampling frequency.

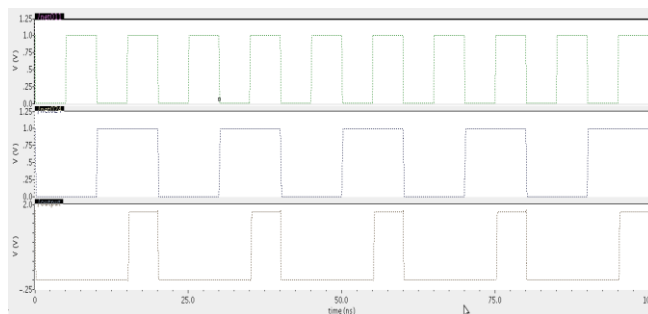


Figure 10. Transient response of D flip flop

At every rising edge of the clock the input is transferred to the output. The number of transistors in this case is less so, it shows reduced area and power consumption compared with DFF used in the previous works [4]. The 5T TSPC DFF delivers only 77.61uW power.

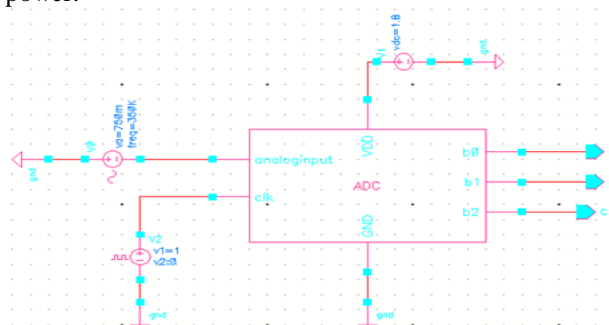


Figure 11. Test bench for the simulation of ADC

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The test bench used for the simulation and analysis of ADC with VCO quantizer is shown in fig 11. A full scale of 0.5V p-p and 400 KHz input signal is used for the transient response and calculation of SNR. The simulation result of the ADC after the integration of all the blocks are given in fig 12.

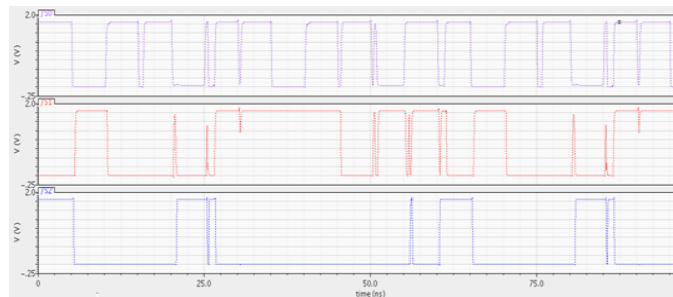


Figure 12. Transient response of VCO-ADC

Power Spectral Density (PSD) of outputs are computed using FFT analysis which is used for the calculation of SNR. Hanning window of size 256 and 65536 number of samples are used for the PSD analysis. The practical SNR is obtained from the PSD graph by taking the difference of power in dB of signal and power in dB of noise floor. The obtained SNR is 61.2 dB which is more compared with other designs [2] [3].

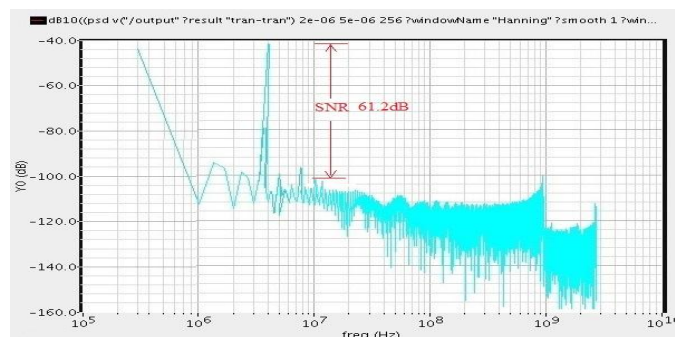


Figure 13. Power Spectral Density plot

VII. CONCLUSION

The time based ADC using multiphase VCO and quantizer is designed and verified in Cadence Virtuoso Analog Design Environment. Based on the simulation results, the various parameters are calculated and compared with the previous works. From the results it can be concluded that the proposed ADC design shows low power consumption and higher SNR value.

The results obtained in this work shows that VCO based ADC is a strong alternative to the traditional ADC because of low power consumption of 1.92 mW with relatively good SNR of 61.2 dB. So the proposed topology can be used to improve the accuracy of tomography and medical imaging techniques.

The ADC input band width is in ultrasonic range therefore, it can be used for ultra-sonic applications. The 5T TSPC DFF designed uses less area as number of transistors used in DFF is reduced to 5. A modified adder circuit introduced in this ADC reduces the circuit complexity.

REFERENCES

- [1] Matthias Voelker, Sara Pashmineh, , Johann Hauer,,MauritsOrtmanns "Current Feedback Linearization Applied to Oscillator Based ADCs" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, vol. 61, pp. 3066-3074, November 2014.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 8, August 2015

- [2] X. L. Zhang, J. Z. Chen, Z. T. Xu, Q. Yu, and Y. Liu* "A VCO Based Continuous Time Delta Sigma ADC with 10MHz BW 55dB SNR and 42dB SNDR" 2012 IEEE.
- [3] Ruihao Si, Fule Li, Chun Zhang "A 100MHz S/s, 7 bit VCO-based ADC which is used in Time Interleaved ADC Architectures", IEEE 2012.
- [4] Jaewook Kim Tae-Kwang Jang, Young-Gyu Yoon, and SeongHwan Cho "Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, vol. 57, pp. 18-13, January 2010.
- [5] Matthew Z. Straayer and Michael H. Perrott, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time $\Sigma\Delta$ ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 43, No. 4, April 2008.
- [6]] Jaewook Kim and Seonghwan Cho, "A Time-Based Analog-to-Digital Converter Using a Multi-Phase Voltage-Controlled Oscillator" IEEE Conference: international symposium on circuits and systems. ISCAS 2006. Pp.3934-3937, May 2006
- [7] R.Jacob Baker, CMOS circuit design, layout, and simulation. Wiley – interscience, second edition 2013.
- [8] BehzadRazavi, "Design of analog CMOS integrated circuits", Tata McGraw-Hill edition 2002.