

A Study on Recent Advancements in VLSI Technology using FinFETs

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ABSTRACT: Scaling is one of the key factor of any new technology and it governs the design metrics of the complete technology. With the scaling up to sub-micro region, single-gate MOSFETs has served the purpose but as designing moves down in ultra sub-micro region, the further scaling of single gate MOSFETs leads to a number of Short Channel Effects which directly affects the various performance criteria and to resolve these effects, Multi-gate MOSFETs are designed and one of the most widely used and efficient is FinFET.

This paper contains the brief description of FinFET, its structure overview, features and some of the latest work that has been carried out using FinFET in ultra sub-micro region i.e. beyond 22nm scale and its comparison with the previous existed technologies.

KEYWORDS: FinFET, Non-planer structure, Digital circuits and memories, Threshold voltage, Fin width.

I. INTRODUCTION

Gordon E. Moore published a paper in 1965 which is considered as the Bible of semi-conductor and Integrated circuits industry. His paper predicted a doubling every year in the number of components per integrated circuit and projected this rate of growth [1] would continue for at least another decade. His prediction proved accurate for several decades, and the Moore's law formed the base in the semiconductor industry to set a path for long-term planning and to set targets for research and development. However, as the process technologies continued to shrink beyond 22 nanometers (nm), it became impossible to achieve a similar scaling of distinct device parameters, particularly the power supply voltage, which is the key factor in determining dynamic power and in view of the difficulties in planar CMOS transistor scaling to preserve an acceptable gate to channel control, FinFET based multi-gate non-planer devices have been proposed as a technology option for replacing the existing technology [2].

The term FinFET was coined by Profs. Chenming Hu, Tsu- Jae King-Liu and Jeffrey Bokor, UC Berkeley researchers to explain a non-planar, double-gate electronic transistor engineered on associate SOI substrate. The distinctive feature of the FinFET is that the conducting channel is wrapped by a slender semiconductor "fin" that forms the body of the device and the fin thickness determines the effective channel length of the device [3].

A FinFET structure has been shown in fig.1 which depicts the gate and channel arrangement between source and drain in FinFETs. A number of materials can be used to form substrate and channel. Here, Indium-phosphate combination has been showed along with Indium-Gallium-Arsenide to form p-type substrate.

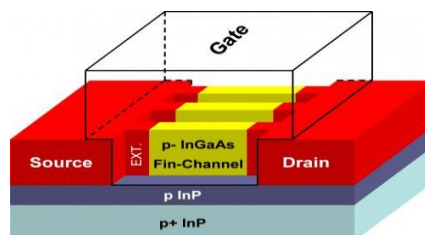


Fig.1 : FinFET structure

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II. FEATURES OF FINFET

FinFETs were introduced to overcome the Short Channel Effects (SCE) and they are having some distinct characters that makes it different from earlier FETs.

- a) **Non-planer Structure** - FinFETs can be fabricated with their channel along different orientations in a single die. Fabrication of planar MOSFET channels along any crystal plane other than $\langle 100 \rangle$ is difficult due to process variations. However, FinFETs can be fabricated along the $\langle 110 \rangle$ plane as well. This results in enhanced hole mobility. $\langle 110 \rangle$ oriented FinFETs can be fabricated by simply rotating the transistor layout by 45° in the plane of a $\langle 100 \rangle$ wafer. Thus, nFinFETs implemented along $\langle 100 \rangle$ and pFinFETs along $\langle 110 \rangle$ lead to faster switching of logic gates since this gives designers an opportunity to utilize the underlying mobility difference between electrons and holes [4].

The way in which the gate surface of nFinFETs and pFinFETs gate can be oriented are shown in fig.2. A number of different orientations are possible which include $\langle 110 \rangle$, $\langle 100 \rangle$, $\langle 111 \rangle$ and others to achieve better mobility for both holes and electrons.

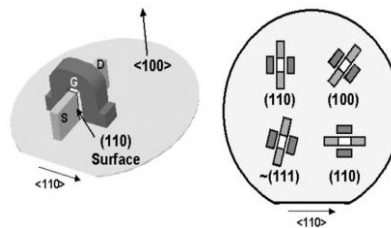


Fig.2: Different channel orientations of FinFET design.

- b) **Effect of Fin thickness and fin height on FinFET-** Fin thickness and its height are the two major parameters used to control drain electric field by lowering the barrier of channel because of reduced source/fin and drain/fin junction capacitances. Sub-threshold slope also increase in thick fin device. The main reason for this is the gate loses its control over the channel. SCEs are mainly depends upon fin thickness. Thinner the fin much better are the chances to overcome SCEs. As the fin thickness is increased, Drain Induced Barrier lowering (DIBL) also increases [5]. If the thickness of the fin was reduced, the off state leakage current was also found to reduce and when the fin height is increased, the potential to drive current also increases. Fin Height is limited by etch technology while Fin Pitch determines layout area and limits S/D implant tilt angle.

Fig.3 gives us a view of flow of current in FinFET along with length of dual-gates, Fin-width and Fin-height. Source and drain in the end of view with dual-gates between them. This figure depicts the way in which gates are formed in FinFETs.

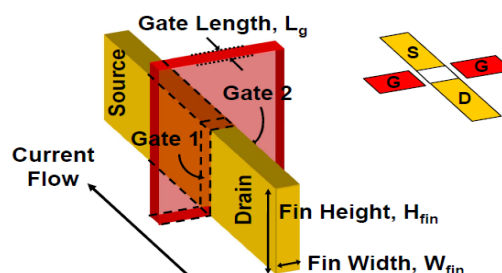


Fig 3: Depiction of Fin Height, Fin Width, Gate Length

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- c) **Vth Controllability** – In FinFET, the Threshold voltage can be controlled by using multiple supply voltages. The V_{th} at each gate of a FinFET can be controlled by applying voltage at the other gate. This method results in the reduction of Sub-threshold leakage because of an increase in the V_{th} of the leaking transistor, while current drive is increased due to the larger gate drive experienced by the active transistor. This explicitly leads to the reduction of dynamic power consumption. Another method to control threshold voltage is via substrate doping [6].
- d) **Parasitic Capacitance**- In digital applications, the main aim is to achieve a lower capacitance and high drive current and the major concern is of Parasitic capacitance. To improve the performance of the device, reduction of parasitic capacitance is very important. This is mainly done by varying the distance between the centers of the two consecutive fin i.e. Fin pitch and the parasitics are calculated for each layout.

III. STUDY OF FINFET BASED CIRCUITS

a) In designing of various basic logic circuits such as XOR-XNOR logic gate, Priority Encoder, Multipliers and others, FinFETs are widely used in the regime below 22nm scale to observe the different design metrics such as propagation delay, power consumption and power dissipation.

- i. FinFET based XOR-XNOR circuit has been designed using FinFET Pass Transistor Logic. The schematic and truth table based on that is given below along with brief description.
Fig.4 shows a pass transistor logic based designing of XOR-XNOR gate. Here, total 10 transistors have been used and along with power supply and ground, connections are made such that the complete circuit will give desired logical outputs.

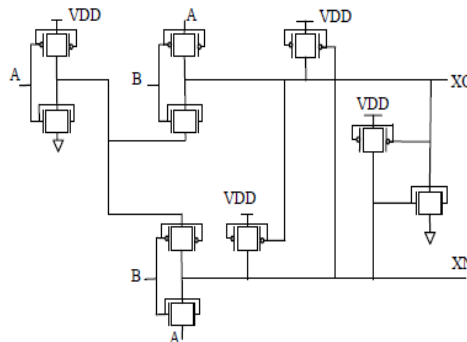


Fig 4 : Schematic of PTL XOR-XNOR

On the basis of fig.4, a truth-table has been formed and showed in Table 1. The four different logic patterns can be implemented using ‘A’ and ‘B’ inputs and on two outputs, one can observe their quality and on that basis a good or bad output can be evaluated.

Table 1: Truth table for XOR-XNOR circuit

A	B	XOR	XNOR
0	0	Good 0	Good 1
0	1	Good 1	Good 0
1	0	Good 1	Bad 0
1	1	Good 0	Good 1

This results in very efficient logic gate having less average power consumption, less number of transistor slices and lesser power-delay product as compared to previous ones [7].

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- ii. A FinFET based 4:3 Priority Encoder had been designed and simulated in 45 nm technology. The design had been observed under a supply voltage than the usual 0.7 V and still results in minimum leakage current, average power and leakage power [8].

Table 2 shows a priority encoder truth table in which based on inputs, output will set high on some desired line according to the priority set by the designer and rest all lines will be don't care. Here, D0-D3 are inputs and X, Y and V are outputs.

Table 2 : Truth table of Priority Encoder

Inputs				Outputs		
D0	D1	D2	D3	X	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

The work which is reviewed here shows that by designing 4:3 priority encoder using FinFET results in around 30% decrease in both average and leakage power as compared to conventional MOSFET circuit [9].

- iii. Single Capacitor DAC based Successive approximation ADC - An ADC has been designed using FinFET Regulated clocked current mirror, a comparator and control logic. The work has shown the advantages which FinFET gives at 45nm scale as compared to 90nm scale where the Short Channel Effects results in lesser efficiency and high power consumption. The main purpose here is to implement the ADC free from SCE. Sampling rate got increased, power dissipation decreased by 15% and relatively higher Ion/Ioff ratio at minimum channel length which enable fast switching between outputs with minimal response time [10].

A Single-switch-capacitor-DAC SAR ADC is shown in fig.5. It consists of a switch control signal section which gets input from a SAR Control Logic block. An Operation amplifier has been used here to give input to Op-amp block whose clock is PWM. The switching has been done by using N-Regulated clocked current mirror (NRCCM) and P-Regulated clocked current mirror (PRCCM).

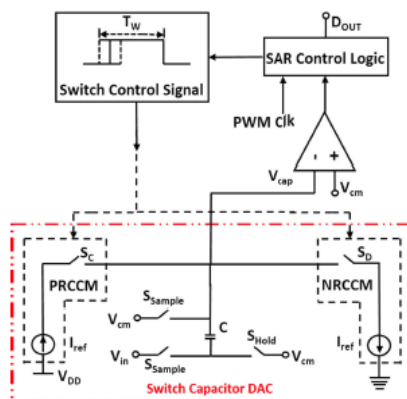


Fig. 5: Single-switch-capacitor-DAC SAR ADC architecture.

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b) FinFET has been extensively used to develop memories with higher capacities and less power consumption. SRAM is the most widely used memory and a lot of work has been done to design SRAM using FINFET. Different designs have been proposed so far and the 6T SRAM is one of the best among them. SRAM with the following characteristic has been the recent one- 0.6V, 1.5GHz, 84Mb design in 14nm FinFET CMOS Technology [11].

A 6 transistor based SRAM cell has been shown below in Fig.6 which consists of a word-line and vertically Bit-lines. Transistor 1 and 2 are directly in contact with word-line and bit-line while other 4 transistors are connected in a manner to act as a storing part.

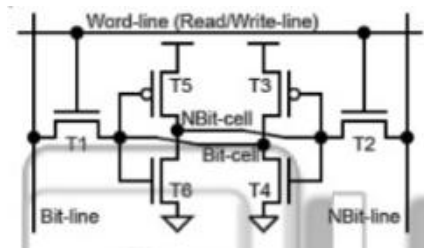


Fig 6 : A 6T SRAM Cell

SRAM mainly requires Trade-off between some important features such as Hold Margin, Read stability Margin, Write Margin, Access time and power consumption.

There are different techniques which one can use to design a SRAM meeting performance requirements.

c) **Impact of Fin Width and Back Bias Under Hot Carrier Injection** – FinFETs have several gates surrounding the channel; therefore, different fin widths (W_{fin}) can show substantially different characteristics. A thinning fin width improves the sub threshold leakage and the SCE of FinFETs and even determines the cut-off frequency. Despite the benefit of thinning width, fin scaling is accompanied by a large reliability degradation under hot carrier degradation [12]. The ultrathin body of FinFETs allows these devices to modulate threshold voltage with the back-gate scheme. The negative voltage on FinFETs allows the circuit to reduce current leakage and power consumption. Meanwhile, a proper circuit design using both forward and reverse voltage can improve leakage reduction. For fully depleted channel MOSFETs, both positive and negative voltages can be implemented with a back-bias generating subsystem for energy efficiency. To achieve this Un-doped n-channel bulk FinFETs employ high-k/metal gate stacks on both sides of a silicon body with an equivalent oxide thickness of around 1nm by atomic layer deposition and SiN on top of the body to eliminate V_t variations [13]. A narrow W_{fin} is close to the quantum width. The double-gate FinFETs with a narrow W_{fin} of 10 nm exhibit a high transconductance (G_m) density but a high drain current degradation and threshold voltage variation under hot carrier injection. This device also exhibits a wide current tuning range but a high hot carrier degradation and threshold voltage variation at a positive back bias. However, this trend can also depend on Si doping concentration.

IV. RECENT ADVANCEMENTS

In Semi-conductor Industries, a lot of research work has been going on in R&D departments considering the vast opportunities in enhancing the FinFET properties. The giants like Intel, Samsung and all others are working on the same technology and trying to scale down as much as they can.

Samsung Electronics Co., Ltd., a world leader in advanced semiconductor solutions, announced the mass production of industry's first mobile application processor using the advanced 14-nanometer (nm) FinFET process technology. They expects the production of 14 nm mobile application processor to positively impact the growth of the mobile industry . As the most advanced technology available today, 14nm FinFET process is able to achieve the highest levels of efficiency, performance and productivity. When compared to Samsung's most advanced previous process technology, this newest process enables up to 20 percent faster speed, 35 percent less power consumption and 30 percent productivity

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gain. By successfully incorporating FinFET structure on transistors, Samsung has overcome performance and scaling limitations of the planar structure used in previous technologies and older processes and gained a significant competitive edge in advanced semiconductors for the mobile industry [14].

For memories, Samsung has been successfully mass producing its proprietary 3D V-NAND products since 2013. Together with its 3D transistor based FinFET process technology, Samsung has strengthened its leadership in 3D semiconductors in both memory and logic semiconductors that addresses the current scaling limitations with planar designs.

Samsung has recently announced the development of S-RAM modules based on 10nm FinFET tech, meaning smaller System-on-Chip (SoCs) with obvious benefits for smartphones.

Samsung's new S-RAM modules will be used for processor cache, and the new 10nm FinFET efforts are apparently 37.5% smaller than 14nm S-RAM. Better performance and lower power draw, which should hopefully mean some nice gains on the battery longevity front. Samsung reckons that it will be ready for mass production of the 10 nm memory modules by 2017.

V . CONCLUSION

This paper gives an insight knowledge of FinFET, its salient features and the way it has revolutionised the semiconductor industry. The brief description of some of the latest work has been done and their future scope is understood. Finally, this can be concluded that a serious research work is going on which will result in efficient, portable, larger memory, even much smaller and faster devices in near future.

REFERENCES

- [1] Moore Gordon E., "Cramming more components onto integrated circuits", Electronics, Volume 38, Number 8, April 19, 1965.
- [2] Yadav Neha, Saurabh Khandelwal, Shyam Akashe, "Design and Analysis of FinFET Pass Transistor Based XOR and XNOR Circuits at 45 nm Technology", International Conference on Control, Computing, Communication and Materials (ICCCCM), 2013.
- [3] Hu Chenming, "FinFET and other New Transistor Technologies", seminar in University Of California, July 2011.
- [4] Gangwa S., S. Mukopadhyay, and K. Roy, "Optimization for surface orientation for High-performance, low-power and robust FinFET SRAM", In Proc. Custom Integrated Circuits Conf., pp. 433–436, September 2006.
- [5] Saini Gaurav, Ashwani K Rana "Physical Scaling Limits of FinFET Structure: A Simulation Study", International Journal of VLSI design & Communication Systems (VLSICS), Vol.2, No.1, March 2011.
- [6] Ramey S., "Tri-gate Transistor Reliability," IPRS Tutorial, 2014.
- [7] Mishra Shiv Shankar, Adarsh Kumar Agrawal and R.K. Nagaria, "A comparative performance analysis of various CMOS design techniques for XOR and XNOR circuits", International Journal on Emerging Technologies, Vol. 1, Issue 1, pp. 1- 10, (2010).
- [8] Huang S.W., Y.J. Chang, "A full parallel priority encoder design used in comparator," Proc. 53rd IEEE International Midwest Symposium on Circuits and Systems, pp. 877-880, 2010.
- [9] Mishra Vishwas, Dr. Shyam Akashe, "Calculation of Average Power, Leakage power, and leakage Current of FinFET based 4-bit Priority Encoder", 2015 Fifth International Conference on Advanced Computing & Communication Technologies, 2015.
- [10] Kushwah R. S. and S. Akashe, "Finfet based tunable analog circuit: Design and analysis at 45 nm technology", Chinese Journal of Engineering, Vol. 2013, No. 165945, 2013.
- [11] Karl Eric, Zheng Guo, James W. Conary, Jeffrey L. Miller, Yong-Gee Ng, Satyanand Nalam, Daeyeon Kim, John Keane, Uddalak Bhattacharya, Kevin Zhang, "A 0.6V 1.5GHz 84Mb SRAM Design in 14nm FinFET CMOS Technology", 2015 IEEE International Solid-State Circuits Conference, 2015.
- [12] Pei G., J. Kedzierski, P. Oldiges, L. Meikei, and E. C.-C. Kan, "FinFET design considerations based on 3-D simulation and analytical modelling," IEEE Trans. Electron Devices, vol. 49, no. 8, pp. 1411–1419, August 2002.
- [13] Chang Wen-Teng, Member, IEEE, Li-Gong Cin, and Wen-Kuan Yeh, Member, IEEE, "Impact of Fin Width and Back Bias Under Hot Carrier Injection on Double-Gate FinFETs", IEEE Transactions on Device and Material Reliability, Vol. 15, No.1, March 2015.
- [14] Samsung Electronics Co., Ltd., "Mass production of industry's first mobile application processor using the advanced 14-nanometer (nm) FinFET process technology", Seoul, Korea, February 16, 2015.