

# Design of a Power Optimal Reversible FIR Filter

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**ABSTRACT:** In present development, the reversible logic design fascinating more attention due to its low power consumption. Reversible logic is very significant in low-power circuit design. The imperative reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, Toffoli gate, and peres gate etc. In this paper, an efficient architecture of FIR filter structure is presented. For achieving low power, reversible logic mode of operation is implemented in the design. It also gives brief idea to build adder circuits using the basic reversible gate like peres gate and TSG gate.

**KEYWORDS:** Low-power VLSI, Low-power CMOS design, reversible logic, quantum cost

## I. INTRODUCTION

Digital filter plays an important role in digital signal processing applications. Digital filters are widely used in digital signal processing applications, such as digital signal filtering, noise filtering, signal frequency analysis, speech and audio compression, biomedical signal processing and image enhancement etc. A digital filter is a system which passes some desired signals more than others to reduce or enhance certain aspects of that signal. It can be used to pass the signals according to the specified frequency pass-band and reject the frequency other than the pass-band specification. The basic filter types can be classified into four categories: low-pass, high-pass, band-pass, and band-stop. On the basis of impulse response, there are two fundamental types of digital filters: Infinite Impulse Response (IIR) filters, and Finite Impulse Response (FIR) filters [1].

Finite Impulse Response digital filter has strictly exact linear phase, relatively easy to design, highly stable, computationally intensive, less sensitive to finite word-length effects, arbitrary amplitude-frequency characteristic and real-time stable signal processing requirements etc. Thus, it is widely used in different digital signal processing applications [1, 2]. FIR filter is described by differential equation. The output signal is a convolution of an input signal and the impulse response of the filter.

$$y(n) = \sum_{k=0}^{N-1} (h(k)x(n - k)) \dots \dots \dots (1)$$

x(n) is the input signal

h(n) is the impulse response of fir filter

The transfer function of a causal FIR filter is obtained by taking the z-transform of impulse response of FIR filter h(n). The delays in operating on prior input samples. The h (k) values are the coefficients used for multiplication, so that the output at time n is the summation of all the delayed samples multiplied by the appropriate coefficients.

$$H(z) = \sum_{k=0}^{N-1} (h(k)Z^{-k}) \dots \dots \dots (2)$$

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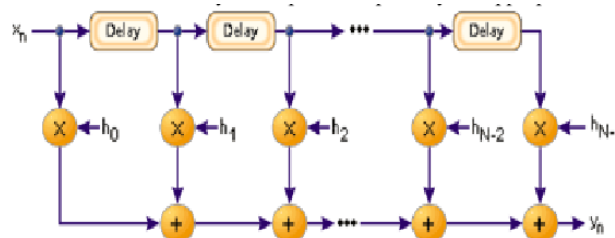


Fig.1 Block diagram of FIR filter

## II. RELATED WORK

FIR filter consists of multipliers, delay element and adders. The various multipliers and adders are described as follows: In this paper various multiplier architectures have designed, during the past few years. In digital signal processors and microprocessors multiplier is one of the key hardware blocks in most of the digital and high performance systems. With the recent advances in technology, more efficient multipliers have routed by many researchers.

### Wallace tree multiplier

To reduces the number of partial products to be added into 2 final intermediate results we use Wallace tree. The basic operation of Wallace tree is multiplication of two unsigned integer, an efficient hardware to implement a digital circuit that multiplies two integers is Wallace tree multiplier. There are three steps in Wallace Tree:

**Partial Product Generation Stage:** The primary step in binary multiplier is Partial product generation. These are the intermediate terms which are generated based on the multiplier value. The first step in binary multiplier is Partial product generation. These are the intermediate terms which are generated based on the multiplier value. In the process of multiplication of two numbers, the main operation is addition of the partial products. Thus, the performance and speed of the multiplier depends on the performance of the adder that forms the core of the multiplier.

**Partial Product Reduction Stage:** To complete the multiplication process we have 5 stages. In each stage we used half adders and full adders that are denoted by the red circle for the 1 bit half adder and the blue circle for the 1-bit full adder. Reduce the partial products by using half adders and full adders that are combined to build a carry-save adder (CSA) until there were just two rows of partial products left.

**Partial Product Addition Stage:** We use multiple half adders and full adders in these addition stages to sum the products of the multiple bits. In this stage the Wallace multiplier method is using ripple carry adders (RCA) to perform these addition operations.

Three steps used in Wallace method to process the multiplication operation. They are

1. Construction of bit product(s)
2. Exhausting conventional adder, combine all product matrixes to form 2 vectors (carry and sum) outputs in first row.
3. Fast carry-propagate adder, remaining two rows are summed to produce the product.

### DADDA multiplier

Dadda multipliers are derived from parallel multipliers presented by Wallace in [5]. In parallel multiplier we use different types of schemes, DADDA scheme is one of the schemes that fundamentally minimize the number of adder stages required to perform the summation of partial products. This exists succeeded by using full adders and half adders to reduce the number of rows in the matrix, number of bits at each summation stage. While the DADDA multiplication has regular and less complex structure, the process is slower in manner. Further, Wallace tree multiplier is expensive compared to that of DADDA multiplier.

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## III. PROPOSED REVERSIBLE LOGIC BASED DESIGN OF FIR FILTER

The proposed method of low power FIR filter design consists of multipliers, delay elements and adders, realized using reversible logic gates.

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one-to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1\*1 or 2\*2) required to realize the circuit.

### A. Basic Reversible logic gates

**Feynman Gate:** Feynman gate is a 2\*2 one through reversible gate as shown in fig.2. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by  $P=A$ ,  $Q=A \oplus B$ . Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

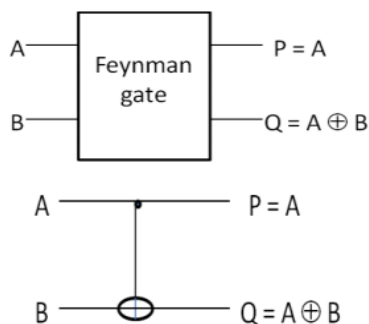


Fig.2: Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 1: Truth table of Feynman gates

**Toffoli Gate:** Fig 3 shows a 3\*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O (P,Q,R). The outputs are defined by  $P=A$ ,  $Q=B$ ,  $R=AB \oplus C$ . Quantum cost of a Toffoli gate is 5

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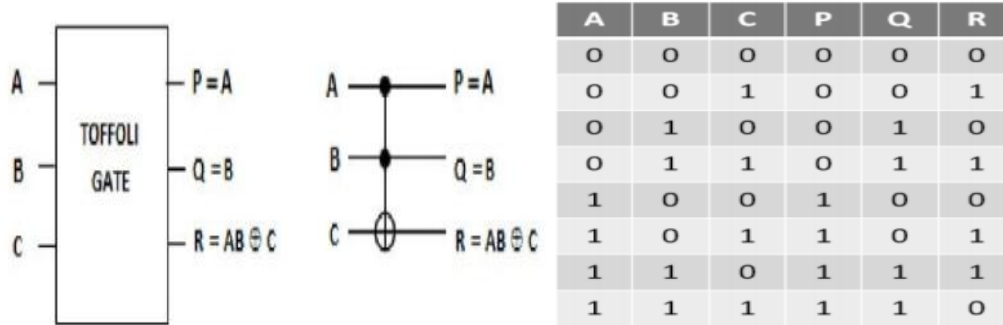


Fig. 3: Toffoli gate Table 2: Truth table of Toffoli gate

**Fredkin Gate:** Fig 4 shows a 3\*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by  $P=A$ ,  $Q=A' B \oplus AC$  and  $R=A' C \oplus AB$ . Quantum cost of a Fredkin gate is 5.

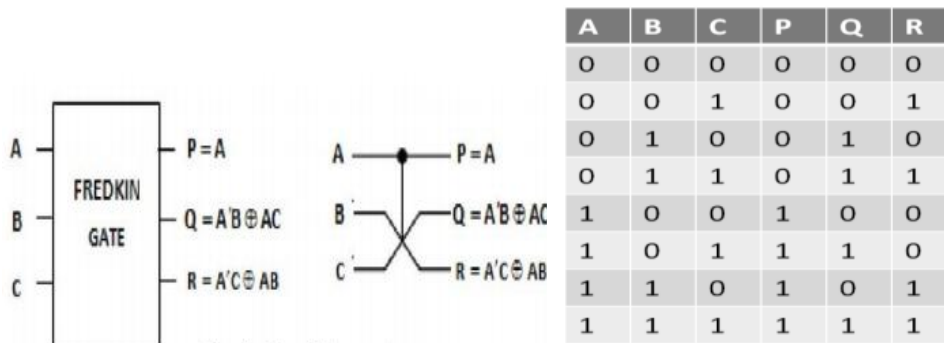


Fig. 4: Fredkin gate

Table 3: Truth table of fredkin gate

**Peres Gate:** Fig 5 shows a 3\*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by  $P = A$ ,  $Q = A \oplus B$  and  $R=AB \oplus C$ . Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

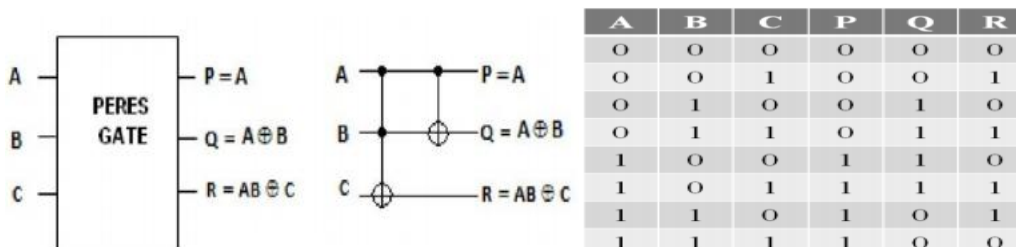


Fig. 5: Peres gate

Table 4: Truth table of peres gate

A full- adder using two Peres gates is as shown in fig 6. The quantum realization of this shows that its quantum cost is 8 two Peres gates are used

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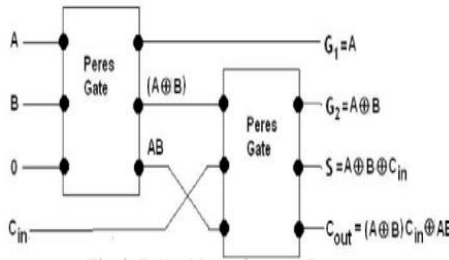


Fig 6: Full adder using two Peres gates

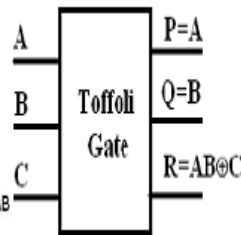
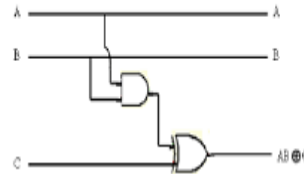


Fig.7: Toffoli Gate



**TOFFOLI Gate:** TOFFOLI gate which is a 3\*3 gate with inputs (A, B, C) and outputs P=A, Q=B, R=AB XOR C. It has Quantum cost five.

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

1. Low power CMOS.
2. Quantum computer.
3. Nanotechnology
4. Optical computing
5. Design of low power arithmetic and data path for digital signal processing (DSP).
6. Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair.

### a. Reversible Multipliers:

The Conventional Wallace tree and dadda multipliers are realized using reversible logic.

**Reversible Wallace multiplier:** For 4 bit multiplication totally there are 3 stages of partial product reduction. If there are p rows of partial products,rows are grouped and the remaining p mod 3 rows are passed to the next stage.

- 1) Rows are summed using fulladders [(3,2) counters] if there are 3 partial products in 1 column and using half adders[ (2,2) counter] if there are 2 partial products in 1 column.
- 2) The resulting sum and carry of the full adder and half adder are passed on to the next stage.
- 3) Finally in the last stage Full adders are used to obtain the product.
- 4) The full adder block is replaced by the Peres full adder.
- 5) Similarly, half adder block is replaced by Peres half adder block. Fig.8 shows the 4x4 reversible Wallace multiplier.

**Reversible Dadda multiplier:**In the Dadda multiplication,[Fig.9] the first stage consists of N2 AND gates, forming the partial products.

The successive reduction levels involve the Peres full adder and Peres half adder blocks leading to the resultant product.

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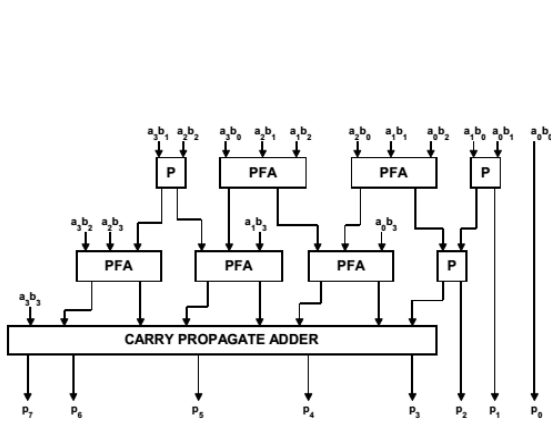


Fig.8 Reversible Wallace multiplier

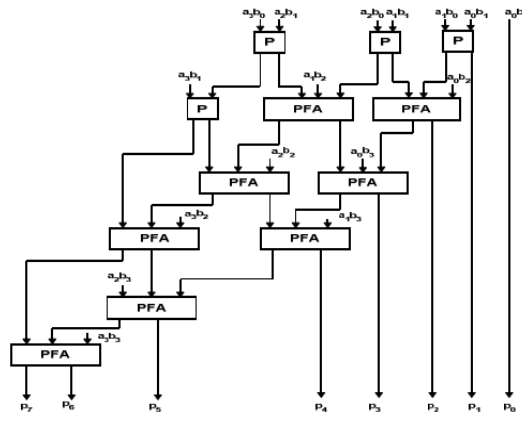


Fig.9 Reversible Dadda multiplier

### b. Reversible Adder:

In the adder blocks, the fulladder is replaced by Peres gate. In CLA, the generate and propagate block is replaced by the Peres gate and Toffoli reversible gates, since addition and multiplication operations are present in the corresponding reversible gates. The Fig.10 shows the generate propagate logic (GPL) realization in Carry look ahead adder. The inputs to the GPL are a, b and c and the outputs are p, q, c1.

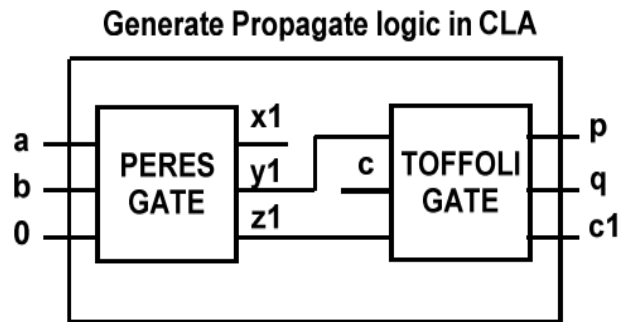


Fig.10 Generate propagate logic in CLA

## IV. DISCUSSIONS

The following are the specifications on the FIR filters employed.

- Input sequence and coefficients are 8-bit data.
- Input sequence are the speech sequences are taken from ITU-T Test Signals for Telecommunication Systems, which includes Artificial voices, real speech and other artificial voices.
- The filter structure follows equiripple characteristics.

## V. CONCLUSION

The reversible circuits form the basic building block of quantum computers. This paper grants the primitive reversible gates which are collected from collected works and this paper aids researches/designers in designing higher complex computing circuits using reversible gates. Also in this paper, low power reversible FIR filter architecture is proposed. In the proposed method the input data samples and filter coefficients are given as input to the multipliers and adders designed using reversible logic gates.

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