

Analysis of Partial-Select Concern Free SRAM with Low Leakage Power

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ABSTRACT: Low-power has been a major concern in all real time application and the memory plays a crucial part in VLSI as it holds the temporary instructions and data needed to complete the tasks. This memory consumes power to a greater extent. For this criterion, a new 8T SRAM design is presented using 0.18 μ m CMOS technology. This SRAM design gives a better performance at V_{DDmin} than the other conventional SRAM cells. Another major problem underwent during write operation in SRAM is Partial-selection of cells. Therefore, an 8 bit SRAM is designed using new PSCF8T SRAM cell which uses new low-power internal write-back scheme. This partial-selection of cells in SRAM array could be addressed by this scheme

KEYWORDS: CMOS(Complementary Metal Oxide Semiconductor), PSCF8T (Partial-Select Concern Free 8T SRAM), SRAM (Static Random Access Memory), Low-Power, Sub-threshold.

I. INTRODUCTION

As power remains to be a major concern in the battery-oriented and electronic devices, it is advisable to reduce it to some extent using CMOS technology. The major role of power consumption is observed in SRAM as it remains to be in idle mode for some time which in turn produces leakage power in the devices. Increment in leakage power is examined with the scaling of device dimensions [1]. Therefore, we reduce the supply voltage of SRAM. The stability of the cell gets declined with the lowering of V_{dd} , hence novel eight transistor cell configuration has been proposed to substitute the conventional 6T SRAM topology for subthreshold purposes [2]. The processor accesses the data which is present in the embedded SRAM. Variability in processes due to diminishing of technology node makes the data access a difficult one. These variations can make memories "UNSTABLE" by losing the stored data. By the progress of CMOS technology, SRAM undergo considerable degradation of cell stability due to the variation in V_{th} of the cell [3]. The combination of both lower V_{dd} and increased process variations lead to memory failures in the design. This challenge could be accomplished using our PSCF8T SRAM cell. Read and write operation in SRAM is performed by only one bit-line of the cell which ensures the optimised result. And both read stability and write ability problem is avoided here. A new solution has been demonstrated to overcome stability problem, improve V_{min} and increase performance for multiport applications by using 8T SRAM arrays. Partial (half)-select takes place when wordline WL of the SRAM is on and the bit-lines are "OFF" leading to poor stability. In our paper, a new low-power write-back scheme is used to overcome the problem of partial selection during write operation in SRAM.

The rest of this paper is organized as follows. Section II depicts the comparison of different SRAM cells. Section III depicts our proposed SRAM design and simulation results. Section IV depicts the solution for half-selection observed in SRAM arrays.

II. COMPARISON OF DIFFERENT SRAM CELLS

Conventional 6T SRAM cell encounters the trouble in sizing of the transistors which is termed as access transistor sizing conflict. These weak access transistors cannot break the feedback loop to force the data into the cell which is referred as poor write-ability. In 9T SRAM cell topology, the two write access transistors are managed by write signal (WR) and the data is stored in the upper sub-circuit memory. The read access transistor and bit-line access

transistor is present in the lower part of the sub-circuit of 9T SRAM cell. Here the read stability of the 9T SRAM cell is improved[4]. But the write-ability of the cell is not maintained. In LP(Low-Power)10T SRAM, there is a series connection of tail transistor which is controlled by the output of the XOR gate[5].The area overhead is reduced by means of the above configuration and there comes a conflict in sizing of tail transistor used in the circuit. In ST(Schmitt-Trigger)10T SRAM, the Schmitt trigger configuration is used to increase or decrease the threshold voltage of the inverter gate. The above ST10T SRAM design provides better noise immunity. Adversely, the power consumption is greater compared to all other SRAM cells.

III. PROPOSED PSCF8T SRAM CELL

Fig. 1 illustrates the circuit design of our proposed PSCF8T SRAM cell, NM0 and NM4 are the write and read access transistors. We, increased the size of the write access transistor (NM0) to acquire write-ability and reduced the size of the read access transistor(NM4) to have better read stability of the cell. The criteria of sizing transistors could not be satisfied using conventional. 6T SRAM cell. In PSCF8T SRAM, the additional pMOS and nMOS transistors (PM0,NM2) will be “OFF” during write operation. Thereby these added transistors suspends VDD and GND connections of the left inverter of PSCF8T SRAM. The right inverter becomes stronger during the write operation and the data is forced into the cell using NM4 access transistor. Meanwhile, the left inverter remains weaker during the write operation.

The bit-line (BLT) which is meant for read operation is precharged to VDD before the read operation starts. Read operation is initiated by making the logic of the RWL higher. The capacitance of BLT gets charged or discharged based on the stored data present at the output node(Q) of the right inverter.

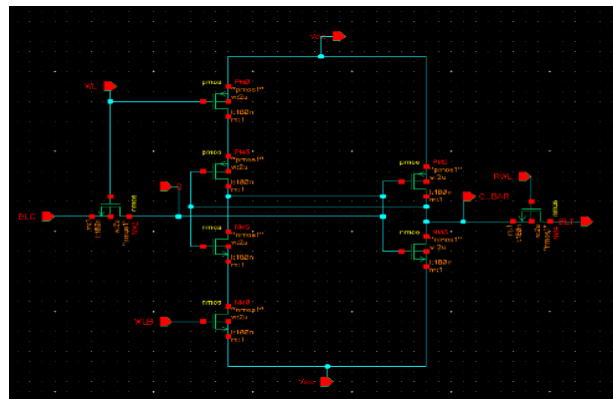


Fig. 1. Partial-Select Concern Free 8T SRAM cell.

The stability of the cell is maintained by having separate access transistors for read and write operation in PSCF8T SRAM[10].

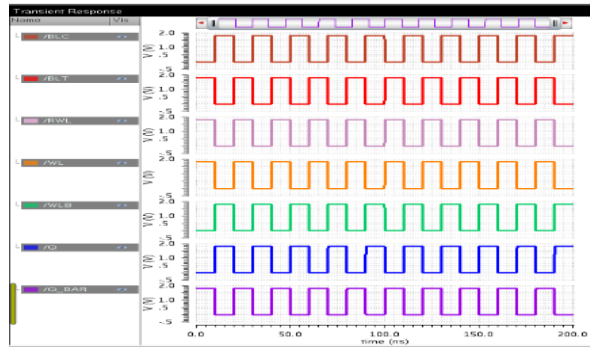


Fig. 2. Transient response of PSCF8T SRAM.

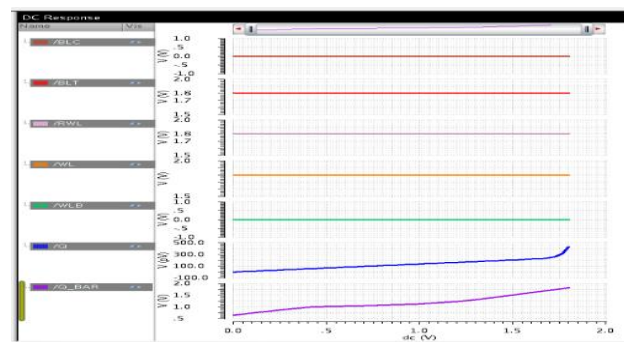


Fig. 3. DC response of PSCF8T SRAM.

The characteristics (DC&Transient) of PSCF8T SRAM is determined for PSCF8T SRAM using 0.18 μ m CMOS technology as shown in Fig.2 and 3. In the transient response graph, Y-axis represents time in nano seconds(ns) and X-axis represents the voltage in volts(V). Here in Fig.2, output node of right inverter Q remains high when the input of it gains a lower value through the bitline BLC. The nodes Q and Qbar have the waveforms contradictory to each other because of the different input voltage given to the bitlines. In the DC response graph, X & Y axis represents the voltage in volts(V). Here in the Fig.3 the waveform of output node Q have a steep increase due to value imposed by the port BLC through write access transistor NM0.This is made clear in the above response graph.

A. Power consumption and delay during read and write operation:

The power consumption for SRAM configurations are found for both read and write operation. The delay during write operation occurs at the time where write word-line WL is affirmed until the internal node voltages of Q and Qbar attains the same value. The delay during read operation takes place at the time where read word-line RWL is affirmed until the voltage difference of about 50mv arise between BLC and BLT. Here the delay during write operation is observed to be greater than other SRAM configurations as our design is “SINGLE-ENDED”.

For read operation, the capacitances formed due to write-drivers (i.e.) WL and WLB are comparatively greater and it has a impact on delay which tends to be smaller than other differential SRAM designs [6]. The values of power consumption and delay for read and write operation are tabulated in table I.

TABLE I. POWER CONSUMPTION OF SRAM CELLS

Configuration	Operation (V _{DD} =1.2V)			
	Read		Write	
	Power(nW)	Delay(ns)	Power(nW)	Delay(ns)
6T	24.71	0.35	6.39	0.43
9T	19.41	0.36	6.56	0.49
LP10T	46.24	0.32	5.461	0.48
ST10T	14.03	0.31	1.99	0.54
PSCF8T	13.44	0.54	2.073	0.40

The values are represented graphically in the Fig.4.

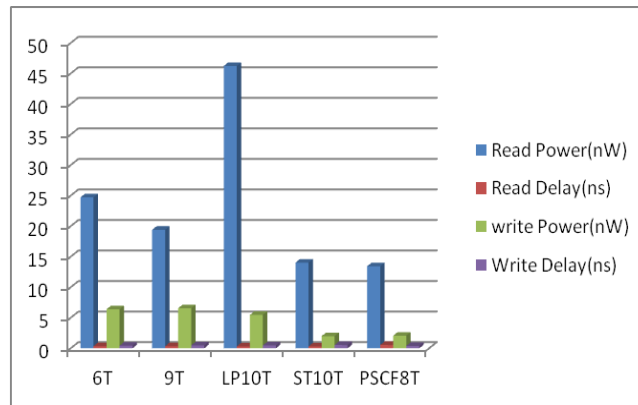


Fig. 4. Graphical representation for power consumption of SRAM cells

B. Leakage power for PSCF8T SRAM:

A SRAM cell remains inactive for a period of time and as a result, leakage power is produced. The leakage power expression is given below:

$$P_{leak} = \sum_{u \in V} I_{sub} * V_{DS} \quad (1)$$

Where I_{sub} is the subthreshold leakage current, V_{DS} is the drain-source voltage.

$$I_{sub} = \mu_0 C_{ox} \frac{W_{eff}}{L_{eff}} \left(\frac{KT}{q}\right)^2 e^{1.8 \frac{q}{nKT} (V_{GS} - V_t)} \left(1 - e^{-\frac{qV_{DS}}{KT}}\right) \quad (2)$$

Here, C_{ox} is the gate oxide capacitance per unit area,
 W_{eff} and L_{eff} are effective channel width and effective channel length,
 μ_0 is the zero bias mobility,
 n is the subthreshold swing co-efficient of the transistor,
 KT is the thermal energy,
 q is the magnitude of electronic charge,
 V_{GS} is the gate-source voltage of the transistor

From the above equation (1) and (2), the leakage power for all SRAM configurations are tabulated below in the Table II.

TABLE II. LEAKAGE POWER FOR DIFFERENT SRAM CELLS

Configuration	Leakage Power(nW)
6T	10.51
9T	10.37
ST10T	11.25
LP10T	8.65
PSCF8T	8.44

The leakage power for our proposed SRAM cell found to have lower value due to heaping effect than other SRAM configurations. Leakage power for ST10T is higher because leakage path becomes twice due to additional nMOS feedback transistors.

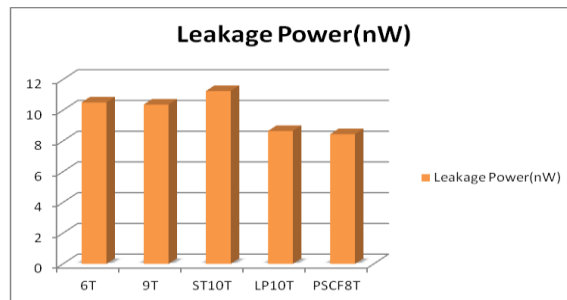


Fig. 5. Graphical representation for leakage power of SRAM cells

The leakage power derived from the above equations (1) and (2) are represented graphically in the fig.5.

IV. PARTIAL SELECT CONCERN FREE 8T SRAM

Here, we have a proposed a new scheme of low power write-back scheme (Fig.6) to overcome the challenge of partial-selection in SRAM arrays. Stability of the cell is not maintained when half-selection occurs[7]. This problem is because of column select remains in "OFF" state when the word line WL is in "ON" state. The data which is present in the selected row are read before write operation in order to prevent losage of data.

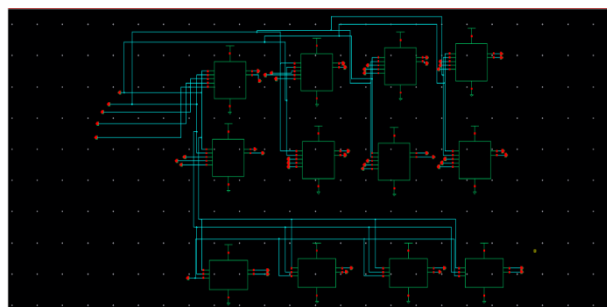


Fig. 6. Proposed partial-select concern-free scheme

Thereby enabling `wb_en` signal and using the inverters at each column, the read data which got inverted are written back on write bitline “WL” as shown in Fig.7.

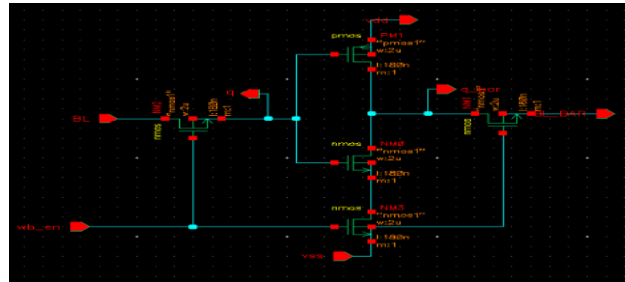


Fig. 7. Partial-selection elimination block.

TABLE III. POWER CONSUMPTION (READ & WRITE) FOR PARTIAL-SELECT CONCERN FREE SCHEME

Configuration	Operation ($V_{DD}=900mV$)	
	Read power(nW)	Write power (nW)
Conv.6T	122.4	343.2
PSCF8T	165.3	390.7

By having additional two nMOS (NM1,NM2), inverters at each column gets eliminated when it is not needed. When inverter remains in idle state, the nMOS transistor (NM3) becomes “OFF” to avoid leakage power [9]. The charging and discharging of capacitive voltage found at the internal nodes is reduced by having only one write-bit line in our proposed design. The partial selection is avoided by ensuring that the write-bitline has internal node voltage. This leads to have a lower power consumption than the previous schemes[8]. By having this architecture, the consecutive write operation observed in microprocessor is reduced upto 80%.The read and write power consumption for PSCF8T and Conv.6T is tabulated below in Table III.

V. CONCLUSION AND FUTURE WORK

In our paper, a new design of PSCF8T SRAM is designed and simulated using 0.18 μ m CMOS technology and it is compared with different SRAM bit cell configurations. At V_{DDmin} , the proposed design proves to have lower power consumption than other SRAM cells. It has the progress of write and read power by 45% and 67% over the conventional one. An 8-bit SRAM is designed to overcome the problem of partial-selection during write operation using low-power write-back scheme with the help of PSCF8T. This proposed cell could be designed using 0.9 μ m CMOS technology to get better optimization in terms of area and power in the future work.

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