

Optimizing Low Leakage SRAM Design Based On Hetero Junction CMOS Technology

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ABSTRACT: SRAM is basically used as data storage elements. In SRAM(Static RAM), during Read operation, Dynamic Noise Margin occurs. During Read operation, Adiabatic Charging occurs in word line which generates DNM. Low voltage performance used to reduce DNM. In proposed method introducing new SRAM architectures, which is smaller than conventional and previous. The most widely used form of primary storage today is a volatile form of random access memory (RAM), meaning that when the computer is shut down, anything contained in RAM is lost. However, most forms of non-volatile memory have limitations that make them unsuitable for use as primary storage. In Existing they were proposed the design Conventional SRAM has 2 pre-charged BL. Single BL SRAM uses only one Bit-Line for read operation. They proposed Single bit line SRAM design because single bit line design has larger Static noise margin than Two-BL SRAM provides high speed, low power. The existing design need reduced size SRAM design. But by shared ports in circuit, leakage occurs. It also consumes power. In their proposed work concentrated to reduce the power consumption and area efficiency. This project propose a design SRAM using CMOS technology. CMOS technology provide less noise ration during design. The proposed SRAM design is based on Hetero junction CMOS technology performs possible data store and restore operations.

KEYWORDS: SRAM, Bit Line, Dynamic Noise Margin.

I. INTRODUCTION

Wireless sensor network technologies are attracting attention in emerging applications, such as industrial monitoring and security surveillance.

The power available to a wireless sensor network is limited because it comes from a battery or super capacitor. Thus, network nodes must have the capabilities of low-power sensing, processing, and communication [1].

One way to reduce the power of an SRAM is to reduce the supply voltage (VDD)[2]. In Existing they were proposed the design Conventional SRAM has 2 pre-charged BL. Single BL SRAM uses only one Bit-Line for read operation. Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy. Hence they proposed Single bit line SRAM design. Our previous study of SNM showed that an SRAM with a single-bit line (BL) had a larger SNM than one with two BLs, and that the BL precharge voltage should be lower than VDD [3]. In this paper, we attempted to adiabatically charge a word line (WL) in a single-BL SRAM to stabilize the flip-flop (FF). Adiabatic charging has been widely investigated [4] and is already being used to charge the cells of plasma display panels [5]. We found that it significantly increased the dynamic noise margin (DNM) for a read operation. Which provides high speed, low power. The existing design need reduced size SRAM design. But by shared ports in circuit, leakage occurs. Which also consumes power. Hence in their proposed work concentrated to reduce the power consumption and area efficiency. Here, we propose a design SRAM using CMOS technology. CMOS technology provide less noise ration during design. The proposed SRAM design is based on Hetero junction CMOS technology. Which performs, possible data store and restore operations.

II. RELATED WORKS

Shunji Nakata, Hiroki Hanazono, Hiroshi Makino, Hiroki Morimura, Masayuki Miyama, and Yoshio Matsuda, "Increase in Read Noise Margin of Single-Bit-Line SRAM Using Adiabatic Change of Word Line Voltage", et

Conventional SRAM has 2 pre-charged BL. Single BL SRAM uses only one Bit-Line for read operation. Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy. Hence they proposed Single bit line SRAM design. The proposed design need reduced size SRAM design. But by shared ports in circuit, leakage occurs. Which also consumes power. [6].

Shunji Nakata, Hirotsugu Suzuki, Hiroshi Makino, Shin'ichiro Mutohl, Masayuki Miyama, and Y oshio Matsudi, "Increasing Static Noise Margin of Single-bit-line SRAM by Lowering Bit-line Voltage during Reading", deals with Single-BL reading is achieved by using a left access transistor and a left shared reading port. We designed the cell layout and confirmed that there is no area penalty for producing two word lines in a memory cell. An analysis of butterfly plots clearly confirms that the single-BL SRAM has the larger static noise margin than the two-BL one. It is confirmed that the static noise margin in the single-BL SRAM is further increased when the BL is precharged to not VDD but to the lower value in the range of $V_{DD}/2$ to $3V_{DD}/4$. In addition, a new sense amplifier circuit without reference voltage is proposed for single-BL reading. We also propose a divided word line architecture for writing to maintain the static noise margin for unwritten blocks.[7]

Keejong Kim, Hamid Mahmoodi, and Kaushik Roy, "A Low-Power SRAM Using Bit-Line Charge-Recycling", In the proposed write scheme, differential voltage swing of a bit-line is obtained by recycled charge from its adjacent bit-line capacitance, instead of the power line. Applying such a charge recycling technique to the bit-line significantly reduces write power. A test chip with 32 Kbits (256 rows x 128 columns) is fabricated and measured in 0.13 μm CMOS to demonstrate operation of the proposed SRAM. Measurement results show 88% reduction in total power during write cycles compared to the conventional SRAM (CON-SRAM) at $V_{DD} = 1.5$ V and $f = 100$ MHz. During discharging have to consider the power dissipation in the SRAM design[8].

Myeong-Eun Hwang, Arijit Raychowdhury, and Kaushik Roy, "Energy-Recovery Techniques to Reduce On-Chip Power Density in Molecular Nanotechnologies", deals with Carbon nanotube has emerged as a promising candidate. However, molecular devices such as carbon nanotube field-effect transistors (CNFETs) with their super-scaled dimensions and high current densities would increase the power density on chip and reasonable predictions estimate that they would far exceed the maximum power density limitation. This paper explores the use of energy-recovery techniques in molecular CNFET based digital circuits and demonstrates how they can alleviate the power density problem in such circuits. Delay cycle and power leakage are considerable[9].

I.G. Baek, D.C. Kim, M. J. Lee, H.-J. Kim, E. K. Yim, M. S. Lee, J. E. Lee, S. E. Ahn, S. Seo, J. H. Lee, J. C. Park, Y. K. Cha, S. O. Park, H. S. Kim, I. K. Yoo, U-In Chung, J. T. Moon and B. I. Ryu, "Multi-layer Cross-point Binary Oxide Resistive Memory (OxRRAM) for Post-NAND Storage Application", et Novel plug contact type bottom electrode (plug-BE) could reduce active memory cell diameter down to 50nm with smaller operation current and improved switching distributions. With 2 additional masks, one layer of plug-BE included cross-point memory array could be added on top of another one. No signal of inter-layer interference has been observed. Also, prototype binary oxide based diodes have been fabricated for the purpose of suppressing intra-layer interference of cross-point memory array. suppressing intra-layer interference of cross-point memory array[10].

Nam Sung Kim, Todd Austin David Blaauw, Trevor Mudge, Ann Arbor, Jie S. Hu, Mary Jane, Irwin Mahmut Kandemir, Vijaykrishnan Narayanan, "Leakage Current: Moore's Law Meets Static Power", et Off-state leakage is static power, current that leaks through transistors even when they are turned off. It is one of two principal sources of power dissipation in today's microprocessors. The other is dynamic power, which arises from the repeated capacitance charge and discharge on the output of the hundreds of millions of gates in today's chips. It is one of two principal sources of power dissipation in today's microprocessors. The other is dynamic power, which arises from the repeated capacitance charge and discharge on the output of the hundreds of millions of gates in today's chips. sub threshold leakage, a weak inversion current across the device; and gate leakage, a tunneling current through the gate oxide insulation[11].

III. SYSTEM DESIGN

A. CMOS Design for WSN

Complementary metal-oxide-semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS

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technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. CMOS is also sometimes referred to as complementary-symmetry metal-oxide-semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.[1]

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.[2]

The phrase "metal-oxide-semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminium was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and beyond.[4]

B. SRAM for WSN

Static random-access memory (SRAM or static RAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. In addition to such six-transistor (6T) SRAM, other kinds of SRAM chips use 4, 8, 10 (4T, 8T, 10T SRAM), or more transistors per bit. Four-transistor SRAM is quite common in stand-alone SRAM devices (as opposed to SRAM used for CPU caches), implemented in special processes with an extra layer of polysilicon, allowing for very high-resistance pull-up resistors. The principal drawback of using 4T SRAM is increased static power due to the constant current flow through one of the pull-down transistors. This is sometimes used to implement more than one (read and/or write) port, which may be useful in certain types of video memory and register files implemented with multi-ported SRAM circuitry.[12] Generally, the fewer transistors needed per cell, the smaller each cell can be. Since the cost of processing a silicon wafer is relatively fixed, using smaller cells and so packing more bits on one wafer reduces the cost per bit of memory. Memory cells that use fewer than four transistors are possible – but, such 3T or 1T cells are DRAM, not SRAM (even the so-called 1T-SRAM).[13]

Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M_5 and M_6 which, in turn, control whether the cell should be connected to the bit lines: BL and \overline{BL} . They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins.[14]

C. Hetero Junction CMOS

This is a junction between two different node; which functions as a diode. heterostructure uses gate-controlled modulation. Heterostructures are fully compatible with current MOSFET. In MOSFETs, the source and Drain are interchangeable, with the distinction only determined by the voltages during operation.[16]

D. Writing circuit, Self enable switching circuit, Reading circuit

The writing circuit to enhance the STT-MRAM architecture. To optimize the complexity level. The write driver provides a bidirectional current passing through MTJ. The enable circuit to improve the writing speed in STT-MRAM architecture. Although the speed of STT switching has been proved as fast as subnano second, the STT switching is stochastic and some input data could not be stored correctly during one limited writing pulse. Both the power-efficient write and the whole lifetime of MTJ can be greatly improved because of the shortened switching duration and the

reduced switching number. The analysis of sensing output is worse due to the high resistance in sensing circuit. To improve the reliability of reading circuit.[17]

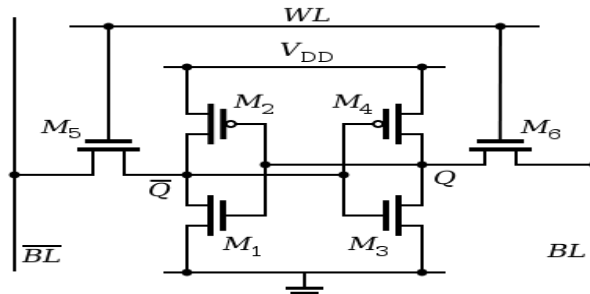


Fig 1 SRAM Design

E. System Block Diagram

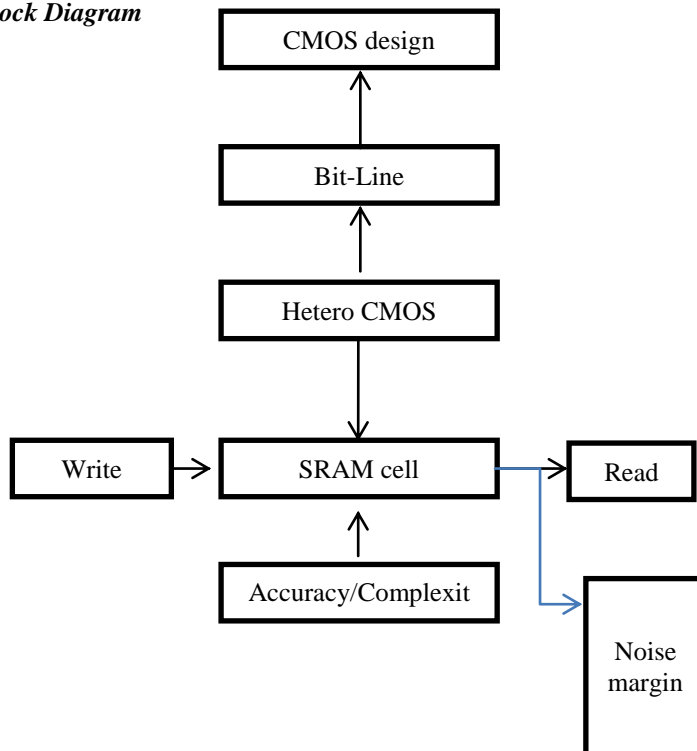


Fig 2. System Block Diagram

IV.HETERO JUNCTION SRAM DESIGN

Our proposed design replacing the existing block by Hetero junction technology. Our phase1 work is to reduce noise margin using CMOS technique. This technique modifies the existing system. Single BL SRAM uses only one Bit-Line for read operation. Hence we propose Single BL SRAM design based on hetero CMOS design. The proposed design of hetero CMOS Provides less power consumption. By the proposed design of SRAM, the part of Hetero junction CMOS as shown in bellow figure. This circuit makes the read operation with reduced power consumption. This technique to improve the writing speed architecture in SRAM. And to reduce the noise level. This technique to

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enhance and optimize the SRAM architecture. Hence the complexity will be reduced and power consumption can be obtain by our proposed system.

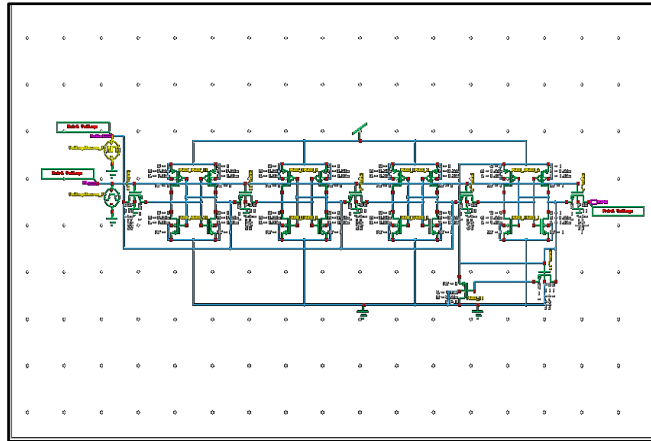


Fig 3. Schematic Diagram of Hetero junction CMOS Design

V.RESULT ANALYSIS

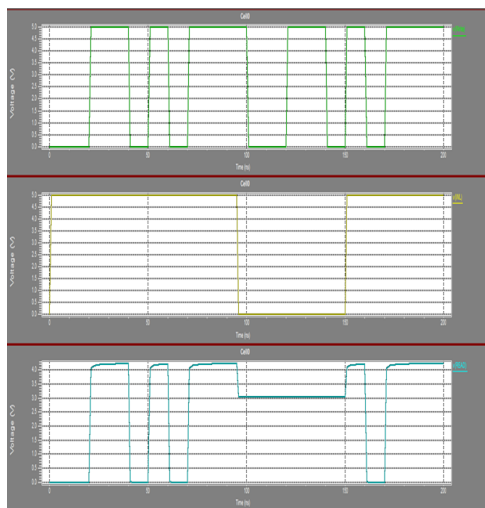


Fig 4 Simulation result of Design of SRAM
(a)input (b)write(c)Read of SRAM

The simulation result shows the input and output. First the clock is enabled and then the input data values is assigned. After that simulation the read and write is performed. The input data reads the written date if it is high.

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Noise Measurement

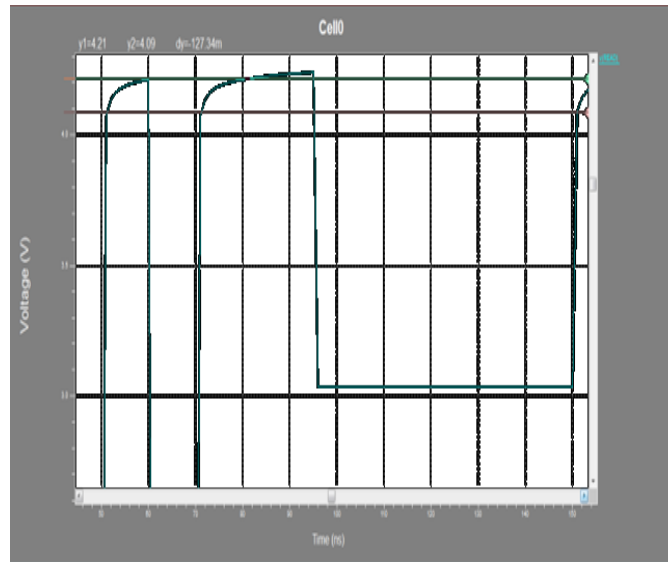


Fig 5. Noise Measurement

The above result show the leakage power is less than the existing method. In the proposed circuit the power obtained is 127mV. In the Existing method the output power is 140mV.

Accuracy

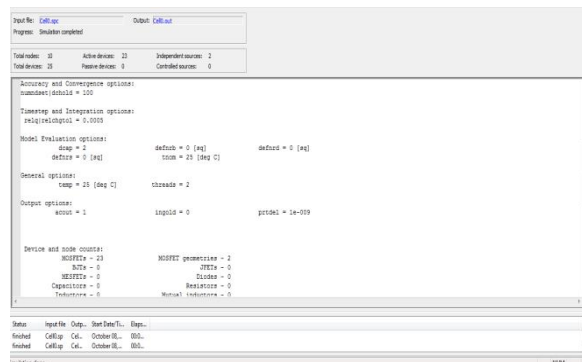


Fig 6 Accuracy

The above window shows the accuracy. It gives 100% accuracy than the existing method. In existing method achieved only 98%. It provides better accuracy than the existing method.

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Parameter	Conventional system	Proposed System
Read Noise Margin	140mv	127mV
Accuracy	98%	100%

Table 1 Performance of proposed system

VI. CONCLUSION

In this project, from existing design of SRAM based on Conventional design is Proposed in our work with Hetero junction CMOS technology, In the existing design that was based on power reduction and noise reduction, but our proposed design provides promising result than existing system. Our work concentrated on reduction of Noise in read port and reduced delay, and also area efficiency, thus from the overall parameters we have achieved better performance than the existing design of Flip-flop. For this design held in CMOS design methodology and we have used Tanner EDA 13.0 as simulation tool to show the performance analysis.

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BIOGRAPHY

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