

A Low Power Pipelined ADC Using Time Shifted Correlated Double Sampling (CDS) Technique

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ABSTRACT: The pipelined ADC can be used for reducing power and predictive error rate. The digital and analog circuit designs have benefited from the speed, power, cost, and area improvements associated with the technology time-interleaved CDS. The Existing system reviews the pipelined ADC which discusses the design challenges for switched-capacitor circuits in deep-submicron CMOS technology. Our proposed system has a novel CDS technique using Time interleaved sampling design.

KEYWORDS: Sample and hold, Time-interleaved CDS, Comparator design, Analog-to-digital conversion (A/D), MDAC-Multiplying Digital-to-Analog Converter.

I. INTRODUCTION

Analog-to-digital converters (ADCs) are very important building blocks in signal processing and communication systems. Applications like wireless communications and digital audio video communication have created the need for higher speed and resolution, cost-effective data converters. Among different ADC architectures, flash ADC can achieve reduced power consumption. The main challenge lies on the constant speed, which makes more critical design[4]. A wide-band communication systems using comparator-sharing pipelined analog to digital converter technique is used to achieve a widely scalable conversion rate with a constant FOM, where the capacitor network is custom designed to suppress the gain mismatch between the two DAC's, but the conversion rate is too complicate[2]

In a low power comparator sharing technique [6] the sampling phase is removed to reach the full efficiency of the comparator. This design not uses any static components to achieve a widely scalable conversion rate with a constant FOM.

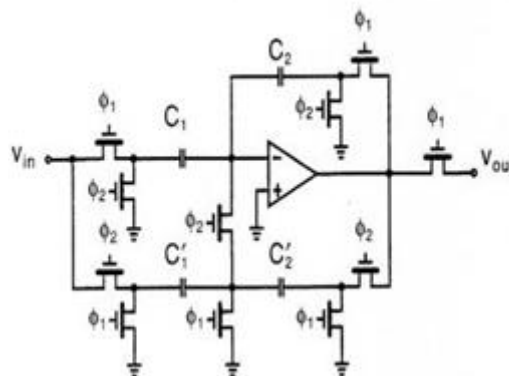


Fig 1.Flicker noise minimization

In this way, we reduce the design effort and minimize the additional power consumption. Fig 1.shows an flicker noise minimization design, where by using an CDS Technique to minimize the errors due to input offset voltages, 1/f noise and finite gain, because this error is inversely proportional to the op-amp gain.

The rest of this paper is organized as follows: in section II we describe the prior CDS techniques. In Section III, we briefly review time shifted CDS technique. Measurement and comparison results are summarized in section IV and we make some concluding remarks in section V.

II. OVERVIEW OF CDS TECHNIQUE

The most important pipelined ADC with semi digital transconductance based amplifier follow an resistor ladder technique can be used to determine the transconductance of the amplifier, and their speed of conversion rate, in practice which can be applied only for semi-digital driver circuit [5]. In the input swapped op-amp sharing technique, the memory effect occurring in the op-amp sharing process, and automatically correct the current of the V/I converter, has been developed.

The proposed ADC achieves low power consumption, high noise immunity, and has small area, by employing an input swapped op-amp sharing technique in that summing node in an multiplying digital-to-analog converter and V/I converter with supply voltage, and temperature condition detector. The ADC shows a differential nonlinearity (DNL) of less than 0.48 LSB, and an integral non linearity (INL) of less than 0.95 LSB. Also, an signal to distortion ratio of 56.2dB is measured with a 1 MHz input frequency. This has been implemented in a 0.18µm CMOS process, and occupies 1.6*0.8mm² of active area.[6]

An op-amp operating in a linear mode with negative feedback, using balanced, split-voltage power supply has its transfer function typically written as

$$V_{out} = A_0 (V_1 - V_2) \tag{1}$$

Where V_{out} is output voltage, A_0 is gain of the op-amp, and V_1, V_2 is input voltages.

The gain of op -amp as comparator is given by the given equation:

$$V(out) = V(in) * A \tag{2}$$

Where $V(out)$ is comparator output voltage, $V(in)$ is comparator input, and A is a gain of the input.

A low power comparator design for 6-Bit flash ADC in 90nm CMOS follows an inverter based comparator which creates low power dissipation[7]. Unfortunately , it has some drawbacks. First it is possible at only ultra wide band applications using CMOS 90nm technology. Second mismatch will be occurred in some transistors. The error e caused by the finite gain is expressed as follows:

$$e = 1/A^2 (1 + C_s/C_f) \{ (1 + C_s + C_f/C_f) V_0 - C_i/C_f V_{o-p} \} \tag{3}$$

Delay of comparator and finite output resistance of current sources will directly affect the accuracy of comparator based circuits. As a result the accuracy degrades for high sampling rates. In this paper , new techniques are proposed to increase the sampling speed of comparator-based MDAC while maintaining the accuracy, where we have the coarse phase and fine phase. Coarse charge transfer phase is used to obtain quick, rough estimate of output and virtual ground condition while fine transfr phase is utilized to obtain more accurate and virtual ground condition. For a very high frequency the input impedance of the stages is low. When the voltages are nearly equal, the output voltage will not fall into one of the logic levels thus analog signals will enter the digital domain with unprectable results.

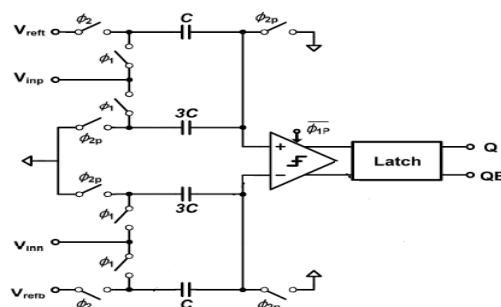


Fig 2.Switching capacitor with latch model

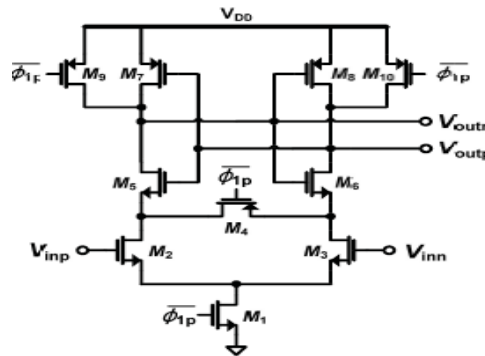


Fig 3.Simple comparator design

In the odd phase, the capacitors C_S and C_F samples actual input V_{in} . During even phase C_S and C_F samples V_o . The energy storage device and the heart of the SHA is capacitor. Fig 2 shows the switching capacitor with latch model. The switching circuit and its driver form the mechanism by which the SHA is alternatively switched between track and hold. Fig 3 shows simple comparator design that compares two voltage or current outputs. They are commonly used in devices that measure and digitize analog signals, such as Analog-to-Digital converters (ADCs), as well as relaxation oscillators [8].

III. TIME SHIFTED CDS

The most important conventional comparator have been replaced with the CMOS inverter base comparator design, the reported structure of the ADC is designed using time aligned CDS with the aim of increasing design efficiency[3]. Our time aligned CDS technique follows the two phase dependent gain transition outputs. Reference voltage flow depends on number of gain transition into next stage. The gain transition output flow throws switching capacitors C , the value of C is chosen as small as 50fF. During phase ϕ_1 input is applied to the input terminal of both capacitors. During phase ϕ_2 input signal will be sampled, both capacitors shorted to op-amplifier circuit. An operational amplifier (op-amp) has a well balanced between difference input and a very high gain.

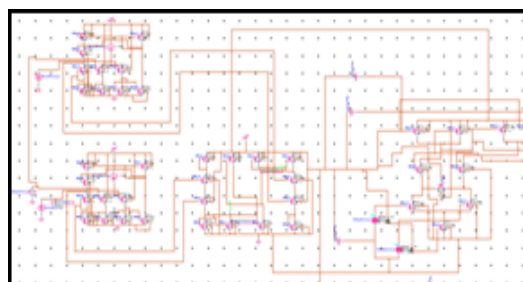


Fig 4. Schematic diagram for time shifted CDS

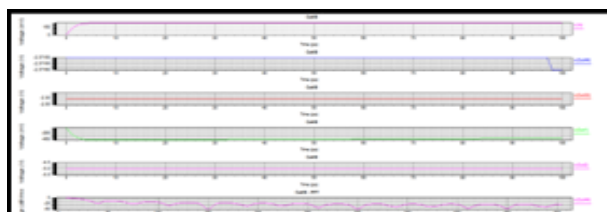


Fig 5. Measured FFT Output for different voltage sources

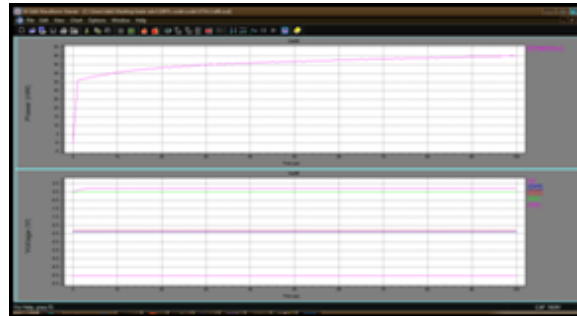


Fig.6. Measured power output for voltage source

Fig.4. shows the schematic diagram for our proposed system. Where the schematic follow an sample and hold circuit, time interleaved CDS, comparator design, and ADC output.

A standard op-amp operating in open-loop configuration (without negative feedback) may be used as a low-performance comparator. The op-amp's output voltage is limited by the supply voltage. Comparator will generally be faster than a general-purpose operational amplifier pressed into service as

Table.1. Power Analysing of pipelined ADC

Parameter	Pipelined ADC	Pipelined ADC using Time Shifted CDS
Power	32mW	50nW

a comparator. A dedicated voltage comparator may also contain additional features such as an accurate, internal voltage reference.

Operational transconductance amplifier (OTA) provides larger output swing, since the accumulation error will occur, which degrades the linearity of the ADC.

In our system an op-amp has a well balanced difference input and a very high gain. This parallels the characteristics of comparator and can be substituted in applications with low-performance requirements. A standard op-amp operating in open loop configuration may be used as a low performance comparator. When a non-inverting input is at a higher voltage than the inverting input, the high gain of the op-amp causes the output to saturate at the highest positive voltage it can output. An op-amp operating in a linear mode with negative feedback, using a balanced split voltage power supply, has its transfer function typically written as equation number (1).

IV. EVALUATION

A. Measurement Results

The measured Fast Fourier Transform (FFT) spectrum is shown in Figure 5. Which uses the sampling rate 40GHz. Figure 6 shows the measured power consumption which was 50nW.

B. Comparison results

Table 1 shows the comparison of our design with pipelined ADC technique, however, the power consumption of the entire ADC is reduced around 50%. In comparison with resistor ladder technique [5] although predictive error was reduced. The mismatching error and nonlinearity function of the transistors are also reduced, but it requires high sampling frequency. From these results, we conclude that our technique reduced the power without any input swapping.

In the advanced CMOS process, two-stage op-amp topology would be used to achieve enough output signal swing at a low supply voltage[9]. The calibration reduces errors from finite op-amp gain and increases the maximum allowable output swing of the op-amps, which reduces the required power dissipation with given overdrive voltages. The calibration takes effect immediately and appears at the ADC output after its latency [10].

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V. CONCLUSION

The predictive error of the proposed system is analysed and the output is propagated successfully. A transformer provides a signal-to differential input signal conversion. The power was reduced by providing time shifted double sampling CDS technique.

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REFERENCES

- [1] Jong-Kwan Woo, Hyunjoong Lee, Hwi-Cheol Kim, Deog-Kyoon Jeong, and Suhwan Kim, transactions on very largescale integration (vlsi) systems, "1.2 V 10-bit 75 MS/s Pipelined ADC With Phase-Dependent Gain-Transition CDS" in IEEE trans vol., 22, no. 3, March 2014.
- [2] Chenghao 1; 2; Yan Jun 1, Shi Yin 1, and Sun "A 130 nm CMOS low-power SAR ADC for wide-band communication systems" No. 2 Journal of Semiconductors February 2014.
- [3] Parthasarathy K, Dr. K. C. Narasimhamurthy., "A Low power comparator Design for 6-Bit flash ADC in 90nm CMOS", JEAT-2014.
- [4] Bian Chenhao yan jun, Shi Yin and sun ling., "Low power CMOS flash ADC" journal of semiconductor-2014.
- [5] Morie. T, ozeki. T, dosho. T., "10 bit 100MS/s pipelined ADC using input swapped op-amp sharing and self calibrated V/I converter", in IEEE trans. March-2011.
- [6] Byungsub kim, hong-june park, jae-yoon. "A 10 bit 25MS/s 1.25mW pipelined ADC with a semi digital Gm based amplifier" in IEEE trans. March-2011.
- [7] P. Nuzzo, F. D. Bernardinis, P. Terreni, and G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.
- [8] D. Shinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold time," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, Feb. 2007, pp. 314–315.
- [9] Jin-Fu Lin, Student Member, IEEE, Soon-Jyh Chang, Member, IEEE, Chun-Cheng Liu, Student Member, IEEE, and Chih-Hao Huang, "A 10-bit 60-MS/s Low-Power Pipelined ADC With Split-Capacitor CDS Technique" *IEEE transactions on circuits and systems—ii: express briefs*, vol. 57, no. 3, march 2010.
- [10] Omar A. Hafiz, Xiaoyue Wang, Paul J. Hurst, and Stephen H. Lewis, Omar A. Hafiz, Xiaoyue Wang, Paul J. Hurst, and Stephen H. Lewis, "Immediate Calibration of Operational Amplifier Gain Error in Pipelined ADCs Using Extended Correlated Double Sampling", *IEEE journal of solid-state circuits*, vol. 48, no. 3, march 2013.

BIOGRAPHY

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