

A Review on Clock Skew Compensation Techniques

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ABSTRACT : We can define the clock as the difference in the arrival time between different memory elements. Thus these differences in clock signal arrival times across the chip are called as clock skew. It is important while designing that timing must satisfy register setup and hold-time requirements. The data propagation delay and clock are parts of these delay calculations. The clock distribution networks try to match the flow of data signals among similar data paths. The way they are designed can dramatically affect the system wide performance and reliability. A number of theoretical backgrounds of clock skew are provided in order to understand better, how clock distribution networks try to interact with data paths. The changes in the timing from minimum to maximum are developed from the relative timing between the local clock skew and the data paths.

KEYWORDS: Clock distribution networks, clock trees, clock skew, clock skew scheduling, interconnect delay, process variations, synchronization, timing optimization.

I. INTRODUCTION

In a synchronous digital system, the clock signals can be defined as a time reference, so that the data can move within the system with a certain reference so that we will be able to calculate the delay in the system. The clock function is very important in the operation of a synchronous system, as the word synchronous itself tells us that the clock must be in sync. That is the reason why much attention has been given to the characteristics of these clock signals and the networks used in their distribution. Clock signals are often considered to be simple control signals, however these signals are one of the most important factor to be considered during circuit [3]. This paper review tells us that how clock skew occurs when the clock signals arrive at sequentially adjacent storage elements at different time used and how different techniques have been used over the years. Although, it has been shown that intentional clock skew can be used to improve the clock frequency of a synchronous circuit clock skew is typically minimized when designing the clock distribution network, since unwanted or unintentional clock skew due to process parameter variations may put a limit to the maximum frequency of operation. Clock skew may cause circuit failure independent of the clock frequency (*i.e.*, race conditions) [4]. Over the years as the silicon fabrication technology is developing, the chip sizes are getting bigger and better. Along with the number of logic gates the operating frequency is also increasing, and because of this entire clock skew becomes very important in ensuring the proper functioning of VLSI chips. As you go on increasing the clock speed in the design it becomes very difficult to reduce clock skew on chip. Clock skew also occur due to different RC delay of clock which interconnect along with different clock signal paths and different delays of clock buffers due to process variations, temperature differences on the same chip, and power supply differences due to power rail IR drop [5]. Another method involves to reduce clock skew by clock distribution network which should be carefully designed. As the frequencies of processors continue to increase in the multi-GHz space, the clock skew becomes one of the main factors that constrain the improvement of clock frequencies and affects the reliability of systems [6]. In this review paper we will see the different clock skew reduction techniques used over the years and how using these different methods and researches has tried to overcome the issue of clock skew.

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II. METHODS USED

1. CMOS Delay Locked Loop (DLL) and Phase Locked Loop (PLL)

Delay Locked Loops are negative feedback control systems that try to adjust the propagation delay of an internal circuit so that it matches the period of a reference signal or the standard signal. PLLs are also negative feedback control systems that try to adjust the oscillation frequency and phase of internal oscillator so that they match the frequency and phase of a reference signal and the regulation of delay range in PLL is unlimited and tracking jitter is also very large as compared to DLL [8]. Ideally the clock signals should have no skew that means ideally they should have no propagation delay. Flip flops and latches receive clock at different time instances and for faithful operation of the circuit the time difference should be ideally zero. However practically it is not possible and 10% of the clock is wasted in compensating clock skew[7].DLLs have the high deskewing resolution, but long locking time and high power. Therefore it is very important to keep clock skew under control.

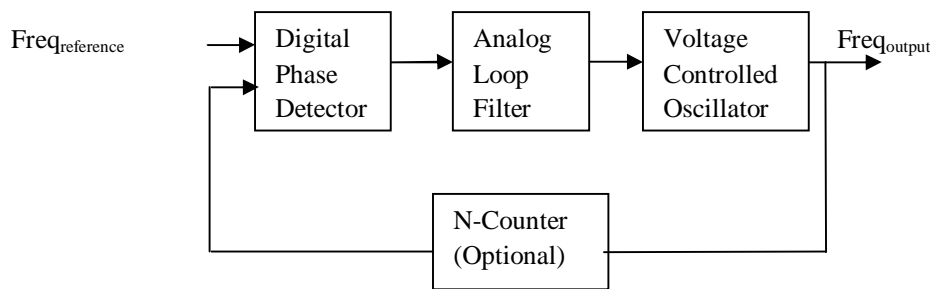


Figure 1. Digital Phase Locked Loop [15].

The important advantages to PLL clock generation do not come without a price. A PLL, unless designed completely from digital circuitry, is essentially an analog circuit, and requires very careful design. The noise inherent in a digital system, especially a high-speed microprocessor, can cause many problems for a PLL clock generator. Furthermore, PLLs typically require relatively large passive elements for stable operation. Some integrated circuit technologies do not lend themselves well to the creation of such structures. Last, but certainly not least, even a well-designed PLL exhibits variation in its output phase and frequency over time

III. CLOCK TREE

2.1 Buffered Tree Distribution

First we will study one of the most common method for distributing clock signals in VLSI applications which is the clock tree method. The tree structure shown in fig.2 is so called because buffers are placed between the source which is a clock and along the clock paths as they branch out towards the clock loads.

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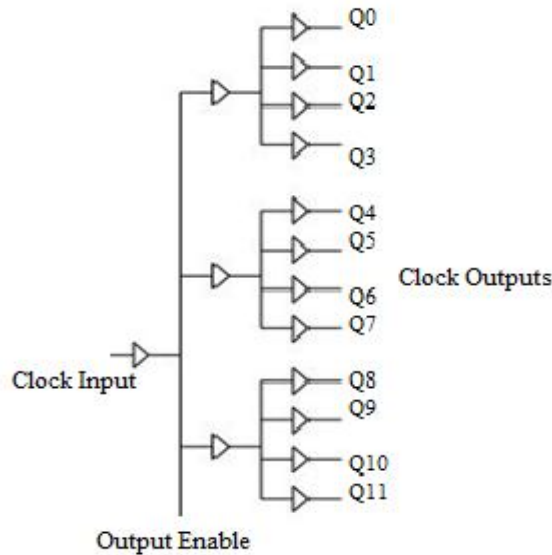


Figure 2. Buffer tree clock distribution [11].

This tree structure is so called because buffers are placed between the source which is clock and along the clock paths as they branch out towards the clock loads.

2.2 H-Tree Distribution

This method aims to produce zero skew- clock routing technique by matching the length of every path from clock source to register load. This is accomplished by creating a series of H-shaped routes from the centre of the chip as illustrated by fig. 3. In the fig.3 below we can see that at the corners of each "H" as the shape which is similar to the letter "H" in English language the nearly identical clock signals provide the inputs to the next level of smaller "H" routes [11].

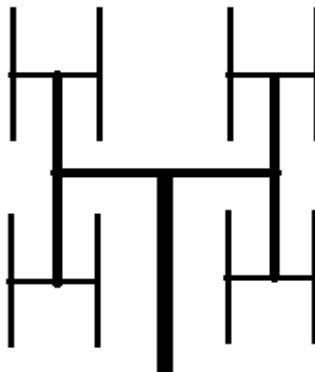


Figure 3. H-Tree Distribution [11].

As the magnitude of the clock skew is only significant for sequentially adjacent registers, the symmetry which is provided by H-tree distribution is largely unnecessary. If we consider the additional interconnect capacitance which

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may lead to increase power dissipation, the benefits of zero clock skew may not be worthy of the price. The clock grid connects the outputs of a number of clock distribution drivers of the same level, thus averaging their delays.

IV. WIRELESS CLOCK DISTRIBUTION

Clock distribution is a crucial part of modern multi-GHz microprocessor design. Conventional distribution schemes are more or less monolithic in that a single clock source is fed through different levels of clock buffers to eventually drive almost the entire chip. Because of which a number of challenges are raised [11]. Optical interconnect is a method that offers numerous benefits over the electrical interconnects, including the potential for dense high-bandwidth interconnections, essentially no distance dependent signal loss or degradation, and immunity to electromagnetic interference [12]. Wireless interconnect should provide an additional means for global communications by freeing up conventional wires for other uses. This new interconnect technology is being developed utilizing a clock distribution system as the driver. With the use of wireless interconnects in a clock distribution system, it should reduce the latency in the clock tree which should help reduce clock skew and should eliminate the frequency dispersion problem that may ultimately limit the maximum clock frequency [11]. Most of the time all conventional optical interconnects use continuous wave (CW) lasers, which are either driven directly or they externally modulated. We can use short pulses or square wave pulse like return to zero (RZ) data format whose data bit is half the bit rate, hence short pulses which can be used to switch on and off the LED or Laser acting as optical sources. Several aspects of such short optical pulses provide advantages over a system using modulated CW beams. Another theory that I have read is about optical clock skew compensation obtained by shuffling the bits before transmitting and rearranging the bits again at the receiver known as mB1C shuffling technique [14]. With this method as the data is sent parallel and if any data packets are lost then, only 1 bit from each channel is lost instead of the entire message.

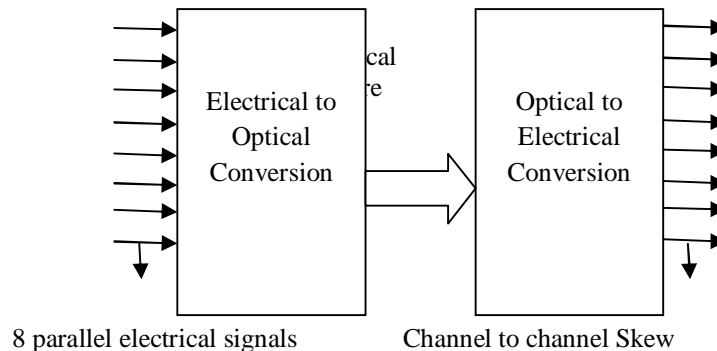


Figure 4. Variance among propagation delays results in channel-to-channel skew.

Sending of this data parallel is shown in fig.4. The advantage of using optical data is that electrical crosstalk is mitigated and reflections are avoided without power consuming terminations. Additionally, optical interconnection enables new approaches such as wavelength division multiplexing (WDM) and precise optical clocking for time-division multiplexing (TDM) of data are also possible with optical interconnects. WDM offers flexible bandwidth, while optical clocking enhances interconnect performance [13]. Other advantages are freedom from capacitive loading effects which allows greater fan-in and fan-out, immunity to mutual interference effects, lack of planar constraints resulting in reduced cross-coupling for criss-crossing waveguides, reconfigurability of free space focused interconnects and possibility of direct injection of optical signals into electronic devices without the need for optical to electrical conversion.

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V. CONCLUSION

Thus after going through a lot of research work on clock skew, we can conclude that reducing the delay and obtaining clock skew is a difficult process and over the years lot of techniques have been introduced to overcome clock delay and compensate the same. Thus these number of research works and results tries to show that how delays in micro, nano and pico seconds can hamper the entire working of the circuit with addition to power consumption too.

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