

# Design and Implementation of Vedic Multiplier using Positive Feedback Adiabatic Logic

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**ABSTRACT:** In recent years, low power circuit design is crucial issue in any system. Adiabatic logic dissipates less power than static CMOS logic. It has been a significant approach in low power circuit design. A high speed processor greatly depends on the multiplier as it is one of the key hardware block in most of the processing systems. A multiplier designed by vedic mathematics will be very fast. Of the different sutras present urdhva trivakbhyam sutra is used in this paper. This paper presents a simple multiplier structure based on Urdhva Triyakbhyam sutra of vedic mathematics, by applying positive feedback adiabatic logic(PFAL). As the energy that is transferred to the load is mostly recovered the power consumption of the proposed multiplier is significantly low. The proposed multiplier structures have been designed in 0.13um CMOS technology and verified by pyxis schematic editor.

**KEYWORDS:** Adiabatic logic, Low power, vedic multiplier.

## 1. INTRODUCTION

The performance of a processor is determined by its speed. For any system a Processor with High speed is an important requirement. In any processing system multiplier is a fundamental operator. So a high speed multiplier has more demand in up surging VLSI technology. This paper mainly focuses on fast multiplication using Vedic Mathematics. Earlier some multipliers like booth multiplier, Modified Booth Multiplier, and array multipliers were considered for high speed multiplication. But in these a lot of intermediate steps are involved. This leads to reduction in speed for increased bit lengths. For any signal processing and data processing applications Multiplier forms the essential and basic arithmetic operation. In any multiplication operation the speed of the multiplier is a constraint. So by reducing the steps involved in any computation an increase in speed can be achieved. In any system the efficiency is determined by the speed of the multiplier.

Energy efficiency is more important for high performance applications. As the power dissipation increases, heavy, expensive cooling machines and heat sinks, and fans are required. Many power management techniques have been developed to reduce this power dissipation. One of them is scaling the power supply voltage. As the technology scales down below 90nm, eventually it becomes more difficult to scale the supply voltage. The power dissipation in conventional CMOS circuits can be reduced by using adiabatic technique. By using adiabatic technique, the energy dissipated in PMOS network can be reduced. Instead of dissipating the energy stored at load capacitance as heat, it can be recovered. The variation in parameters highly effect the adiabatic logic technique.

Section II illustrates about vedic multiplier and adiabatic logic. The importance of vedic multiplier, its design and implementation are described. The importance and different types of adiabatic techniques are discussed in section II. Section III discuss about the results of different vedic multipliers and adiabatic vedic multiplier. Section IV discusses the conclusion of the work.

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## II. LITERATURE SURVEY

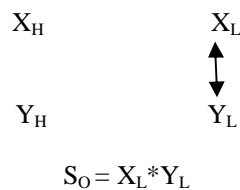
### Vedic Multiplier

Vedic mathematics is derived from Atharvana veda. It consists of different sutras which describe different mathematical calculations. In the multiplication process using vedic algorithm Urdhva Tiryagbhyam sutra is the most preferred one. Urdhva Tiryagbhyam means vertically and crosswise multiplication. For the design of convenient and fast processing systems involving decimal number multiplication it was discovered. All the partial products in vedic multiplier are generated in parallel, as a result the multiplier operates fastly. By using vedic multiplier the number of AND gates, Half adders and Full adders can be reduced. As all the partial products and sums are generated in parallel it is independent of operating frequency. The net advantage of this multiplier is that there is no necessity of higher clock frequencies. Vedic multiplier is area, speed and power efficient.

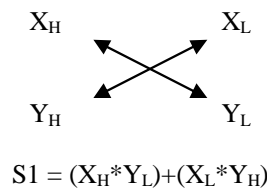
### Implementation of general vedic multiplier

In this we discuss the organization of 2x2 multiplier block. From this we can construct 4x4, 8x8, etc multipliers. Let us consider 2 inputs (X and Y) having two digits each (X—X<sub>1</sub>X<sub>0</sub> and Y—Y<sub>1</sub>Y<sub>0</sub>) and we get the outputs (S<sub>3</sub>S<sub>2</sub>S<sub>1</sub>S<sub>0</sub>) as the result. To implement any NxN multiplier in vedic multiplier style we need an N/2 x N/2 multiplier. So basically a 2x2 multiplier is required for implementing any higher multiplier. The following cases illustrate the multiplication of general vedic multiplier.

Case 1 :



Case 2 :



Case 3 :

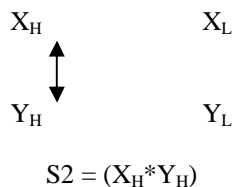


Fig. 1. General implementation of vedic multiplication

Here, X and Y are inputs and S is the output. X<sub>H</sub> and Y<sub>H</sub> are the higher order bits of the inputs X and Y. X<sub>L</sub> and Y<sub>L</sub> are the lower order inputs of the inputs X and Y. The carry generated in each case is forwarded to next case and the generated sum is taken as output. This sort of algorithm can be applied to any number of bits.

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The following figure depicts the 2\*2 Vedic multiplier.

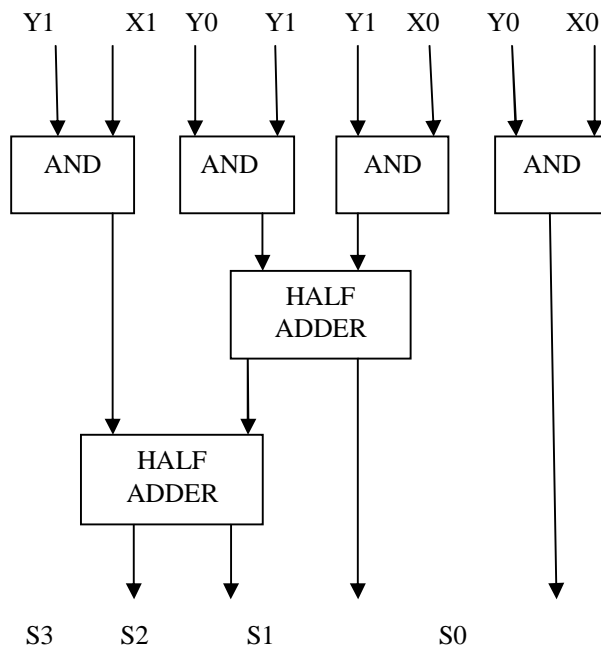


Fig. 2. 2\*2 Vedic Multiplier

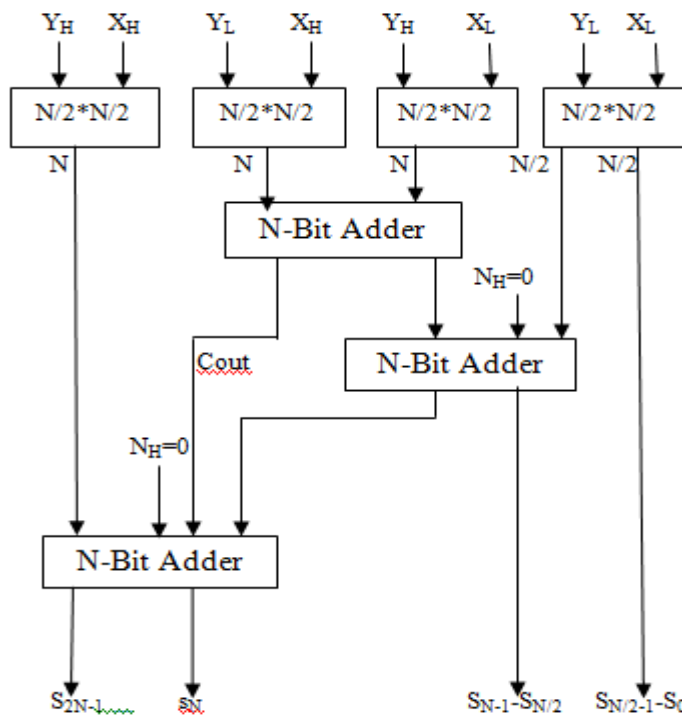


Fig.3. Block diagram of NxN Vedic multiplier

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### Adiabatic logic:

The demand for ultra low power systems is the principle issue in VLSI design. Reducing supply voltage, reducing switching activities and decreasing the physical capacitance are some of the classical approaches to reduce dynamic power. As the technology scales down, these techniques go vain in achieving low power.

Dynamic power dissipation and static power dissipation are two types of power dissipations in any digital CMOS circuits. In any circuit a signal switching from low to high and high to low leads to Dynamic power dissipation. The logic states of the system determine the static power dissipation of the circuit and it does not depends upon the signal switching action. In any digital CMOS circuit the average power dissipation is given by

$$P_{avg} = P_{sw} + P_{static} + P_{sc} + P_{leak} \quad (1)$$

In the above equation  $P_{sw}$  is switching power dissipation,  $P_{static}$  is the static power dissipation,  $P_{sc}$  is the short circuit power dissipation and  $P_{leak}$  is the power dissipated due to leakage current. All these powers dissipations can be reduced by some techniques such as lowering supply voltage, reducing capacitance, reducing switching activities ect. But these techniques are fit enough to meet today's power requirements. So a new technique namely adiabatic technique is introduced to reduce power consumption.

Adiabatic is a greek word which describes a system in which transition occurs without energy being lost or gained from the system. In other words, i.e., in electronic system context it depicts preservation of electronic charge rather than heat. Thus an electronic charge is neither gained nor lost in an adiabatic system. In a conventional CMOS circuit load capacitor is charged from a constant voltage source where as in a adiabatic circuit it is charged by a time varying voltage source.

Adiabatic families are classified as partially adiabatic or fully adiabatic. In a fully adiabatic logic circuit the charge that is present at the load capacitance is mostly recovered where as in a partial adiabatic logic some portion of charge is allowed to the ground. Regarding input power clock synchronization and operating speed fully adiabatic logic faces a lot of problems. So in most of the cases partial adiabatic logic circuits are preferred.

In any adiabatic logic power clock plays a very important role. For increased bit lengths of any application of adiabatic logic power clock synchronization becomes difficult and plays an important role. When it increases or decreases a very small drop in voltage present at the switching device. The power clock supply is the supplier of energy for the circuit. It not only supplies energy but also recovers it. A separate power clock generator can be designed or supply source that is readily available can be used. In the work proposed a sinusoidal power clock supply is used. The total power dissipation in a adiabatic circuit is expressed in the following terms:

$$E_{diss} = (2RC)/T \cdot C_L \cdot V_{DD}^2 \quad (2)$$

In the above equation RC represents the time constant and T represents the time period. For  $RC \ll T$ , the system having adiabatic logic will operate at an higher efficiency.

Of the different adiabatic logic used in regular practice efficient charge recovery logic(ECRL) and positive feed back adiabatic logic(PFAL) are used at higher extent. In a ECRL logic, the logic levels are degraded so to avoid that drawback PFAL is used. Because of feed back path in PFAL the levels are sustained.

### III. PROPOSED WORK

The Partial energy recovery circuit structure named positive feedback adiabatic logic(PFAL) is used for the proposed work as it shows the lowest energy consumption when compared to other similar families.

Different types of adiabatic logic styles such as ECRL, EEAL and PFAL are compared with the conventional CMOS logic for an inverter. Output voltages of different adiabatic logic styles are simulated at 100MHz frequencies with a load capacitance of 20fF.

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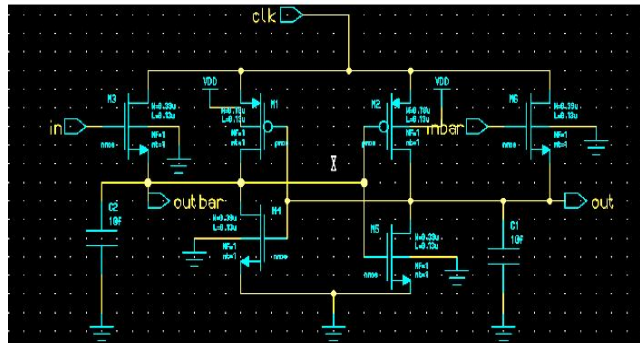


Fig. 4. PFAL inverter

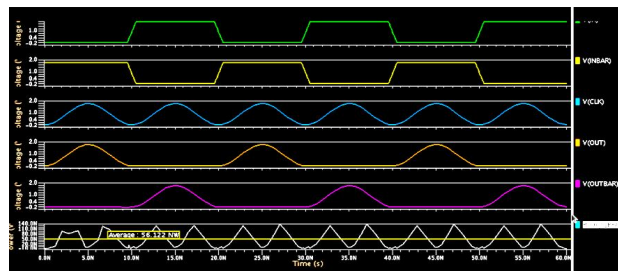


Fig.5. output of PFAL inverter

TABLE I  
POWER DISSIPATED FOR DIFFERENT INVERTERS

s.no	Type of adiabatic logic	Power dissipated (nW)
1	CMOS	4887.9
2	ECRL	624.56
3	EEAL	49.72
4	PFAL	56.12

The results of different adiabatic inverters show that conventional CMOS logic exhibits highest power dissipation where as different adiabatic techniques exhibit lowest power dissipation.

All the simulations are done at 1.8V supply voltage. During the simulation of a 2x2 multiplier we have considered the inputs as A0-0101, A1-0011, B0-0101, B1-0011.the results are obtained as follows:

The simulated waveforms of 2x2 Vedic multiplier and 2x2 PFAL multiplier are shown in fig.6. and fig. 7. Table II shows the results of different vedic multipliers, their power and their delays. The Table II shows that 92% of the power is saved by implementing in PFAL logic. By using any adiabatic logic a considerable amount of power can be saved but at the cost of increase in delay. Static conventional CMOS logic style has been used to implement Vedic multiplier. We have designed an adiabatic logic family, consisting of common digital gates such as inverter, two inputs and three input functions, adder and multiplier blocks of varying bit length. W/L ratio of PMOS and NMOS are taken with  $W/L=12\lambda/2\lambda$  and  $6\lambda/2\lambda$  where  $2\lambda=0.18\mu\text{m}$  respectively.

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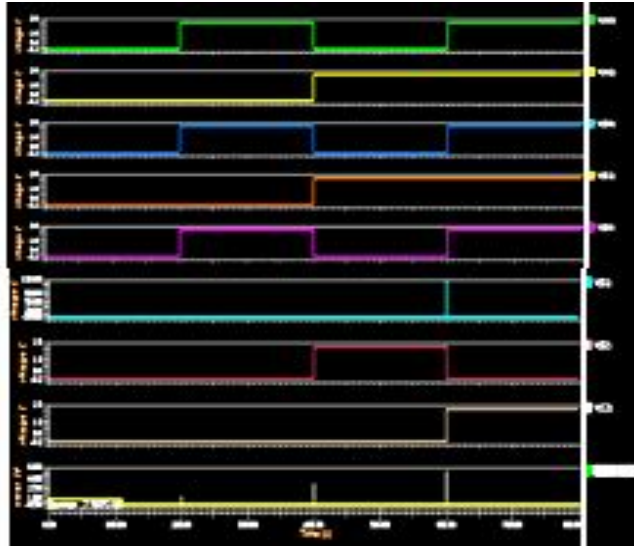


Fig. 6. Outputs of 2x2 Vedic Multiplier

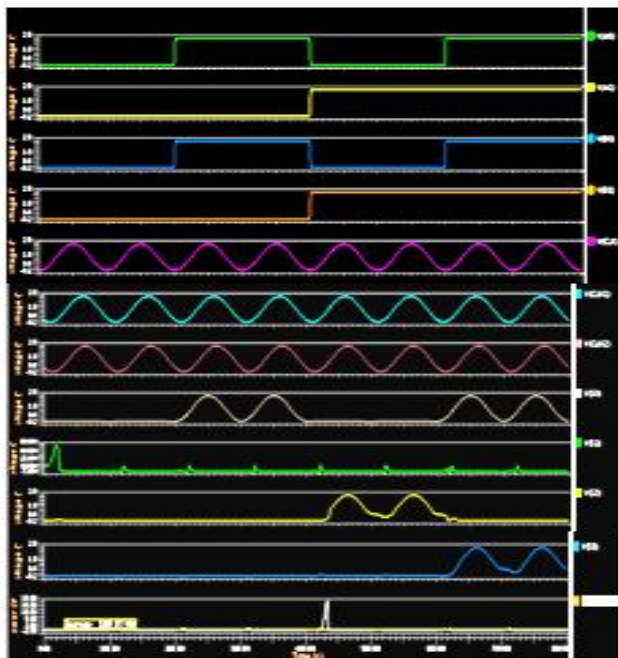


Fig. 7. Outputs of 2x2 PFAL Vedic Multiplier

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TABLE II  
POWER DISSIPATION AND DELAY OF VEDIC MULTIPLIERS FOR VARYING BIT LENGTHS

s.no	Length of multiplier	Power(uW)	Delay(ps)
1	2x2	2.563	114.87
2	4x4	46.718	658.76
3	8x8	302.94	826.69

Table III shows the result of 2\*2 positive feedback adiabatic logic vedic multiplier whose power dissipation is reduced when compared to conventional 2\*2 vedic multiplier.

TABLE III  
POWER DISSIPATION AND DELAY OF ADIABATIC MULTIPLIER

s.no	Length of multiplier	Power(uW)	Delay(ns)
1	2x2	0.18	25.12

### IV. CONCLUSION

An efficient adiabatic multiplier structure based on Urdhva Tiryagbhyam sutra of vedic mathematics has been proposed using PFAL logic. Simulation results for varying bit lengths are reported using pyxis schematic editor(mentor graphics) 130 nm technology. As the number of bits increases, clock synchronization becomes difficult.

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