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# Design of High Performance Double Edge Triggered D-Flip flop using MTCMOS Technique

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**ABSTRACT:** Synchronous logic design is an important stream in designing the integrated circuits (IC). Flip-flops are the basic building blocks in any synchronous design. A large amount of power is consumed by flip flops and latches due to redundant transitions and clocking system. In this paper, several flip-flops are analyzed and double edge triggered clock pair shared flip flop using Multi-threshold voltage CMOS is proposed (DETCPSFF). The flip-flops are evaluated based on parameters such as delay, power. Simulation results shows the proposed design has less delay than existing designs, which claims that proposed design is suitable for high speed applications. The flip-flops are simulated using Mentor graphics in 130nm technology.

**KEYWORDS:** Delay, Flip Flop, IC, MTCMOS, Power.

## I. INTRODUCTION

The present day technologies has set a goal of high performance with low power consumption for VLSI designer [1]. In digital systems, flip-flops are important timing elements and have a great impact on speed and power consumption of a circuit. To determine the performance of a synchronous circuit, it is important to determine the performance of a flip-flop. High performance can be achieved by increasing the frequency of clock. However, high clock frequency results in increasing the power consumption of clock system dramatically and also redundant transitions of clock takes place. Flip-flops and clocking network consumes about 30%-70% of the total power in the system [2].

An alternative method to use storage elements which are capable of capturing data on both rising and falling edges of the clock. Such storage elements are termed as Dual-Edge Triggered Flip-Flops (DETFs). Double Edge triggering doubles the rate of data processing or alternatively halves the clock rate thereby, increasing the data throughput or reducing power consumption in the clock circuit respectively. Half of the power in clocking network can be saved by using double edge triggering [3].

The power in a digital CMOS circuits is given by the following equation:

$$P = P_{\text{dynamic}} + P_{\text{short circuit}} + P_{\text{leakage}}$$

Here,  $P_{\text{dynamic}}$  is also known as the switching power and it is the power dissipated by charging and discharging the gate output capacitance is given by

$$P_{\text{dynamic}} = \alpha C V_{\text{dd}}^2 f$$

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Short-circuit power is the short circuit power and occurs when the gate inputs are at an intermediate level both the p and n type networks can conduct resulting in conducting path from  $V_{dd}$  to  $V_{ss}$ . Short circuit power is given by

$$P_{\text{short circuit}} = I_{\text{short circuit}} V_{dd}$$

Leakage is the leakage power. When the supply voltage decreases, the threshold voltage also decreases in order to maintain performance of the device. Leakage power is given by

$$P_{\text{leakage}} = I_{\text{leakage}} V_{dd}$$

Dynamic power is proportional to the square of the supply voltage and clock frequency, contributes highest power consumption among the three. The power consumption can be reduced by scaling the supply voltage. However it results in degrading the speed of the system. Reduction in clock frequency is achieved by using double edge clocking approach to reduce dynamic power. As the technology scales down leakage power becomes dominant. Multi-threshold voltage CMOS technique is employed to reduce leakage power.

This paper is divided into 6 sections. Section II presents technical background of various techniques to reduce switching activity. Section III, the proposed Dual edge triggered CPSFF using MTCMOS is presented. Section IV shows the simulation results and Section V includes counter design using the proposed flip-flop. Section VI concludes the paper.

## II. BACKGROUND

A large part of on-chip power is consumed by the clock drivers [4]. It is desirable to have less clocked load in the system. The switching activity mainly depends on the number of clocked transistors. For the minimization of clocked transistors, various techniques are

### A. Conventional DEFF

Conventional DEFF [5]-[6], is a dual edge triggered flip-flop having Master Slave structure. During the rising edge of clock the upper data path is triggered and lower data path is triggered on falling edge. Whenever the transmission gate is closed the inverter and other logic circuitry is used to hold the logic level. The data paths are connected with feedback loops such that, the logic level at the output is retained whenever the clock is stopped. Conventional DEFF uses 24 transistors of which 12 transistors are clocked transistors.

### B. Conditional Discharge Technique

Conditional discharge technique [7] can be applied for both implicit and explicit pulse triggered flip-flops. It uses double edge triggered pulse generator [8]. Here, the pulse generator is present external to explicit flip-flops thereby power overhead of the pulse generator can be distributed among a group of flip-flops. The extra switching activity is eliminated by adding an NMOS transistor which is controlled by the feedback signal Qb. During Low-High transition, the output Q changes to high and Qb changes to low. As long as the data input is at high, the output does not make transitions because of no discharging path for the output. Here, the delay is more due to longer stack of NMOS transistors.

### C. Conditional Data Mapping Technique

Conditional data mapping flip-flop [9] uses pulse triggered structure for high performance. CDMFF has a floating node on critical path. When clock signal (CLK) transits from low to high, CLKDB will stay high for a short while which produces an implicit pulse window for evaluation. During this period, the transistors P1, P2 are off, as a result the internal node X is not connected to  $V_{dd}$  and the output Q becomes high and Qb\_kpr becomes low. As a result the transistor N6 is on. In addition, if D transits from low to high, N3 is off making the pull down network to be

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disconnected from GND too. Hence internal node X is not connected with  $V_{dd}$  or GND during most pulse windows, it is essentially floating periodically. Due to this floating node glitches may appear at the output. CDMFF annihilate CDFF in terms of power consumption and speed [10]-[11].

## D. Clock Pair Shared Technique

Clock pair shared flip-flop [12]-[13] avoids floating node problem as well as reduce the number of clocked transistors in CDMFF. The floating problem is avoided by making the transistor P1 always ON which is used to charge the internal node X. The circuit operates when clk and clkdb are at HIGH. When D is High, Q is low and Qb is high which makes N5 to be OFF and N1 to be ON. The ground voltage will pass through N1, N3 and N4 then the node X discharges. As the node discharges, the output Q pulls up through P2 as it is in ON state. When the output is at high and D is at Low, N5 and N2 are ON and N1 is OFF, then Q output is pull down to LOW through N2, N3 and N4. The flip-flop output is depending on previous output Q and Qb\_kpr in addition with clock and data input.

## E. Clock Pair Shared Flip-Flop using MTCMOS

As the technology scales down supply voltage has been scaling down as a result performance degrades. To increase performance, threshold voltage has to be scaled down which leads to increase in leakage current. Hence, static power consumption is expected to exceed switching portion of power consumption. Multi threshold CMOS [14]-[17] is a technique used for leakage current. The circuit comprises of two different set of transistors one which works on High  $V_t$  are termed as "sleep" transistors and the transistors which works on Low  $V_t$  comprises the logical circuit. The sleep transistors are used to achieve high performance by reducing the leakage current while the Low  $V_t$  transistors enhance the circuit's speed performance.

Clock pair shared flip-flop using MTCMOS [17] is designed for reducing the standby leakage power consumption and switching activity. The high threshold voltage NMOS transistor is controlled by sleep signal. The circuit operation is similar to CPSFF during active mode. During sleep mode, there is no discharging path for node X as the M7 is off. Thus the leakage power can be reduced.

## III. PROPOSED DUAL EDGE TRIGGERED CPSFF USING MTCMOS

Conventional DEFFs requires more area and load on the inputs. Explicit pulsed DEFFs use external clock pulse generators, which increase the power. To reduce clock load, clock branch sharing topology is used to ensure efficient implementation of double-edge clock triggered flip-flop in implicit manner.

MT-DETCPSFF is shown in Fig. 1. The transistors (N4, N6), (N5, N7) are shared by the first stage and second stage. The advantage of this sharing concept is the number of transistors gets reduced. Only a small amount of short circuit current yields because, the discharging path will be ON for a short interval. Figure 1 illustrates the schematic diagram of dual edge triggered D- flip flop using multi threshold CMOS technology.

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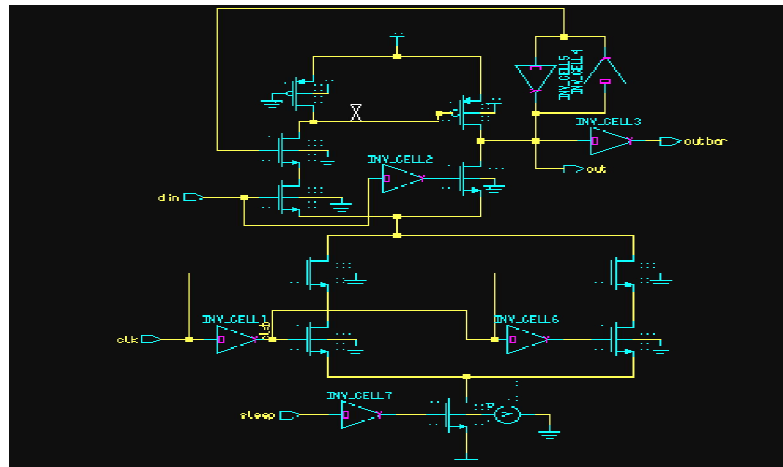


Fig 1: Schematic of MT-DETCPSFF

The circuit operates in normal mode when the sleep signal is active. N7 is controlled by Q\_fdbk signal. When CLK is high, CLKB will be high for a short interval of time equal to one inverter delay. During this period, (N4,N6) branch will be on and the other clocked branch (N5,N7) is disconnected. When CLK is low, CLKB will rise after one inverter delay, and CLKB\_delay will stay high for a period of two inverter delays during which the transistors N5 and N7 are both on. Consider the initial values of Q and Q\_fdbk are 0 and 1. When the input is high then the internal node X gets discharge through N1,N3,N4,N6 and sleep transistor and the outputs Q and Q\_fdbk becomes high and low. During the next interval, N1 is off as a result the first stage is disconnected from ground preventing node X to undergo redundant switching activity. When the input becomes low the second stage will be on and making the output to discharge. So that, Q and Q\_fdbk will be 0 and 1.

At node X the capacitance is much smaller than that on node Q, which causes a significant difference in propagation delay through the flip-flop. The delay is further reduced by placing inverters I1 and I2 at the bottom to drive N6 and N7. The reason is they make clock branch transistors to be on during the rising and falling clock edge. Also, making the nodes A, B to discharge before the evaluation period occurs. Hence this DETCPSFF using MTCMOS is used for high speed applications. During sleep mode of operation the sleep transistor is off as a result the leakage power gets reduced as it is not directed to ground.

## IV. SIMULATION RESULTS

The simulation results of proposed flip-flop are shown. The circuit is drawn and simulated using MENTOR GRAPHICS Pyxis Schematic Editor tool and the technology used here is 130nm. Table 1 illustrates the power consumption comparison of various flip-flops at different supply voltages and at 500MHz and 750MHz frequencies. Table 2 illustrates the delay analysis, switching activity and area for different flip-flops at 1.5V supply voltage and 500MHz frequency. Figure 2 describes the simulation results of dual edge triggered D- flip flop using multi threshold CMOS technology.

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Table 1: Power Consumption Comparison for Various Flip-Flops

Design Name	Frequency					
	500MHz			750MHz		
	Power Consumption(mw)			Power Consumption(mw)		
	Supply Voltage( $V_{dd}$ )					
	1. 5V	2.5V	3V	1.5V	2.5V	3V
DEFF	1.7	173.3	306	1.8	175.6	310
CDFE	0.075	0.246	0.394	0.099	0.322	0.516
CDMFF	0.026	0.131	0.217	0.028	0.184	0.262
CPSFF	0.016	0.048	0.072	0.021	0.066	0.090
MT-CPSFF	0.012	0.037	0.054	0.016	0.046	0.068
MT-DETCPSFF	0.049	0.148	0.220	0.066	0.196	0.291

Table 2: Delay Comparison for Various Flip-Flops

Design Name	Area (No. of Transistors)	Switching Activity	Delay (ns)
DEFF	24	12	30.2
CDFE	26	13	19.89
CDMFF	20	7	9.74
CPSFF	17	4	1.94
MT-CPSFF	21	4	1.15
MT-DETCPSFF	24	8	0.66

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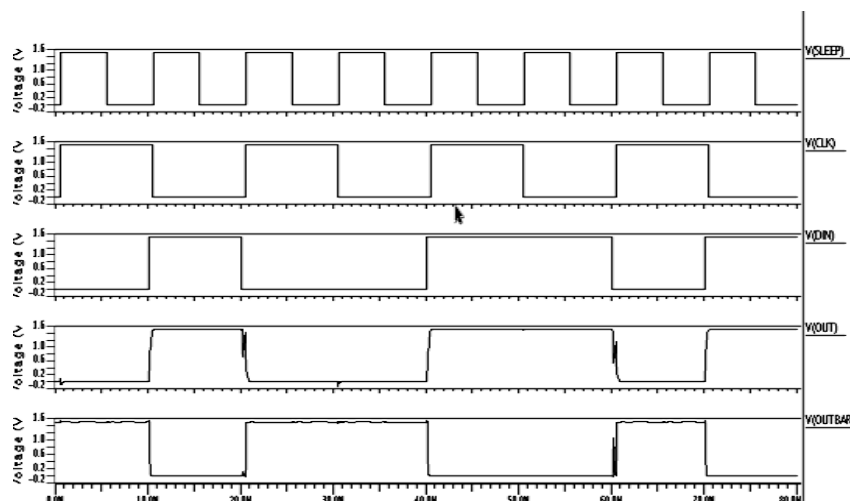


Fig 2: Simulation result of MT-DETCPSFF

## V. APPLICATION

### A. Jhonson Counter

Jhonson counter is also known as twisted ring counter, and is exactly same as ring counter except that the inverted output of the last flip-flop is connected to the input of the first flip-flop. Figure 3 illustrates the schematic diagram of 2- bit Jhonson counter using proposed flip-flop. Figure 4 illustrates the simulation results 2- bit Jhonson counter .

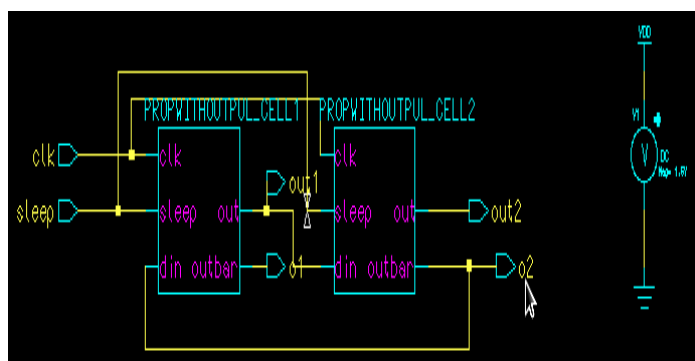


Fig 3: Schematic of 2-bit Jhonson Counter

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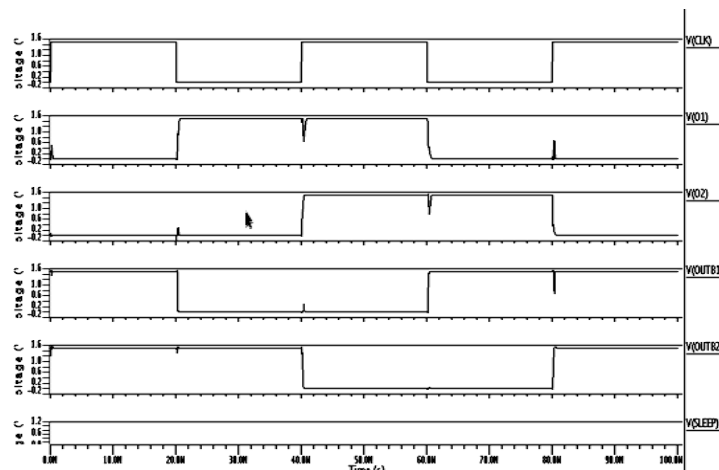


Fig 4: Simulation result of 2-bit Johnson Counter

## VI.CONCLUSION

In this paper, high speed flip-flop is designed and verified in Mentor Graphics Tool. The power parameter is analysed at 500Mhz and 700MHz frequency and at various supply voltages. Also, various flip-flops are compared and observed that proposed design has less delay and hence used in high speed applications. The proposed flip-flop is used to design counters, linear feed back shift registers etc.

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