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Design of a Low Power 10T SRAM Cell

R. K. Sah, M. kumar²

P.G. Student, Department of ECE, NERIST, Nirjuli, Arunachal Pradesh, India¹

Assistant Professor, Department of ECE, NERIST, Nirjuli, Arunachal Pradesh, India²

ABSTRACT: SRAM is a semiconductor memory cell. In this paper, a 10T SRAM cell is designed by using cadence virtuoso tool in 180nm CMOS technology. Its performance characteristics such as power, delay, and power delay product are analysed. 10T SRAM cell is basically 6T SRAM cell with 4 extra transistors. In this 10T SRAM cell, additional read circuitry is attached to avoid flipping of cell. The power dissipation, delay, and power delay product of the designed 10T SRAM cell in 180nm CMOS technology are found to be 22.08×10^{-9} W, 39.95×10^{-9} s and 0.8820×10^{-15} Ws respectively.

KEYWORDS: Power, Delay, Power Delay Product, 10T SRAM cell.

I. INTRODUCTION

SRAM is semiconductor memory cell. It stores one bit of information. It is faster and consumes very less power as compared to other memory cells. Due to its robustness and stability, researchers are interested in further improvement of SRAM cell. SRAM is vital component in a chip or microprocessor IC. Designing a SRAM cell in nanoscale regime has become a challenging task because of reduction in noise margins and increased sensitivity to threshold voltage variation [1]. 10T SRAM cell performs better than 6T SRAM cell in terms of reliability and stability. 6T SRAM cell has less reliability at low supply voltage due to degradation in noise margins [2].

II. RELATED WORK

Conventional 6T SRAM cell consists of six transistors. Fig. 1 shows the conventional 6T SRAM cell [3]. Transistors N2 and N3 are access transistor, while remaining four transistors: N1, N2, P1 and P2 form two inverters. These two inverters are used to latch data. The data enters into latching inverter through access transistor. The process of introducing a data is known as write operation and retrieving a data is known as read operation. Word line (WL) selects a row of SRAM cell. Bit line (BL) and bit line bar (BLB) are used to select a column of SRAM cell. When both WL and BL are ON, a particular SRAM cell is selected [3-5]. A 10T SRAM cell can be designed by using a conventional 6T SRAM cell and an additional read circuitry.

In this paper, a 10T SRAM cell is designed by using cadence virtuoso tool in 180nm CMOS technology and its performance characteristics such as power, delay, and power delay product are analysed.

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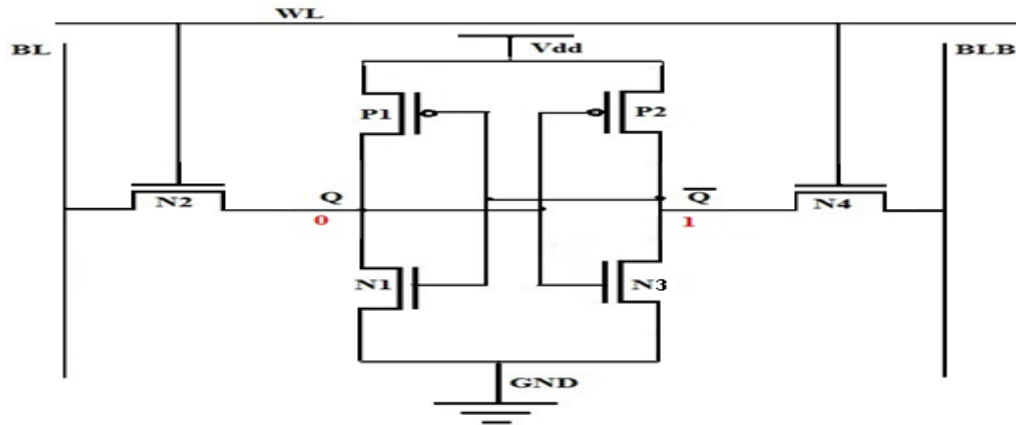


Fig.1. A 6T SRAM cell

III. DESIGN AND SIMULATION OF A 10T SRAM CELL

The architecture of a 10T SRAM cell is similar to the 6T SRAM cell except additional read circuitry [6]. Fig. 2 shows the designed 10T SRAM cell. In this 10T SRAM cell, 10 transistors have been used. It consists of conventional 6T SRAM cell and an additional read circuitry. Difficulty in conventional 6T SRAM cell is the high risk of data loss during read operations. There is possibility of flipping node voltage at Q and Q' due to back to back inverter actions. This situation can be avoided using extra read circuitry. In this 10T SRAM cell, write operation is same as in 6T SRAM cell [6-7]. In case of read operation, charge sharing takes place between read bit line (RBL) and uncharged bit line BL / BLB during read operation. Due to sharing of charge, read bit line does not discharge completely and stay at mid voltage level. Hence this cell behaves as an automatic bit line swing limiter.

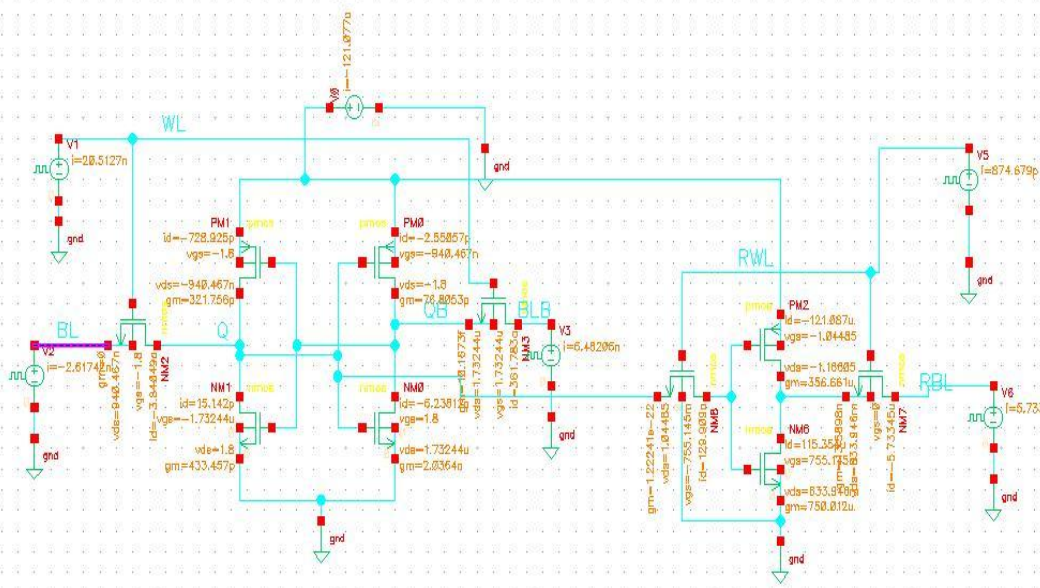


Fig.2. Design of a 10T SRAM cell

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Fig. 3 shows the waveform of the designed 10T SRAM cell. BL is having a time period of= 40ns and WL is having period of = 20ns. Third line shows the stored value at node Q and the fourth line shows the voltage at node QBAR. Table 1 shows power, delay, and power delay product of the designed 10T SRAM cell in 180nm CMOS technology. This table shows that the power dissipation, delay, and power delay product of the designed 10T SRAM cell are 22.08×10^{-9} W, 39.95×10^{-9} s and 0.8820×10^{-15} Ws respectively.

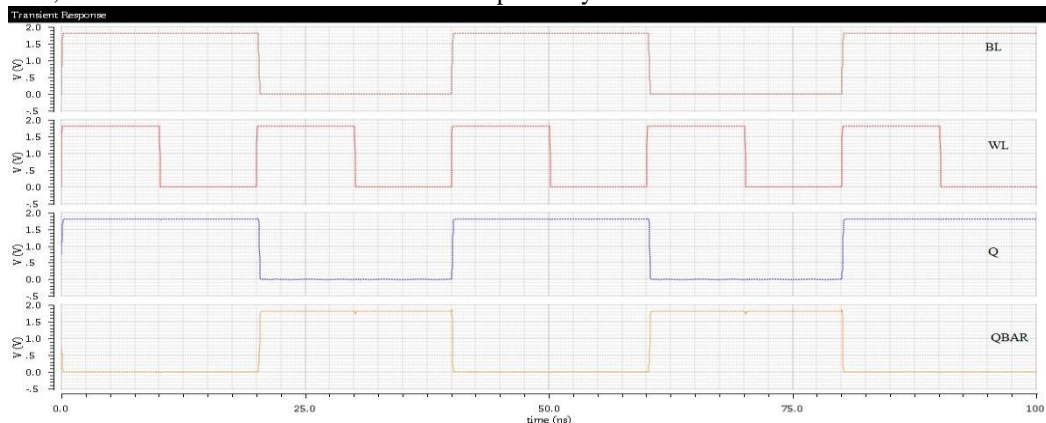


Fig.3. Waveform of the designed 10T SRAM cell

Table 1. Power dissipation, delay and power delay product of the designed 10T SRAM cell

Power	Delay	Power delay product
22.08×10^{-9} W	39.95×10^{-9} s	0.8820×10^{-15} Ws

IV. CONCLUSION

The 10T SRAM cell is designed in cadence virtuoso in 180nm CMOS technology and its performance characteristic has been analyzed. The designed 10T SRAM has write capability as good as 6T SRAM and improved read stability than 6T SRAM cell. The power dissipation, delay, and power delay product of the designed 10T SRAM cell are 22.08×10^{-9} W, 39.95×10^{-9} s and 0.8820×10^{-15} Ws respectively.

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