

Design of Low Power High Speed Adders in McCMOS Technique

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ABSTRACT: Adder are the core component of processors and digital design architecture. Also, not only addition, but performs many other arithmetic operations such as subtraction, division and multiplication. The focus of VLSI technology is to reduce power consumption, enhancing the performance and speed of a digital circuit. Less power consumption is the ultimate attention for any computation. In this paper, 16 bit adders are designed using one such technique i.e. McCMOS and compared for power dissipation, delay, leakage power and power delay product. Different types of adders have been designed using Multiple channel CMOS (McCMOS) technology and compared with conventional with 45nm technology. The simulation result shows that the average power reduces to 30 – 35% less and PDP is reduced to 15- 17% than the power and PDP of the conventional CMOS. Hence the technique can be used for low leakage high speed application. The simulation has been carried out in tanner tool EDA 14.1 with 1V power supply.

KEYWORDS: Carry Save Adder, Carry Select Adder, McCMOS, ALU (Arithmetic logic Unit).

I. INTRODUCTION

Adders are the key components in any arithmetic operation calculation. There are some more operations such as subtraction, division and multiplication which are addition based arithmetic circuits. Adders and multipliers are the most significant part of all data path circuits in digital signal processors and microprocessors. Multiplication process need adders, for the addition in the final step [7]. So it is very clear that the performance of multiplier is totally depends on the performance of the addition i.e. adders. Hence the optimization of the adders will affect the constraints (power, delay, pdp) of the multiplier.

The reduction of propagation delay and power dissipation are the primary concern in modern VLSI designs. This reduction can be done by an effective technique which reduces leakage power as well as average power and delay for the addition of binary numbers. This presented technique increase the speed of the adders. The scheme for controlling the leakage, McCMOS (multiple channel CMOS) [3] has been used to achieve optimized power and performance of the adders. Furthermore, an optimization in elementary unit which will further reduce the parameters of higher order units, for example multiplier. This paper proposed a modified binary adders such as carry bypass adders and carry select adder. The results shows a considerable improved performance is achieved by using McCMOS compare to conventional adder which uses CMOS style and contributes a better performance in applications. The structure of paper is as follows: section II shows the related work; section III presents basic leakage control using McCMOS; Section IV deals with the conventional CMOS adder; Section V describes the modified adders using McCMOS; Section VI encompasses simulation results; and section VII shows conclusion.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

II. RELATED WORK

The technology used in designing multipliers in this dissertation is McCMOS leakage control technique. Mark C. Johnson et al. proposed in [3] that a possibility of achieving an excellent leakage control by using non minimum transistor length. The analyses proves that, by factor 100 one can reduce the leakage, with very small increase in switched capacitance and area. The proposed technique reduce the leakage current much more than other costly technique without any need of bias control circuitry or process change. However minimum size feature continue to shrink to reduce the leakage. But even in case when the circuit is active, McCMOS is suitable to control leakage.

Multiplication generally required two basic steps such as generating partial products (PP) and summation of these partial products. Several multipliers are designed to improve the performance either by reducing the generated partial products or by using different schemes for summing PP. The chapter highlights some of the earlier designed adders and multipliers like array multiplier, Wallace multiplier, booth multiplier and Vedic multipliers and technique for optimizing.

J. Hazra et al. proposed an efficient technique to design a high performance two finite length sequence linear convolution using McCMOS technique [4]. A TG array based novel architecture had been proposed for the implementation of the partial products of multiplication given better performance in terms of speed & power. The result using this technique shows 77 – 97% PDP reduction than the conventional.

Diptendu Kumar Kundu et al. [7] designed a multiplier based on Vedic Multiplication “UrdhvaTiryakbhyam”. The Noise and power of 2x2 and 4x4 design had been calculated in Tspice-13 with 45nm technology. From the result it was concluded that the proposed multiplier is 18 times faster, two times area efficient, 181 less transistor required and 1.2 times area efficient from the conventional multiplier.

D. Kaya et al. [1] proposed 8x8 Vedic multiplication is proposed with the efficient leakage control technique using McCMOS at 130nm, 90nm, 65nm and 45nm node technology 1 V power supply. The simulation results of 8x8 Vedic multiplier UrdhvaTiryakbhyam using McCMOS technology show approx. 80% reduction in PDP then the conventional Multiplier. Moreover, McCMOS structure circuit are more efficient and high performance ultra-low power application. The delay of McCMOS UrdhvaTiryakbhyam Multiplier is about 73% - 90% less compare to conventional multiplier. Hence, the overall PDP reduced significantly as there was considerable reduction in delay, leakage power consumption and total average power consumption using proposed algorithm.

Radheshyam Gupta et al. described 16 bit Vedic multiplier using McCMOS technique at 45nm technology [9]. The Vedic Multiplier UrdhvaTiryakbhyam is approximately 10 times faster than the conventional multiplier. The simulation results shows 75% reduction in power delay product on comparing with conventional multiplier algorithm. The 1V power supply is used in simulation of the algorithm. Also, there was considerable reduction in power, delay, leakage power consumption and PDP.

III. McCMOS (MULTIPLE CHANNEL CMOS)

The Keeping in mind, the acceptable level down of heat dissipation and power, so to achieve high performance, around 1V low supply voltage and very short channel length is required for the maximum performance of any CMOS design. But this scaling, leads to low threshold voltage and cause increase in leakage current. Also this leakage current will increase the leakage power which is the major issue to be concern in deep sub-micron CMOS technology design. The MOS scaling technology depends on following parameters [8]

$$L_{min} = A[X_j t_{ox} (w_s + w_d)^2]^{1/3} \dots (1)$$

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

Here L_{min} is the minimum channel length, long channel subthreshold behaviour will be observed. Here 'A' is the proportionality factor, 'tox' is oxide thickness, 'Xj' is junction depth, 'wd' is source depletion depth and 'wd' is drain depletion depth in a one dimension abrupt junction formulation[5-6].

The parameters of MOSFET scaling is described as

$$w_d = \sqrt{2}L_B[B(V_{DS} + V_{bi} + V_{BS})]^{1/2} \quad \dots(2)$$

Where $L_B = \frac{\epsilon_s}{BqN_a}$ = Bulk Debye length And $B = (kT/q)^{-1}$,

L_B = Bulk Debye length And ,

V_{DS} = Drain to source voltage,

V_{BS} = Body to source reverse bias, and

V_{bi} = Built in voltage of the junctions.

The threshold voltage, short channel effect, current carrying ability, gate oxide, leakage current edge, and power supply are the important parameters which need to be concern in deep sub-micron designs. The possibility of achieving the tremendous leakage control is non minimum transistor length without the other accepted leakage current controlling technique disadvantage.

While lowing the supply voltage, threshold voltage will scale down in order to maintain the actual performance requirement. However such scaling increase the leakage current. A technique in this paper name as McCMOS, to achieve an improved leakage control together with optimized power and performance. The leakage power is controlled by using a non minimum transistor length of at least one transistor of the circuit in non critical path which results in increase in channel resistance, due to which leakage current reduces [1]. However, same technique is applied in critical path but here channel width increases for performance requirement.

In this paper, we use 45nm model file. To reduce the leakage current in non-critical path, non minimum length of nmos is used and for critical path, channel length is minimum but increasing the channel width of the pmos to satisfy performance. The figure 1 shows the inverter with McCMOS technique.

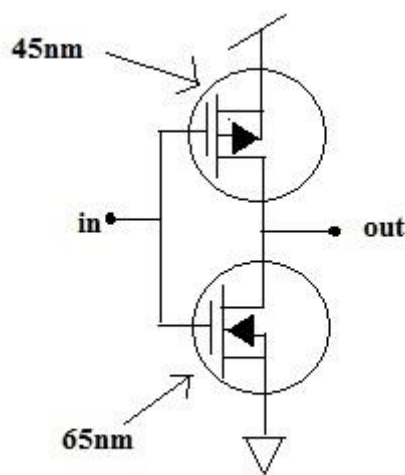


Figure 1: McCMOS Inverter

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IV. CONVENTIONAL ADDER ARCHITECTURE

The simple binary addition usually carried out using full adder. However, if we add multiple bits then the easier method is to connect full adder in series. The technique use for adding multiple bit is defined as adders. RCA (ripple carry adder) is most common among the adders, although implementation of this adder for small length is effective. But, most desktop computers now a days using word length of 32 bit, while server require 64 bit; and the fast computer, such as super computers, mainframes etc., require word length of up to 128 bits. The overall performance limit by the adder's computational time. And the dependence of this computational time is on number of bits of the adder. Many such architecture are proposed to eliminate or reduce the proportional dependency. This section describes the conventional adders.

4.1 Carry Select Adder

Carry select adder is fastest and conditional sum adder used for many processors for fast arithmetic computation. In carry select adder several group of addition are performed, two addition are performed parallel using double RCA. One evaluate the result with carry '1' and other evaluate with carry '0' [2]. Once the input carry is computed, the output sum and output carry C_{out} is selected by the multiplexer. From the circuit point of view, two carry result is generated. Although this adder increase the number of units. But its computation is much faster than usual computation. Figure 2 shows 4 bit carry select adder. The 16 bit Carry select adder is constructed by cascading a number of equal length adder stage.

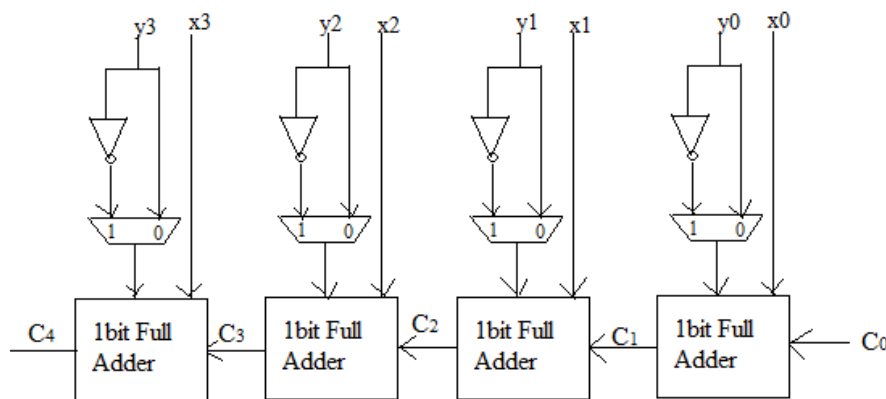


Figure 2: 4 bit Carry Select Adder

4.2 Carry Save Adder

Carry save adder is a 1bit full adder without having any carrying chain. The n-bit CSA have three n-bit inputs and two n-bit outputs i.e. $sum(n-1) \dots sum(0)$ and $cout(n-1) \dots cout(0)$. The main advantage of CSA adder is to calculate partial products in multiplication. The architecture of carry save adder allows the tree style of adding to calculate partial products. The figure 3 shows the carry save adder. Usually, ripple carry adder is used to calculate parameter but it consume more power and large delay which need to be concern for high speed adder.

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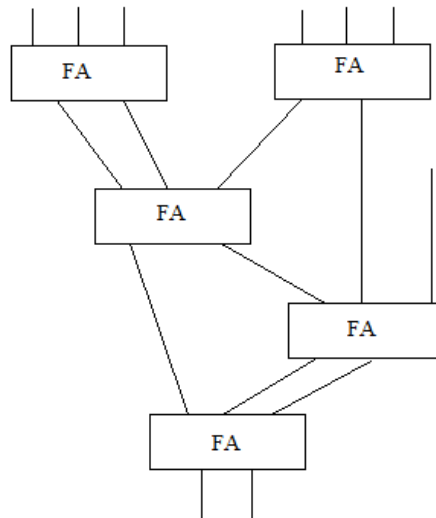


Figure 3: Carry Save Adder

V. MODIFIED ADDER ARCHITECTURE

5.1 Modified Carry Select Adder

Because of the dual ripple carry adder more area is required and carry out stage ripple at each stage. Considering the block of an adder, adding bits K to $K+3$. Instead of waiting for previous carry to come and then compute the computation further, there are two possibilities generated. First, if input carry is '0' and other if input carry is '1', which means two path of carry need to implement. When either the result are decided then the path is selected using multiplexer. The figure 4 shows the 16bit modified carry select adder with dual carry look ahead adder. Propagation delay for the worst case of the unit is

$$t_{add} = t_{setup} + Mt_{carry} + \left(\frac{N}{M}\right)t_{mux} + t_{sum} \quad \dots(3)$$

Where N is number of bits and M is number of bit per stage. t_{setup} , t_{mux} and t_{sum} are fix delay. t_{carry} is delay through a full adder.

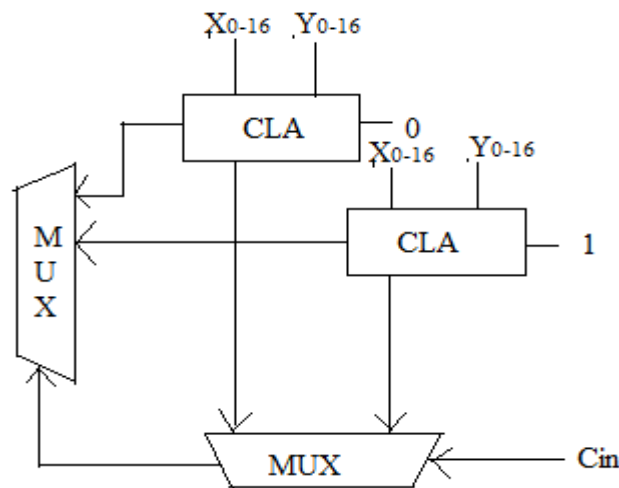


Figure 4: Modified Carry Select Adder

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5.2 Modified Carry Save Adder

The carry save adder have large number of critical paths, which degrade the performance of the architecture. An another modification to realize, to increase the performance of CSA is to move the carry diagonally downwards instead of rippling it to next 1 bit adder which is waiting for the previous carry to come and compute further. Hence, in this way carry is save for the next stage then immediately adding to the next adder. In the final stage, also in place of RCA another high speed adder can be used like Carry look ahead adder or carry select adder. The modified carry save adder is as shown in figure 5.

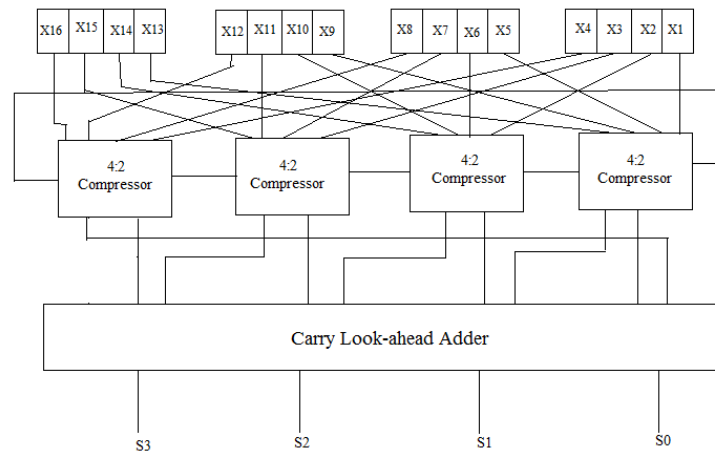


Figure 5: Modified Carry Save Adder

VI. SIMULATION RESULTS

The simulation results are carried out on 45 nm node technology at 1V using tanner tool. Adder using McCMOS have very low power consumption compare to conventional [4]. The overall decrease in PDP is 30 -33% of the adder. Table 1, Table 2 and Table 3 shows the comparative study of the 4 bit, 8 bit and 16 bit conventional McCMOS and Modified McCMOS, respectively. Comparing the average power and PDP of 4 bit CSAVE and CSELECT from figure 6 that CSAVE have very less power and PDP than CSELECT.

The simulation results of power and PDP is compared graphically for different bits 4, 8, 16 in figure 6, 7, 8 respectively

Table 1: Comparison of 4 bit Adders

Adder	Conventional CMOS				Modified McCMOS			
	Power (10^{-6} W)	Delay (10^{-8} sec)	PDP (10^{-13} J)	Transistor count	Power (10^{-6} W)	Delay (10^{-8} sec)	PDP (10^{-13} J)	Transistor count
CSAVE	4.90	2.05	1.00	264	4.18	2.04	0.852	264
CSELECT	8.55	2.04	1.74	288	5.25	2.05	1.08	288

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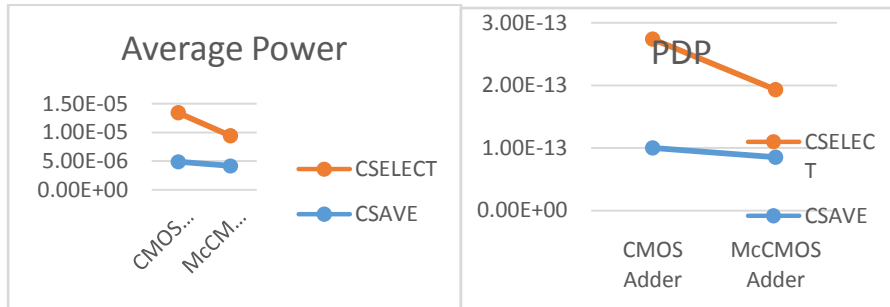


Figure 6: Comparison of 4 bit average power and PDP

Table 2: Comparison of 8 bit Adders

Adder	Conventional CMOS				Modified McCMOS			
	Power (10 ⁻⁵ W)	Delay (10 ⁻⁸ sec)	PDP (10 ⁻¹³ J)	Transistor count	Power (10 ⁻⁵ W)	Delay (10 ⁻⁸ sec)	PDP (10 ⁻¹³ J)	Transistor count
CSAVE	1.17	2.03	2.39	504	0.823	2.04	1.68	504
CSELECT	1.69	2.03	3.44	564	1.10	2.05	2.25	564

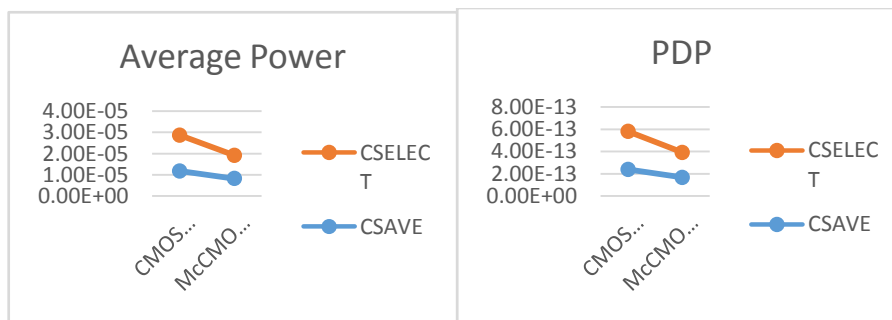


Figure 7: Comparison of 8 bit average power and PDP

Table 3: Comparison of 16 bit Adders

Adder	Conventional CMOS				Modified McCMOS			
	Power (10 ⁻⁵ W)	Delay (10 ⁻⁸ sec)	PDP (10 ⁻¹³ J)	Transistor count	Power (10 ⁻⁵ W)	Delay (10 ⁻⁸ sec)	PDP (10 ⁻¹³ J)	Transistor count
CSAVE	2.41	2.03	4.91	1008	1.67	2.04	3.41	1008
CSELECT	3.51	2.03	7.13	1128	2.23	2.05	4.56	1128

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

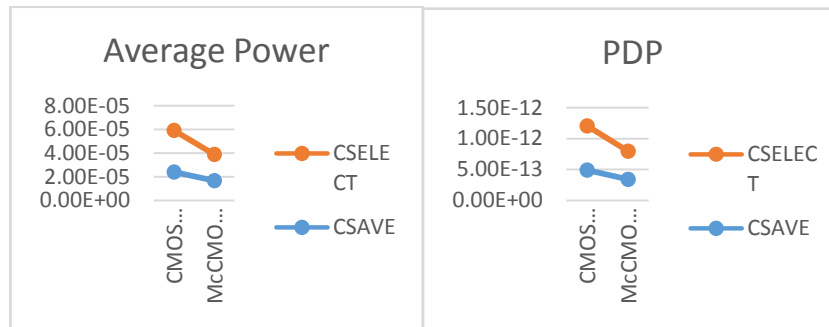


Figure 8: Comparison of 16 bit average power and PDP

VII. CONCLUSION

In this paper, we have design a high speed low power carry save adder and carry select adder using McCMOS technique. Different bits of adder has been designed and compare for the conventional CMOS and Modified McCMOS. Comparison shows that the average power reduces to 30 – 35% less and PDP is reduced to 15- 17% than the power and PDP of conventional CMOS. From table 1, table 2, and table 3 it is also clear that the number of transistor of CSAVE is much more less than CSELECT. Hence, the overall performance of the carry save adder is efficient with less power consumption and high speed

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