

# Low Power High Speed Complex Multiplier in 45nm Technology

Akanksha Goswami<sup>1</sup>, Rajesh Bathija<sup>2</sup>, Shikha Sharma<sup>3</sup>P.G. Student, Department of Electronics and Communication Engineering (VLSI Design), Geetanjali Institute of  
Technical Studies, Udaipur, India<sup>1</sup>Vice Principal, VCET, Jodhpur, India<sup>2</sup>P.G. Student, Department of Electronics and Communication Engineering (VLSI Design), Geetanjali Institute of  
Technical Studies, Udaipur, India<sup>3</sup>

**ABSTRACT:** Low power consumption and high speed with compact size in digital devices are foremost necessity of today. FFT algorithm places an essential role while composing digital signal processing. This paper includes compact design of complex multiplier used for FFT Design. Complex Multiplier is proposed for twiddle factor multiplication. The design based on distributed arithmetic, Urdhva-tiryakbyham multiplier, and carry-look ahead adders has been developed. The proposed design reduces complexity in multiplication which occurs during FFT operation. The work includes simulation and verification of respective multiplier in 45 nm scale using tanner tool version 14.11.

**KEYWORDS:** Complex multiplier, CMOS, DFT, FFT, Urdhva Tiryakbhyam Multiplier

## I. INTRODUCTION

As we represent signal in form complex number, thus operation on these complex numbers is prime requirement. Since this type of multiplication is quite frequent in much application, hence in this paper the implementation of high speed and low power complex multiplier is shown. Complex multiplication design can be the most time and area-consuming operations in a digital signal processing. Thus implementing less number of multipliers in the design is the great need in order to enhance the speed. A compact complex multiplier has been proposed which can be used in high speed FFT implementation. Complex number multiplication is performed using three real number multiplications and five additions/ subtractions. This paper shows a complex multiplier with reduced number of multipliers which increases the speed of operation with low power consumption. This complex multiplier uses Urdhva Tiryakbhyam vedic Multiplier for multiplication which also supports in enhancing speed.

Vedic Mathematics is the ancient system of Indian mathematics which has a exclusive technique of calculations based on 16 Sutras. Various multiplication schemes had been designed to increase the efficiency of the multiplier in algorithmic and structural levels, which confronts the reduction of the partial products and the methods for their partial products addition, but the idea behind multiplication was same in all cases. Many multiplier design using "Urdhva-tiryakbyham" sutras, has been proposed which was adopted from the Vedas.

Using Vedic mathematics, an N bit complex number multiplication was characterised into three multiplications for real and imaginary final products. This sutra is employed for the multiplication, with less partial products, as compared with array based multiplication. Transistor level implementation for power leakage, delay, and power consumption calculation of the proposed design was evaluated by tanner tool version 14.11 using 45 nm CMOS technology and compared with the other design like distributed. Our work resulted in simplified mathematical operations, in comparison with the direct method or the strength reduction technique.

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## II. RELATED WORK

1. Various complex Multiplier has been published in many research papers with with more number of Multipliers on various performance factors like speed, power, delay.
2. The possible structure having high performance must have low area and complexity. Complex multipliers Implementation Process can be speed up by reducing complexity and area.
3. Here required improvements are shown on the reported structures to obtain the high performance of the proposed FFT structure.

## III. IMPLEMENTATION

The complex multiplier implementation includes real part and imaginary part.

$$(a+jb)(c+jd) = x+jy, \quad (1)$$

Where  $a+jb$  is first complex number and  $c+jd$  is the second complex number and,

$$x = ac-bd, \text{ and } y = bc+ad \quad (2)$$

$$\text{Real part, } (a+b) c - (d+c) b \quad (3)$$

$$\text{Img Part, } (a+b) c - (c-d) a \quad (4)$$

Thus algorithm for complex number multiplication shows two separate final results to calculate real and imaginary part. The real part of the output can be computed using  $(ac - bd)$ , and the imaginary part of the result can be computed using  $(bc + ad)$ . Thus four separate multiplications and addition/subtraction are required to produce the real as well as imaginary part numbers. But in order to reduce multiplication, equation (2) is further simplified as in equation (3) and (4). This reduces the multipliers from four to three and hence the overall speed of multiplier is enhanced.

## IV. COMPLEX MULTIPLIER USING VEDIC MULTIPLIER AND ADDER.

Multiplication is a very important part in complex multiplier design. The multiplication design based on vedic sutra Urdhva Tiryakbhyam and carry look ahead adders, gives the efficient performance of multiplier. The Complex multiplier method as shown in fig 1 designed using this vedic multiplier has high speed as well as low power consumption.

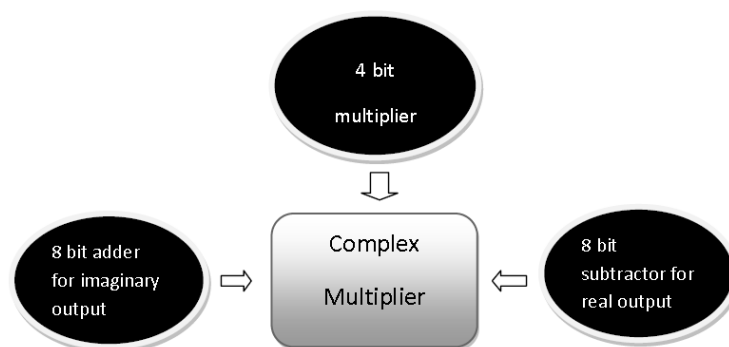


Fig 1: Complex number multiplication method

### A. Urdhva Tiryakbhyam Multiplier

The complex multiplier includes multiplication using Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. The Sanskrit term means “Vertically and crosswise”. Urdhva Tiryakbhyam is used in various multiplication techniques. Here the partial products are generated along with addition of these in parallel. The concept of parallelism in generation of partial products and their addition is calculated using Urdhva Tiryakbhyam explained in Fig. 2.

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## B. Carry Look Ahead Adder

In order to reduce the time taken to propagate the carry, the carry look-ahead adder is implemented by calculating the carry signals first, based on the input signals. The 4-bit Carry Look Ahead adder block diagram is shown in Fig. 3. The Boolean expression of a full adder is redesigned for designing carry look ahead adder. The Propagate P and generate G in a full-adder is:

$$P_i = A_i \oplus B_i \quad \text{Carry propagate}$$

$$G_i = A_i \cdot B_i \quad \text{Carry generate}$$

The sum output and the carryout came out as:

$$S_i = P_i \oplus C_{i-1}$$

$$C_{i+1} = G_i + P_i C_i$$

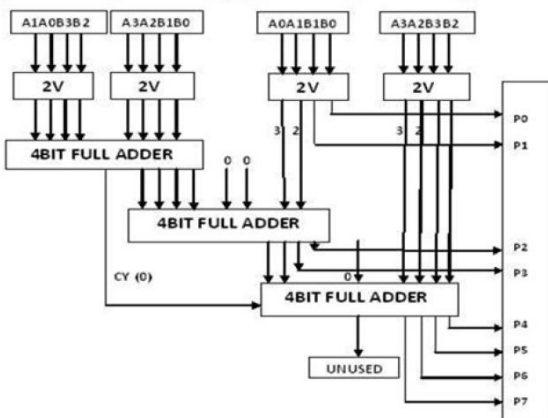
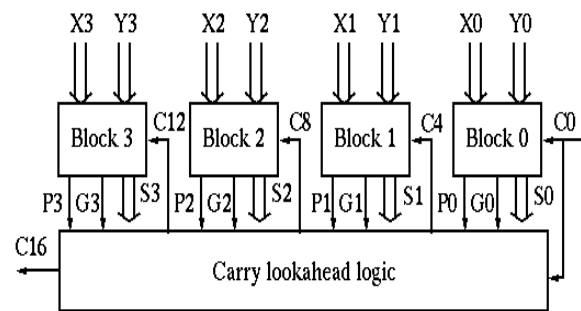


Fig 2: 4x4 Urdhva Tiryakbhyam Multiplier



Figs 3: Carry Lookahead Adder

## V. PROPOSED COMPLEX MULTIPLIER

The proposed Complex Multiplier is shown in Fig 4 and is designed using equation 3 and 4.. The design is used for complex multiplication with twiddle factors. It provides the real and imaginary output respectively. The design includes Urdhva Tiryakbhyam Multipliers, Carry Look ahead adder and subtractor units. Obviously, using this scheme, the design has some advantages. The number of multiplications is reduced from four to three by manipulating the equation (2).

And addition has less consumption of power than multiplication, which in turn reduces overall power consumption of design.

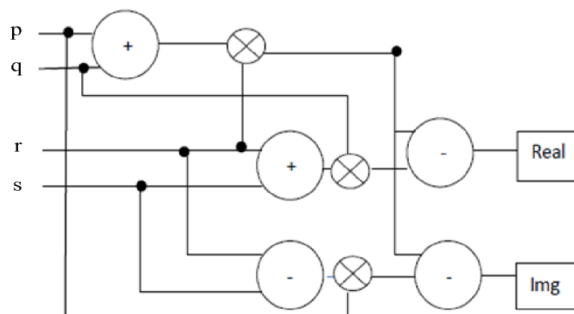


Fig 4: Complex Multiplier Design

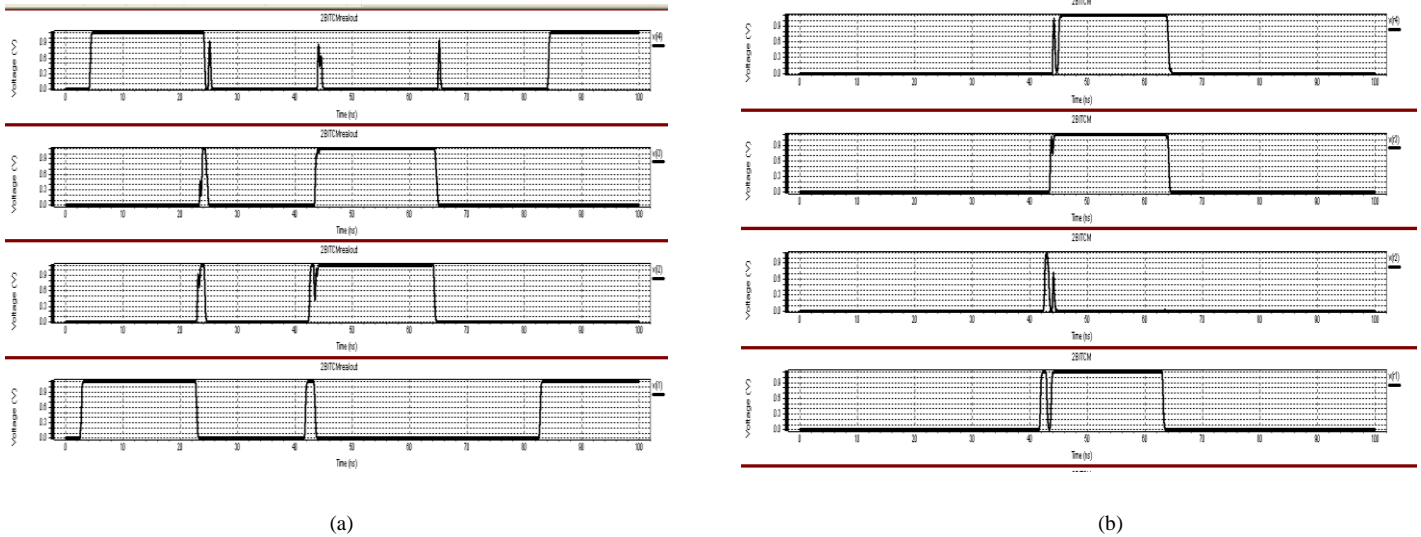


Fig 5: Schematic of Complex Multiplier Design (a) 2bit (b) 4 bit

**V.DESIGN RESULTS**

The proposed Multiplier is designed on 45nm scale and reduces the complexity of multiplication. Fig.5 shows the schematic of the described design.

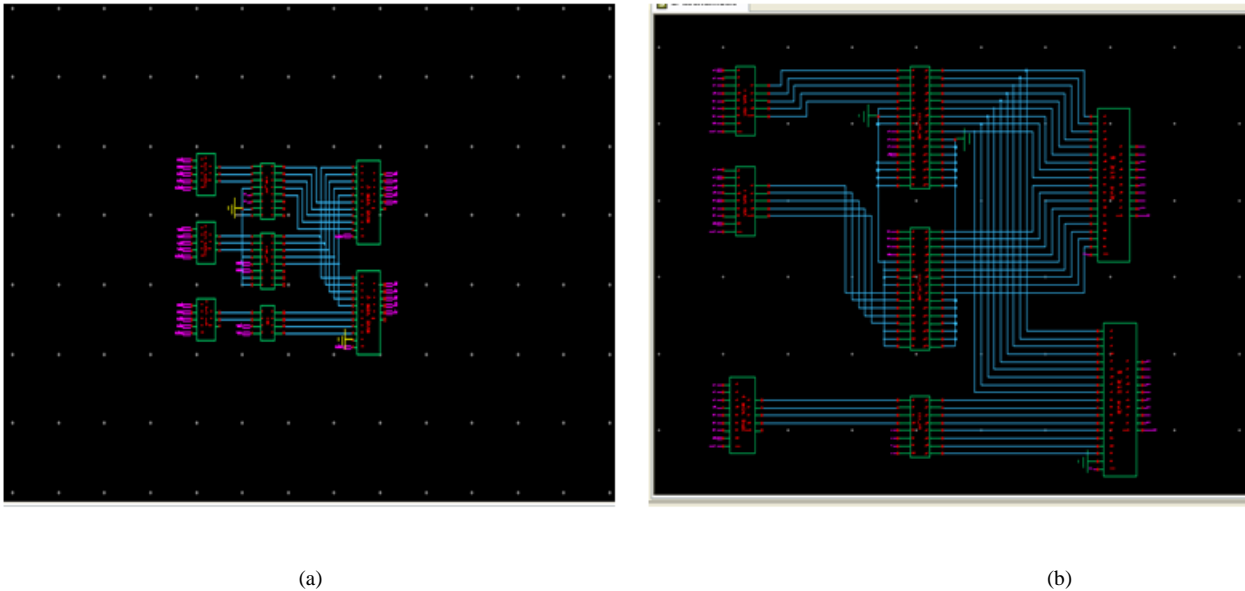


Fig 6: Waveform of Complex Multiplier Design (a) Real outputs (b) Imaginary Outputs

Fig 6 (a) and (b) are the real and imaginary waveforms results of the proposed multiplier. This provides less delay of  $2.2 \times 10^{-8}$  ns and power consumption of 0.026mW - 0.4mW which is quite efficient. Figure 7 shows the power delay product of 2 bit and 4 bit of proposed multiplier.

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Multiplier	Power	Delay	PDP
2 Bit	0.026mW	2.2x10 <sup>-8</sup> ns	5.72x10 <sup>-11</sup> n
4 Bit	0.4mW	2.2x10 <sup>-8</sup> ns	8.8x10 <sup>-11</sup> n

Table 1: Power delay product (PDP) of 2 bit and 4 bit multiplier

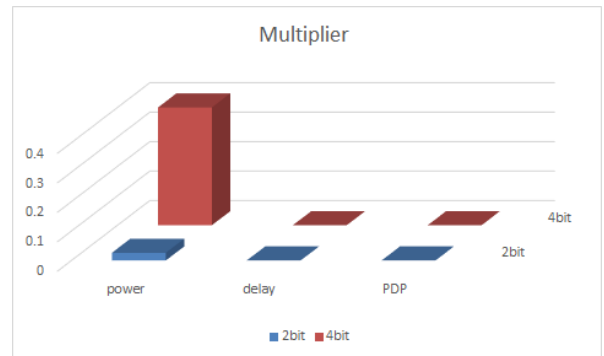


Fig 7: Power Delay Product (PDP) of Proposed Multiplier

## VI.CONCLUSION

Simulation results shows proposed Complex Multiplier represents a better and efficient architecture with delay of  $2.2 \times 10^{-8}$  ns with less power usage of 0.026mW - 0.4mW, which in turn has reduced power delay product for computing FFT. Thus the overall speed of the design is increased. This is due to simplification of the mathematic equations in Multiplier Structure. This can provide the better computation of FFT design.

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