

Design of a High Frequency Dual Modulus Prescaler using Efficient TSPC Flip Flop using 180nm Technology

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ABSTRACT: A high speed efficient TSPC flip-flop divide-by-16/17 dual modulus prescaler is proposed. The efficient (proposed) TSPC flip-flop with split path not only reduces the clock load and decrease power but also increases the speed of operation. The speed of the precaler can improve in two aspects. First is by adopting a new pseudo divide-by-2/3 prescaler, the minimum working period is reduced by half a NOR gate's delay. Second is by changing the connection of TSPC D-Flip-flops, the minimum working period is reduced by half an inverter's delay. The proposed circuit is capable of operating up to 1.8GHz and is implemented in 5V, 0.18um CMOS technology. Simulations and designs are performed on Cadence Virtuoso and Spectre tools using UMC 0.18um technology.

KEYWORDS: Dual-Modulus Prescaler, efficient TSPC, divide-by-2/3, divide-by-16/17 prescaler.

I.INTRODUCTION

Dual-modulus frequency prescaler plays an main role in phase-locked loop (PLL) designs[1]. In spite of fact that current-mode logic and inject locking prescaler can provide working frequency of hundreds/tens GHz with process of SoI CMOS or InP DHBTs and so on. TSPC dual-modulus prescaler is greatly utilized in several GHz with standard CMOS process[2],[3]. TSPC prescaler has the merits of single clock phase, low power, small area, and large output swing. Speed improvement is an important design issue for TSPC prescaler. In addition to the above, several techniques have been developed. At the transistor level decreasing the threshold voltage of nMOS transistors, forward body biasing technique can improve the speed, but it suffers from increased cost and decreased robustness as well as high minimum working frequency[4]. At the gate level, by adopting E-TSPC(extended-true single phase clock) flip-flops can effectively improve the operating speed performance. But the serious is current leakage, thus the performance of the minimum working frequency is limited. At the RTL level, speed improvement of divide-by-2/3 prescaler can also increases in improving the speed of divide-by-16/17 prescaler. However, several TSPC circuit design rules are broken in these paper. It mainly leads to shrinking the range of frequency because these prescalers are not suitable for low frequency operation for longer time.

In recent days, both the divide-by-2/3 and divide-by-4/5 prescaler are most widely utilized. Usually, divide-by-2/3 prescaler has the advantage of speed more than divide-by-4/5 and these prescaler is much more power efficient also. Thus, divide-by-2/3 prescaler is preferred in 16/17 prescalers[5]. On the other hand, divide by 4/5 prescaler is preferred in large division ratio, such as 128/129 prescalers and it helps to minimize the critical path and is more preferred. In this brief, two aspects can improve the maximum working frequency of the divide-by-16/17 prescaler. First, develop a new pseudo divide-by-2/3 prescaler and adopted into the divide-by-16/17 prescaler, which leads to reduce the minimum working period by half a NOR gate's delay. Second, the minimum working period is further reduced by half an inverter's delay, by changing the connection of efficient TSPC D-flip-flops (DFFs). D-flipflop is the data flipflop transfers the data without any flipping.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

II. RELATED WORK

A low-power true single-phase-clock (TSPC) based domino logic circuit design. Compared to using three clock transistors in the conventional TSPC-based scheme, the proposed circuit only requires two transistors. As a result, the clock load capacitance is reduced, leading to low power consumption in the clock distribution network. A keeper design to solve charge sharing is also demonstrated. Simulation results using 90nm and 45nm CMOS technologies are provided and discussed, respectively, which illustrate power saving as compared to conventional design not only when the input logic is active but also when the input logic is held to zero.

Two dynamic circuit techniques, raising only a single-phase clock which is never inverted[6]. This class of circuits has the advantages of simple clock distribution, small area for clock lines, reduced clock skew problems, and high speed. Several examples are demonstrated.

Implementation of a dual modulus prescaler using an extension of the true-single phase-clock (TSPC) technique, the extended TSPC (ETSPC), is presented. The E-TSPC consists of a set of composition rules for single-phase-clock circuits employing static, dynamic, latch, data precharged, and NMOS-like CMOS blocks. The composition rules, as well as the CMOS blocks, are described and discussed.

II. TPC D-FLIPFLOP

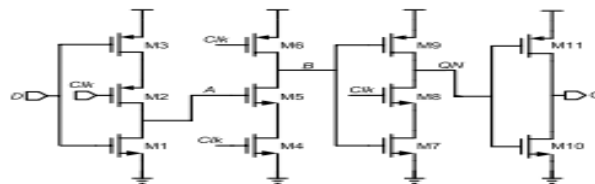


Fig 1.structure of TSPC DFF.

Fig1.shows a popular structure of TSPC D-flipflop. The circuit consists of blocks called n-blocks and p-blocks of four alternating stages. Single clock signal drives the each block. In this design single global clock signal is generated and distributed in order to simplify the design[7]. fig.1 shows the schematic of TSPC D-flip flop consists of 11 transistors, this positive edge triggered flip flop uses just a single clock signal for synchronization. During the ON period of clock whatever is the value of input it will become's an output.

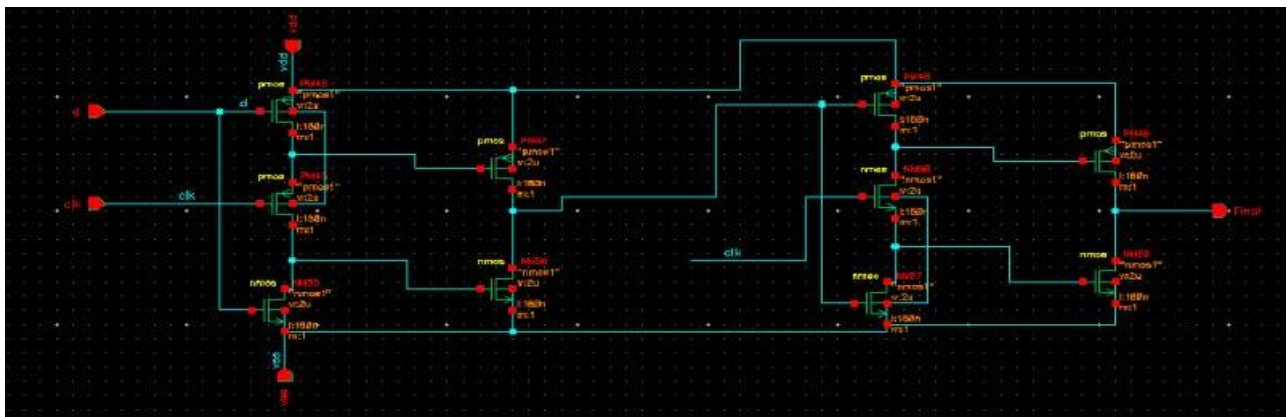


Fig 2: structure of proposed TSPC DFF.

International Journal of Innovative Research in Science, Engineering and Technology

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Now another design of TSPC D-flipflop with 10 transistors is shown in fig2, which consumes less number of transistor's and area compared with previous one and it also reduces power consumption. The proposed TSPC with split path not only reduces the clock load and decreases power but also increases the speed of operation. The true single-phase clock(TSPC)is common dynamic flipflop which performs the flipflop operation with little power and at high speeds. The setup time of the TSPC DFF can be written as

$$t_{setup} = t_{D-A} \dots\dots\dots(1)$$

Where t_{D-A} means the propagation time from node D to node A, which is a clocked inverter's delay. The propagation delay of the TSPC DFF can be written as

$$t_{D-QN} = t_{A-B} + t_{B-QN}$$

$$t_{D-Q} = t_{A-B} + t_{B-QN} + t_{QN-Q} \dots\dots\dots(2)$$

where t_{D-QN} and t_{D-Q} are the propagation delay from CLK to QN and Q, respectively. t_{A-B} , t_{B-QN} , t_{QN-Q} represents the propagation delay from node A to B, B to QN, and QN to Q, respectively.

III. CONVENTIONAL DIVIDE-BY-16/17 DAUL MODULUS PRESCALER

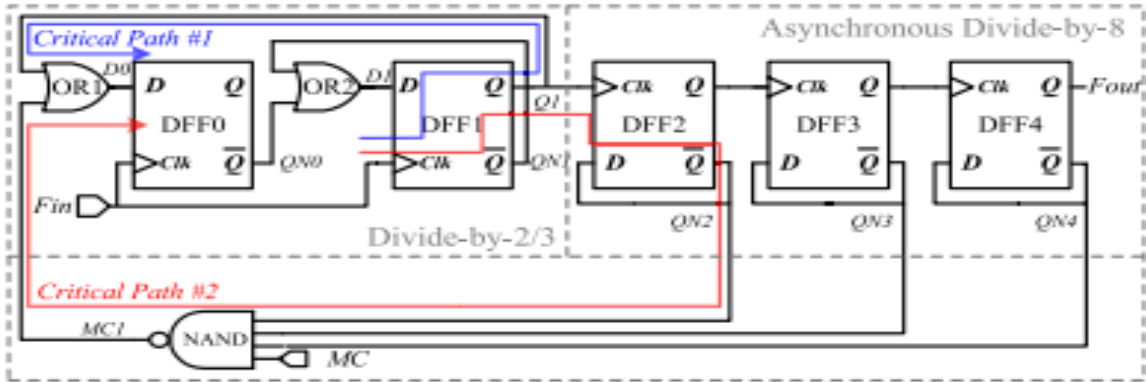


Fig 3: structure of Conventional divide-by-16/17 prescaler

Fig.3 shows the schematic of a conventional divide by 16/17 prescaler. These prescaler is designed based on a divide-by-2/3 prescaler. It consists of a divide-by-2/3 prescaler, an asynchronous divide by 8 divider, four input NAND gate and a two OR gates. It has two critical paths.

First, critical path#1(Q1 path) comes through D-FF1 and OR1.

Second, critical path#2(MC1 path) comes through DFF1, DFF2, NAND AND OR1.

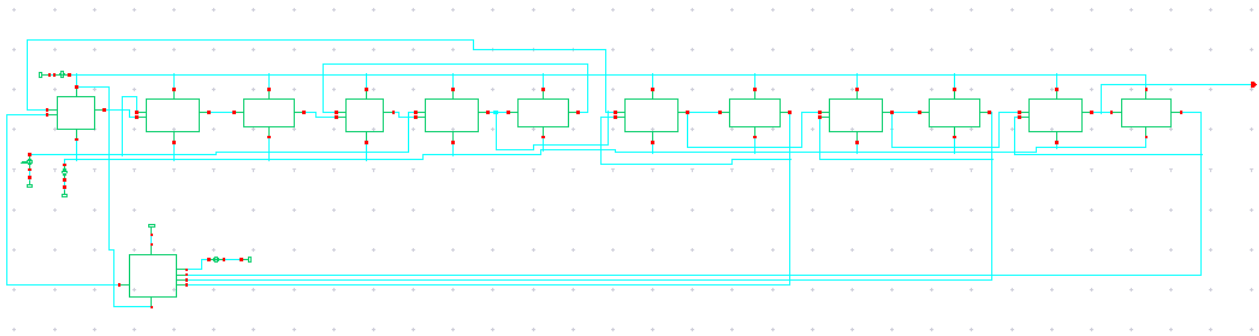


Fig.4 shows the schematic of Conventional divide-by-16/17 prescaler is implemented by using fig3 as reference in 180nm technology.

Within a period of F_{in} , signal must pass path#1 while within a periods of F_{in} it should pass path#2.theoretically, it is critical to identify which path decides the minimum working period. But the result varies in different designs. In conventional divide by 16/17 prescaler there is a trade-off between lengths of the two critical paths. The optimized design is to make the length of critical path #1 approximately equal to half length of critical path #2.

In conventional divide-by-16/17 prescaler, In front of DFF0 two logic gates (NAND and OR1) are located. In addition, there are two critical paths. Apparently, It is not the optimized design .To achieve a high speed both the critical paths should be optimized, which is a great challenge for designers.

IV. PROPOSED DIVIDE-BY-16/17 DAUL MODULUS PRESCALER

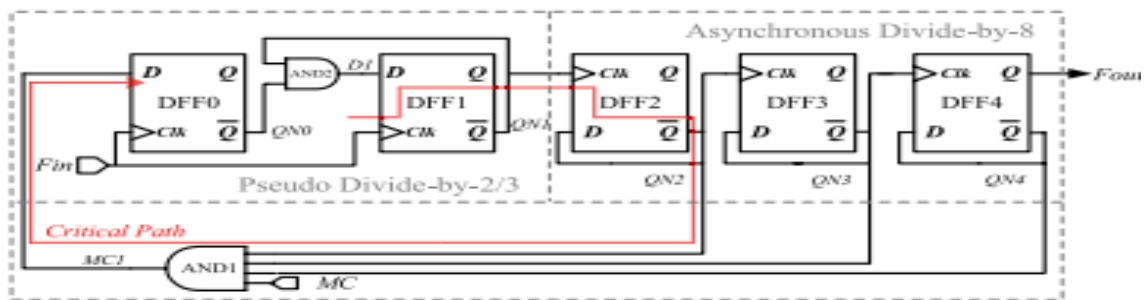


Fig 5: structure of proposed divide-by-16/17 prescaler

Fig.5 shows the schematic of the proposed divide-by-16/17 prescaler. It consists of a pseudo divide-by-2/3 prescaler, an asynchronous divide-by-8 divider, and a four-input AND gate. there are two main changes in the proposed divide-by-16/17 prescaler ,compared with the conventional circuit. First, instead of conventional divide-by-2/3 prescaler, a new pseudo divide-by-2/3prescaler is adopted. The pseudo divide-by-2/3 prescaler can exactly accomplish a single, but not continuously accomplish divide-by-3 operation. An OR gate is saved by adopting a pseudo divide-by-2/3 prescaler and leave's only one AND gate in front of DFF0. As a result, the critical path #1 in conventional circuit is disappeared and the length of critical path#2 is reduced. Second, QN1,QN2 and QN3 node (instead of Q1 and Q2node in conventional circuit) of DFF1, DFF2, and DFF3, is connected to the input CLK node of DFF2, DFF3, and DFF4, respectively. The propagation delay of DFF1, DFF2, and DFF3 will decrease. Thus, there is a reduction in the length of critical path.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2015

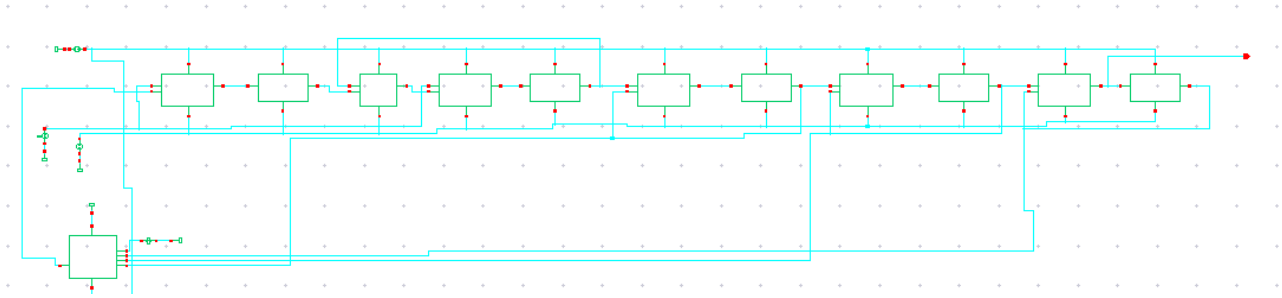


Fig 6: schematic of proposed divide-by-16/17 prescaler

The operation mode of proposed circuit is as follows. When $MC = 1$, MC1 changes its value according to (QN2, QN3, QN4). The pseudo divide-by-2/3 prescaler controlled by MC1 accomplishes seven times of divide-by-2 operations and one time of divide-by-3 operation in a cycle. The whole circuit operates in divide-by-17 mode. When $MC = 0$, MC1 keeps low and the pseudo divide-by-2/3 prescaler keeps on divide-by-2 operation. The whole circuit works in divide-by-16 mode. Fig 6 shows the schematic of proposed divide-by-16/17 prescaler implemented by using fig 5 as reference in 180nm technology.

V. MEASUREMENT RESULTS

TABLE 1: power and delay comparison

TSPC flip-flop	power	delay
pos_edge TSPC flip-flop	10.46e-6	20.1e-9
Modified pos_edge TSPC flip-flop	3.217e-6	20.04e-9

The above table 1 shows the power and delay comparison of normal TSPC flip-flop (positive edge) and proposed TSPC flip-flop. The power and delay consumption of proposed TSPC flip-flop is less compared to normal TSPC flip-flop and the proposed TSPC flip-flop circuit consists of less number of transistors than the normal TSPC flip-flop.

TABLE 2: frequency calculations

frequency	Divide by 2 operation		Divide by 3 operation	
	1Ghz	1G/2	500M	1G/3
1.8Ghz	1.8G/2	1n	1.8G/3	666.66M

The above table 2 shows the frequency calculation for two different frequencies, when control signal is high the circuit performs divide-by-2 operation, means it will divide the clock frequency by 2, when control signal is high. when control signal is low, the circuit performs divide-by-3 operation, means it will divide the clock frequency by 3, when control signal is low.

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Vol. 4, Issue 7, July 2015

TABLE 3: frequency calculations

frequency	Divide by 16 operation		Divide by 17 operation	
	1Ghz	1G/16	62.5M	1G/17
1.8Ghz	1.8G/16	112.5M	1.8G/17	105.88M

The above table3 shows the frequency calculation for two different frequencies, when control signal is high the circuit (fig. 5) performs divide-by-17 operation, means it will divide the clock frequency by 17,when control signal is high. When control signal is low, the circuit performs divide-by-16 operation, means it will divide the clock frequency by 16,when control signal is low.

TABLE 4: power and delay comparison of conventional divided by 16/17 prescaler

frequency	Divide by 16 operation		Divide by 17 operation	
	power	delay	power	delay
1.4G	5.669e-3	1.22e-9	5.334e-3	1.22e-9
1.6G	5.66e-3	1.086e-9	5.84e-3	1.086e-9
1.8G	6.315e-3	980.7e-12	6.607e-3	980.6e-12

TABLE 5: power and delay comparison of proposed divided by 16/17 prescaler

frequency	Divide by 16 operation		Divide by 17 operation	
	power	delay	power	delay
1.4G	5.455e-3	407.5e-12	4.298e-3	465.2e-12
1.6G	5.391e-3	407.9e-9	5.367e-3	441.7e-12
1.8G	6.256e-3	384.2e-12	6.108e-3	417.1e-12

The above table 4 & 5 shows the power and delay comparison of conventional and proposed divide-by-16/17 prescaler. The proposed divide-by-16/17 prescaler consumes less power and delay compared to the conventional divide-by-16/17 prescaler for different frequencies as shown in the above table.

VII.SIMULATION RESULTS



Fig.7 waveform of proposed divide-by-16 operation

The fig 7 shows measured output waveform of the proposed divide-by-16 prescaler at 1.8GHz input frequency in divided by 16 mode. The first waveform is clock signal which is taken as an input. The second waveform is the control signal and the third waveform is the output waveform.

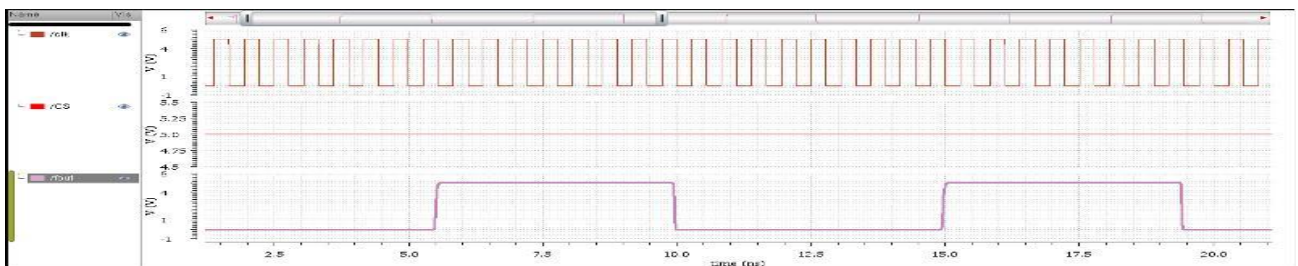


Fig8: waveform of proposed divide-by-17 operation

The fig 8 shows measured output waveform of the proposed divide-by-17 prescaler at 1.8GHz input frequency in divided by 17 mode. The first waveform is clock signal which is taken as an input. The second waveform is the control signal and the third waveform is the output waveform.

VII. CONCLUSION

This brief presents a novel high speed TSPC divide-by-16/17 dual modulus prescaler. The proposed TSPC with split path not only reduces the clock load and decreases power but also increases the speed of operation which in turn reduces total power consumption in divide-by-16/17 prescaler. The speed of prescaler is improved in two aspects. First is by adopting a new pseudo divide-by-2/3 prescaler, the minimum working period is reduced by half an NOR gate’s delay. Second is by changing the connection of TSPC D-Flip-flops, the minimum working period is reduced by half an inverter’s delay. Fabricated in 0.18um CMOS technology, the proposed circuit achieves a 1.8GHz maximum working frequency.

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