

# A Review of Clock Gating Techniques in Low Power Applications

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**ABSTRACT:** Power dissipation is a matter of concern as far as designing high performance systems are concerned. This makes clock signals a great source of power dissipation. High frequency systems use a large number of clock pulses. Whereas clock signals are only used for synchronization of the circuits the power dissipation due to clock pulses is significant making it important to study. Consider a system which is fed clock pulses to change its output. In most of the cases the pulses go waste as the output does not change. Thus the extra clock pulses used form apart of power dissipation rather that adding to the circuit performance. Thus there is a need of the clock gating (CG) technique which can be applied to reduce power. In this paper clock gating technique is used to reduce power consumption as compared to non gated circuit. The circuit simulation is done by Tanner EDA software in 22 nm technology and power consumption is obtained using T-spice simulation.

**KEYWORDS:** clock gating, pulse, Tanner EDA.

## I. INTRODUCTION

In the past, the major concerns of a VLSI designer were area, performance, cost and reliability of the system. Thus power was considered secondary. But nowadays the scenario has changed and day by day power parameter is gaining importance. Several factors have contributed to this trend. The main reason behind popularizing low power is new generation of portable devices which includes laptops, palm tops, mobile phones etc. Thus apart from performing at high speeds the devices must also work at low power to satisfy human needs. Thus it has become imperative to consider power consumption as a very important and significant design concern. [1]

With the smaller geometries in Deep Sub-Micron (DSM) technology, the number of gates that need to be integrated on a single chip, power density, and total power are increasing rapidly. Also, designing for low-power has become increasingly important in a wide variety of applications. However, creating optimal low-power designs involves trade such as timing and power which are applicable to different stages of a design flow. The best designs are the ones which enables a system to be accurate as well as fast with low power consumption. To address these issues directly, it is essential to understand the different types and sources of power dissipation in digital Complementary Metal Oxide Semiconductor (CMOS) circuits. The reason for choosing the CMOS technology is that it is currently the most dominant digital IC implementation technology. Power dissipation in CMOS digital circuits is categorized into two types: peak power and time-averaged power consumption. Peak power is a reliability issue that determines both the chip lifetime and performance [2].

The voltage drop effects, caused by the excessive instantaneous current owing through the resistive power network, affect the performance of a design due to the increased gate and interconnect delay. This large power consumption causes the device to overheat which reduces the reliability and lifetime of the circuit. Also noise margins are reduced, increasing the chance of chip failure due to crosstalk. CMOS digital circuits occur in two forms: dynamic and static. Dynamic power dissipation occurs during the process of switching between logic 0 and logic 1. During this process, any internal and external capacitance associated with the gate's transistors has to be charged, thereby consuming power. Static power dissipation is associated with inactive logic. Dynamic power is important during normal operation,

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especially at high operating frequencies, whereas static power is more important during standby, especially for battery powered [3].

Clock gating is one of the techniques that can be used in various synchronous circuits to reduce power consumption. Generally power dissipation is spoken in terms of dynamic power dissipation as it accounts for maximum part of the total power dissipation. The major objective of clock gating circuitry is to prevent clock pulses to be used in the circuit whenever there no change in the output so that that the flip-flops in them do not have to switch states. As switching of states consume power if unnecessary switching does not take place then there would not be wastage of power [4]. Thus only when enable signal is high the clock pulses are provided to the flip flops. In this way apart from saving power some area is also optimized as use of multiplexers is replaces by clock gated logic

Thus from the above discussion it is seen that low power has emerged as a top parameter to be addressed in today's world of integration. The need for low power arising mainly due to device portability has caused a shift of interest of design engineers where power is given equal importance as compared to performance and area. Two components determine the power consumption in a CMOS circuit. Static power includes sub-threshold leakage, drain junction leakage and gate leakage due to tunnelling. Among these, sub threshold leakage is the most prominent one. Dynamic power includes charging and discharging power and short circuit power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device lowers the threshold voltage even lower [6].

## II. EXISTING GATING METHODS

### A. NOR GATE BASED CLOCK GATING

NOR gate is a very suitable technique for clock gating where we need actions to be performed on Positive Edge of the Global clock. For analysis using NOR gate, the circuit connection is shown in Figure 1. In this figure it can be observed that Counter will work when enable turns ON. [2]

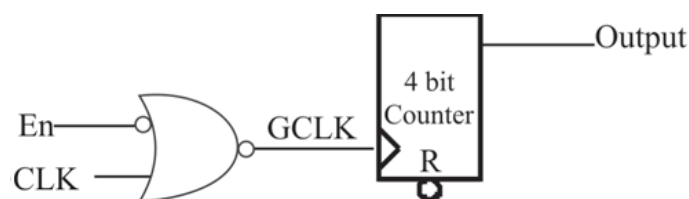


Figure 1: Clock gating using NOR gate [2]

When enable changes to '1' at negative edge of the clock we get an incorrect output. Incorrect output is due to the small glitch when enable turns low at negative edge of the clock, counter increments one more clock. Correct output of the counter is measured with positive edge trigger because enable is changing from positive edge of the clock to the next positive edge of the clock. When any hazard at the enable could be pass on to the Gclk when clk='0' this situation is particularly very dangerous and could jeopardize the correct functioning of the entire system.

### B. LATCH BASED NOR GATE CLOCK GATING

Latch based NOR Gated Clock scheme is shown in Figure 2. Here enable signal is applied through latch in place of direct connection to NOR gate. [2]

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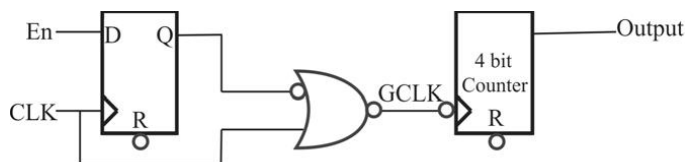


Figure 2: Clock gating using latch-based NOR gate circuit [2]

It is seen that the counter will take one extra clock cycle delay to change its state and after that it will work normally until En is de-asserted and this time also it will take one clock cycle extra to stop changing its state. Thus unwanted outputs due to Glitches at the En must be avoided. The output of the counter will be incorrect if it increments once even when enable is turned down due to a tiny glitch due to the fall time delay of enable.

### C. AND GATE BASED CLOCK GATING

In sequential circuit one two-input AND gate is inserted in logic for clock gating. One input to AND gate is clock and while the second input is a signal used to control the output. For experimental purpose a simple counter shown in Fig 3 is used as a sequential circuit application. Initially at reset = 0 counter is initialized to 0 and after that when reset =1 counter increments at each negative edge of the clock.

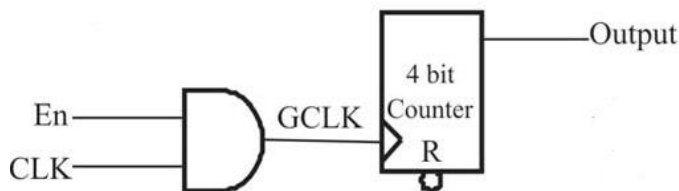


Figure 3: Clock gating using AND gate [2]

The above figure shows the clock gating technique for the counter by inserting one AND Gate. The output of counter is achieved when counter is negative edge triggered and 'enable' changes from clock cycle starting from negative edge to the next negative edge. In this case output of the counter changes after one clock cycle of being en='1'. Thus it can be seen that when counter is positive edge triggered and enable is changing starting from positive edge to the next positive edge, counter increments one extra time, due to tiny "Glitch", when it goes down due to more falling time of the enable, and thus the output achieved is wrong. In general for positive edge triggered system when enable turns ON at negative edge of the clock to the next negative edge, the counter increments only one time at positive edge of the clock because when enable goes down there is the negative edge of the clock not positive. A major problem of Hazards arises when any hazard at the enable could be passed on to the Gclk when clk='1' this situation is particularly very dangerous and could jeopardize the correct functioning of the entire system.

### D. AND GATE BASED CLOCK GATING

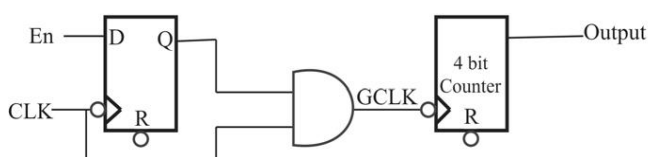


Figure 4: Clock gating using latch-based AND gate circuit [2]

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Latch based and gated clock circuit is shown in figure 4. the enable signal 'en' is applied through a latch to overcome the previous problems of incorrect output in place of directly connected to and gate. the latch is needed for correct behaviour, because en might have hazards that must not propagate through and gate when global clock is '1'. however, the delay of the logic for the computation of en may increase and its effect must be taken into account during time verification. it is clear that counter will take one extra clock cycle delay to change its state and after that it will work normally until, en is de-asserted and this time also it will take one clock cycle extra to stop changing its state .the latch makes it clear that unwanted outputs due to hazards at the en are avoided. when the controlling latch is positive and counter is also positive edge triggered then output of the counter is incorrect because it increments once even when enable is turned down due to a tiny glitch.

### III. METHODOLOGY USED

The basic operation of practical data driven clock gating is explained in the following paragraphs. It can be seen that the clock of the flip flop can be disabled in the next cycle by XORing its output with the present data input that will appear at its output in the next cycle. The outputs of k XOR gates are ORed to generate a joint gating signal for k FFs, which is then latched to avoid glitches. The combination of a latch with AND gate is commonly used by commercial tools and is called integrated clock gate (ICG). Such data driven gating is used for a digital filter in an ultralow-power design. For the scheme studied to be beneficial, the clock enabling signals of the grouped FFs should preferably be highly correlated. Figure 5 shows a practical data-driven clock gating. [1]

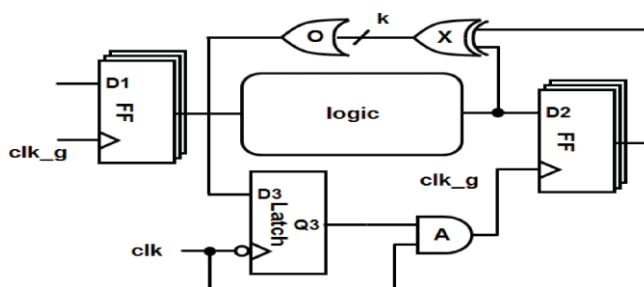


Figure 5: Clock gating logic [1]

With an increase in k, the hardware overhead decreases but so does the probability of disabling, obtained by ORing the k enable signals.

### IV. OBSERVATION & RESULTS

It can be seen from the above mentioned techniques as to how can power consumption can be made low. Such techniques form a very important base in today's world of portable devices. The AND and NOR gate is used for the sake of simplicity as a tool of clock gating. Whereas latch enabled AND and NOR gate is used for a better and complex design.

### V. CONCLUSION

Overall four techniques are studied above. It is seen that latch enabled gating is better as compared to the circuits without latches. Gated 'AND' and 'NOR' circuits reduce the power consumption but are exposed to unwanted signals or undesirable signals technically termed as glitches. If latch enabled clock gating is used then glitches are prevented. Thus all the problems of bad signals including metastability and spurious clocking are also removed using latches.

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