

Low Power 10T SRAM Design for Dynamic Power Reduction

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ABSTRACT: The aim of paper is to get over the problem of 6T SRAM cell where it loses its reliability at low supplies due to degraded noise margins. This is done by using a 10T SRAM where the cell uses a charge sharing technique between the transistors so that SRAM could be made more rigid against the noises that can cause damage to the cell at low power supplies and along with that charge sharing between the bit lines results in power consumption of the cell as the power required for charging bit lines are reduced which results in deduction of dynamic power budget of SRAM cell. The comparison between the power consumed by 8T and 10T SRAM is made. It shows that more power is consumed by 8T as compared to 10T SRAM. Also, the project shows the comparison between area of 8T and 10T SRAM that can be disregarded when used in millions.

KEYWORDS: 10T SRAM, 8T SRAM, dynamic power budget.

I. INTRODUCTION

According to the International Technology Roadmap (ITRS), 90% of the chip-area will be occupied by the memory core by 2014 [1]. This shows an increasing demand for more chips area for embedded memory with a commitment for low power, standby data retention, stability, and less cell area. From few decades, CMOS devices are scaled down to achieve the better performance in terms of speed, size and reliability, power dissipation. Our focus is to make the general use device like computer more compact in terms of size, better speed, less power consumption and so we are moving towards the new technology. That can be done by making memories compact and faster and so the scaling CMOS is done to attain high speed and decrease size of memory i.e. SRAM. Due to scaling of device designs are facing new challenges day by day like oxide thickness fluctuation, intrinsic parameter fluctuation. Working on low threshold voltage and leakage energy also became main concern. SRAM (Static Random Access Memory) is memory used to store data. The comparison of different SRAM cell on the basis of different parameter is done. 6T, 8T and 10T SRAM cell are compared on basis of read delay, power dissipation. The technology used to implement 8T and 10T SRAM is 22 nm and 45nm technology. The performance requirement increases amount of embedded SRAM in systems-on-chip (SoC) and microprocessors in each new technology. Because of the large number of transistors used in the memory caches is the important source of the leakage which also caused by data stability issues and SRAM arrays. So, a SRAM with high data stability and lower power consumption is desirable [2].

Due to this many attempts were being made to decrease the power consumption in SRAM which will increase the battery lifetime of the devices which were operated using battery such as PDA's, wireless, cellular phone, low power biomedical devices alongwith sensor network domain. But due to scaling operation, the gate delay is increased which reduces the frequency of operations [3]. Hence, another method of charge sharing using 10T SRAM is used to get over the severe problems faced by conventional SRAM.

This concept charge sharing is used in architectural level, but it is implemented at the cell level of design on the single ended SRAM's. Hence, aim has been to reduce the power consumption of the SRAMs. Supply voltage scaling is the most used method for power reduction. But the 6T cell loses its reliability at low supplies due to degraded noise margins. So a large number of other cells have been proposed that increase the stability of the cell. Of that, the single

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ended 8T cell is one which frees the read SNM of the cell and makes further scaling of the supply voltage possible at the same time reducing the power consumption of the memory stack arranged in array. Leakage current is the severe problem faced by SRAM when they are subjected to technology scaling in order to bring down voltage requirement of the system. Hence if the accessed cell has a stored data '1' while all other cells in the column have a stored data '0' then the total off state leakages of the cells can drain the read bitline to give a false read value of '0'. Hence it is of most interest to reduce the bitline leakage to avoid such a condition in advanced technologies at low supply voltages. In recent years various techniques to reduce the bitline leakage have been proposed of which the virtual ground is the most effective one. But it incurs area penalty for virtual ground driver and routing of virtual ground lines. Although the concept of charge recycling has been used at the architecture level for the differential ended SRAMs this concept is being introduced at the cell level with inbuilt mechanism for charge sharing within a cell for single ended SRAMs [4].

Now a day's to reduce the silicon area and to achieve high speed and performance, the devices are being scaled down to a great extent. Generally, supply voltage is scaled down to reduce the static power dissipation, but along with that for high performance the threshold voltage should also be scaled down [5]. The reduction in the threshold voltage exponentially increases the sub threshold leakage current which leads to increment in the static power dissipation. Static power dissipation is mainly contributed by sub threshold current and gate leakage current. The cache memory in a microprocessor occupies more than 50% of chip area so the leakage power of cache is a major source of power dissipation in the processor [7].

II. SRAM DESIGN

BASIC 6T SRAM:

A number of SRAM cell topologies are reportable within the past decade. Among these topologies, resistive load four-transistor (4T) cell, load less 4T cell and 6 transistor(6T) SRAM cell have received attention in apply, attributable to their symmetry in storing logic 'one' and logic 'zero'. The information retention within the 4T SRAM cells is ensured by the leakage current of the access transistors. Hence, they're not correct candidates for low-power applications. On the opposite hand, the information stability during a 6T SRAM cell is free lance of the outflow current. Moreover, 6T configuration exhibits a significantly higher tolerance against noise that is a very important benefit particularly within the scaled technologies wherever the noise margins area unit shrinking. That's the most reason for the recognition of the 6T SRAM cell in low-power SRAM units rather than the 4T configurations.

The 6T SRAM cell is most generally utilized in embedded memory attributable to its quick time interval and relatively little space. 6T cell style involves complex tradeoffs between varied factors specifically minimizing cell space, sensible soft error immunity, high cell scan current, low escape current, good cell stability with minimum voltage & amp; minimum word line pulse. The total CMOS 6T SRAM bit cell configuration is shown in figure. Full CMOS SRAM configuration provides superior noise margin, low static power dissipation, high change speeds & amp; suitability for prime density SRAM arrays. Each 6T cell contains a capability of storing one little bit of information [8].

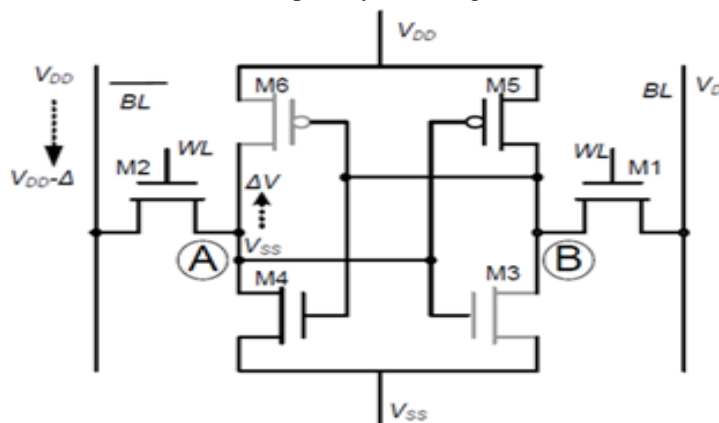


Figure 1: 6T SRAM [8]

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The 6T SRAM cell consists of 2 inverters connected back to back. M1, M2 are access transistors that are controlled by the word line (WL) signal. The cell preserves one in all its 2 possible states denoted as 0 and 1 as long as power is obtainable to the bit cell.

There are 3 operations in SRAM memory cell particularly write, read and hold operations. Read and write operations are initiated by declarative the word-line (WL) signals. Throughout write operation the value to be written is applied to the bit lines and for browse operation each BL and BLB is recharged to VDD. Throughout the browse operation the 0 storing node is rattled & this may flip the keep knowledge, however the palm write operation needs that data should be flipped very easily. Traditionally device sizing has been adopted to balance the read versus write design requirements.

8T SRAM:

At the start of the read cycle the read bitline is precharged to full swing voltage. After the precharge phase is over, Read Wordline (RWL) is asserted that drives the access transistor M5 ON. If the data stored at node Q is '0' the transistor M6 is on and Read Bitline (RBL) discharges through the transistors M5 and M6 to ground. This dip in the voltage of the RBL is detected by the sense amplifier attached at the end of the column and it generates a data output value of '1'. During the read '1' operation access transistor M5 is ON but as Q is '1' M6 is OFF. Hence no discharge current flows through the read path. Only a small amount of leakage current flows which is called bitline leakage [4].

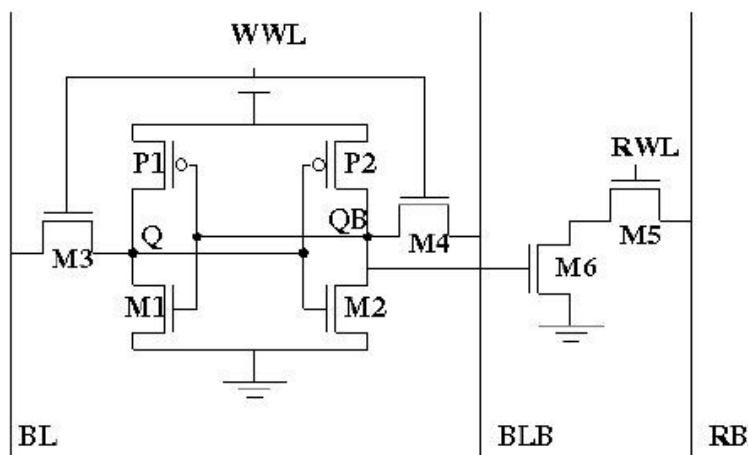


Figure 2: 8T SRAM cell [4]

III. IMPLEMENTED DESIGN

10T SRAM:

In 10T SRAM is similar to the 8T SRAM with extra transistors are connected to the read decoupled path with bit lines (BL & \overline{BL}) to avoid the draining of read current to ground. The architecture of the 10T cell is similar to the single ended 8T cell. In addition to the 8 transistors, 2 transistors are added in the decoupled read path and instead of draining the read current to ground the read path is connected to BL & BLB through these 2 transistors [4]. Hence, whenever read bitline discharges it will get its charge discharge through 2 paths i.e. M5-M6-M7-BL or M5-M6-M8- BLB. So, these paths give 2 cases:

CASE I: If the previous written data was '0', BLB is high and BL is low. If any cell in the column now reads a value '0', the RBL discharge goes though the read path transistors M5, M6 and M7 to BL. As the BL is floating during the read cycle, the charge is shared between the read bitline RBL and bitline BL.

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CASE II: If the previous written data was '1', BL is high and BLB is low. The high BL enables the transistor M8. If any cell in the column now reads a value '0', the RBL discharge goes through the read path transistors M5, M6 and M8 to BLB.

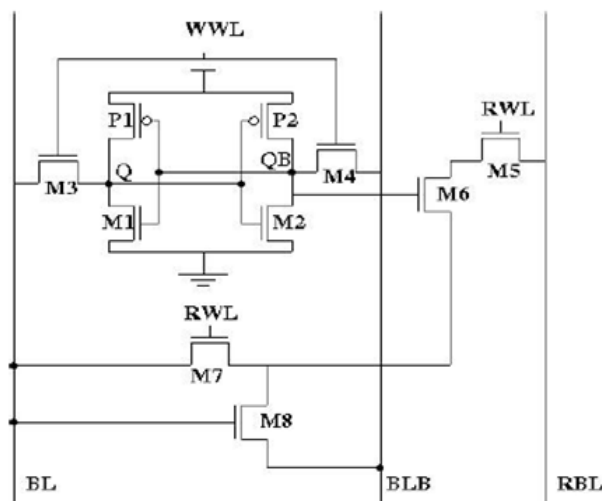


Figure 3: 10T SRAM structure [4]

Write operation:

If in next cycle write '1' operation is performed then BL is to be driven from mid-level voltage to full swing as BL is already at mid-level voltage. Likewise, the read discharge power can be used for the reduction of write power. If in next cycle write '0' operation is performed then BL is grounded. As bit lines are at some mid-level voltages they are to be grounded.

IV. EXPERIMENTAL RESULTS

Power Consumption for 45nm Technology for different operations

Operating Voltages	READ '0'		WRITE '0'		WRITE '1'	
	8T	10T	8T	10T	8T	10T
0.8 V	67.7 μ W	44.85 μ W	67.7 μ W	24.65 nW	67.7 μ W	44.85 μ W
0.9 V	38.4 μ W	26.54 μ W	38.4 μ W	14.38 nW	38.4 μ W	26.54 μ W
1 V	3.64 μ W	72.67 nW	3.64 μ W	6.1 nW	3.64 μ W	72.67 nW
1.1 V	56.52 μ W	32.93 μ W	56.52 μ W	203.4 nW	56.52 μ W	32.93 μ W
1.2 V	117.3 μ W	73.2 μ W	117.3 μ W	2.98 μ W	117.3 μ W	73.2 μ W
1.3 V	197.4 μ W	129.1 μ W	197.4 μ W	20.45 μ W	197.4 μ W	129.1 μ W
1.4 V	314.8 μ W	198.7 μ W	314.8 μ W	62.6 μ W	314.8 μ W	198.7 μ W

Now, for 45nm technology for operating voltage of 1V for READ '0' operation

Power consumed by 8T SRAM = 3.64 μ W

Power consumed by 10T SRAM = 72.67 nW

Power consumption improved by factor = (3.64 μ W/72.67 nW)= 50.09

V. CONCLUSION

Thus, it can be concluded that paper focuses on a method of charge sharing between the bitlines of 10T SRAM and these method consumes less power for read operations and cut systems dynamic power budget to greater extent as compare to 8T SRAM. Thus, for read '0' operation under same operating conditions for 45nm of technology, power consumption of 10T SRAM get reduced by a factor of 50.09 when compared to its counterpart 8T SRAM cell. The significant improvements obtained in the results through the use of 10T cell which will be applicable for future low

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power memory design. Though, there is a major drawback for area for 10T SRAM over 8T cell but the 10T SRAM design can be looked as boon for applications such as sensor network domain that is battery driven application.

SRAM is by far the dominant form of embedded memory found in today's integrated circuits. In fact, the majority of transistors found in many integrated circuits are those utilized in the SRAM bit cells with the percentage die occupied by this type of memory approaching 85%-90% for certain integrated circuits. Because this memory is typically constructed from traditional CMOS devices, all of the issues associated with MOSFET scaling apply to scaling of SRAM. Issues such as dopant fluctuations, gate oxide leakage, control of short channel effects, contact resistance, abrupt and low spreading resistance junction technology must be resolved for continued scaling of the traditional SRAM bit cell.

Additionally, there is a desire to find a dense SRAM replacement that can substantially reduce the area occupied by the traditional SRAM bit cell (6T bit cell traditionally) while maintaining the performance offered by the current technology. Discovery of such a bit cell would have profound implications on the die cost of integrated circuits given the ever increasing area occupied by this type of memory. In addition to area scaling of the bit cell, there is also a need to develop alternative bit cells that maintain stability while operating at low voltages, thus, allowing the industry to substantially reduce standby power consumption in the memory arrays. In all of this research, SRAM bit cells that maintain or increase read/write performance are required.

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