

# CNTFET Based Energy Efficient Full Adder

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**ABSTRACT:** As we know CMOS technology has many drawbacks like short channel effects, drain induced barrier lowering, hot carrier effect etc. So the designers are looking for new technology. CNT was developed in 1991 to overcome the drawbacks of CMOS. CNTFET has its structure similar to CMOS but the channel between source and drain is replaced with carbon nano tubes. CNTFET works on the principle of ballistic transport. To improve its performance, diameter and threshold voltage are made variable parameters to make it an efficient device over CMOS. This variation is made possible with the help of chirality. In the present study, work has been done on full adder using CNTFET and CMOS technology. Different parameters such as power dissipation, propagation delay and power delay product on 32nm model file are calculated for 0.9v, 1.0v and 1.1v power supply. Results of CNTFET and CMOS have been compared. All the work has been carried out on Tanner TOOL V14.1 and HSPICE Version B 2008.09. Circuit designing has been done on S-edit and simulation has been carried out using HSPICE. The waveform of full adder is shown using Avanwaves of HSPICE.

**KEYWORDS:** CMOS, CNTFET, chirality, full adder circuit, advantages of CNTFET, power dissipation, propagation delay, power delay product, tanner tool v14.1, HSPICE version b 2008.09.

## I. INTRODUCTION

As the technology grows the demand for scaling down has increased. The CMOS shows various false effects of scaling down. Some of them are short channel effects, hot carrier effect and drain induced barrier lowering.[15] Due to these effects a new device has been introduced named CNTFET.[2] Carbon nanotube field effect transistor (CNTFET) is the very effective technology to extend due to [12],[13],[14] three reasons: First, the operation principle and the device structure are similar to CMOS devices; we can reuse the established CMOS design infrastructure. Second, we can reuse CMOS fabrication process. The most effective reason is that CNTFET has the best experimentally demonstrated current carrying ability till today. [4]

The carbon nanotubes are formed of graphene sheet. Graphene has advantages of being soft and mechanically strong which make it a suitable component of carbon over diamond for CNT manufacturing. CNTFET offers 1) ballistic transport, i.e current flows only in forward or backward direction. [9] There is no scattering of electrons due to collision because CNT is a hollow tube. So scattering of electrons is almost negligible. 2) almost negligible leakage current. 3) high tolerance to temperature. 4) high conductivity.[6],[7]

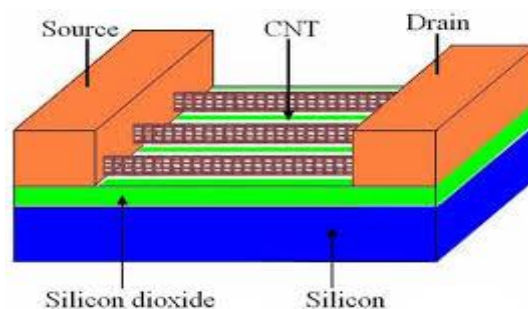


Fig 1: CNTFET Structure [1]

# International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

The rest of this paper is structured as follows: section 2 will provide the introduction of the parameters calculated for the comparison between CMOS and CNTFET technology. The proposed circuit of full adder is shown in section 3. Section 4 is explaining the process of simulation. Section 5 provides the analysis of the results and section 6 will conclude the results.

## II. PARAMETERS CALCULATED

### Power Dissipation:

The CMOS power dissipation has become a very important topic in the last few years. The number hand-held applications, like the mobile phones and laptops are rapidly increasing and many more additional features are added into the systems, like multi-media applications in handy phones. This is one of the emerging topic for analysis of power-reduction methods [10],[5]

- As the packet density increases, the need to minimize power dissipation also increases.
- Static power dissipation means the power dissipated when the device is in off state.
- Dynamic power dissipation is the power dissipated when the device is in conduction mode.
- The logic family must have small power dissipation for becoming an efficient device.

### Propagation Delay:

In any circuit operation there is a delay between the switching on and switching off of the device. The rise and fall delays are given by  $t_{PLH}$  and  $t_{PHL}$  respectively.

### Propagation Delay Parameters:

- $t_{PHL}$  : high-to-low propagation delay
- $t_{PLH}$  : low-to-high propagation delay
- $t_p$  (propagation delay) =  $(t_{PLH} + t_{PHL})/2$
- Maximum switching frequency  $f_{max} = 1/2t_p$

In short,

- The working speed of a device is determined by its propagation delay.
- Propagation delay  $t_p$ , is the average of  $t_{PHL}$  and  $t_{PLH}$ .

$$\frac{t_{phl} + t_{plh}}{2}$$

- The logic circuit is defined as an efficient circuit if its propagation delay is less.

### Power Delay Product:

- It is also known as the figure of merit.
- It is the given by the product of propagation delay and power dissipation of a circuit.
- It has dimensions of energy and its unit is picojoule, pJ.
- For the circuit to be efficient, its power delay product is desired to be minimum. [3]

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Vol. 4, Issue 6, June 2015

## III. PROPOSED CIRCUIT OF FULL ADDER

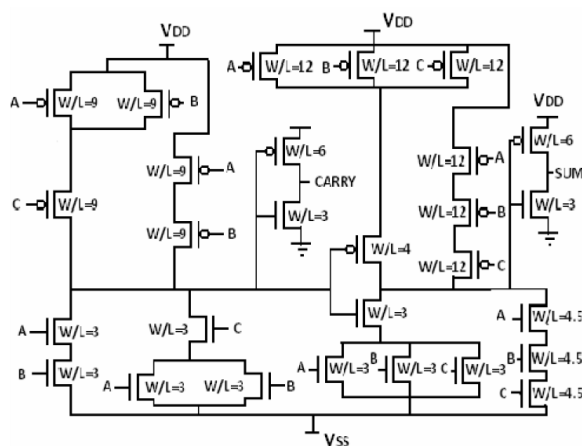


Fig 2: Full adder circuit

**W/L:** Width to length ratio

**Vss:** Source voltage as ground

**Vdd:** Drain voltage as source

**A,B,C:** Inputs

The proposed circuit is a full adder having transistor size of 28. The simulation will be carried out on this circuit for the comparison between CMOS and CNTFET in terms of power dissipation, propagation delay and power delay product.

## IV. SIMULATION PROCESS

In this paper work we will use TANNER TOOL version 14.1 and HSPICE version B-2008.09. In tanner tool I will make use of S-edit for making circuit. HSPICE will be used for coding and simulation. Synopsys HSPICE is an optimizing analog circuit simulator. You can use it to simulate electrical circuits in steady-state, transient, and frequency domains. HSPICE is used for fast and accurate circuit simulation.[8],[11]

The simulation is carried out on 32nm technology for 0.9v, 1.0v and 1.1 v of power supply. Temperature is taken 25 degree Celsius.

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Vol. 4, Issue 6, June 2015

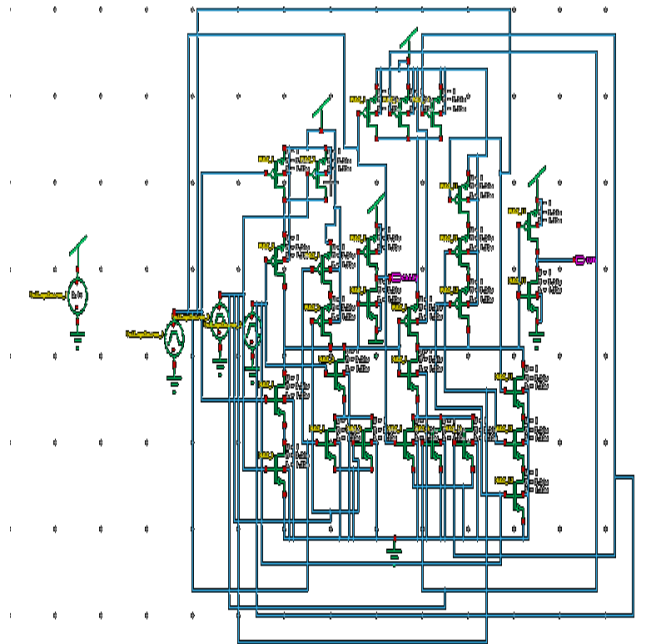


Fig 3: Full adder circuit in S-edit

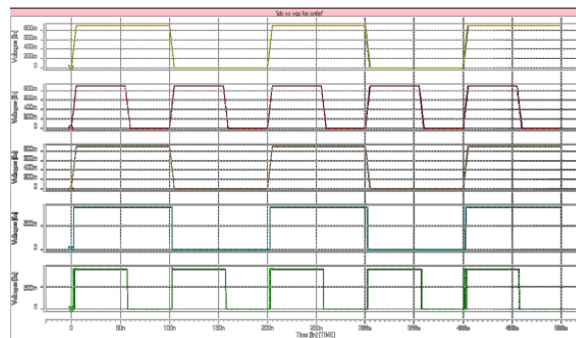


Fig 4: Full adder waveform

## V.RESULTS

Our proposed technique for making a full adder functionality using CNFET working accurately and the results are carried out in the table 1, table 2 and table 3.

### Results For Power Dissipation:

Table 1 shows power consumption in CNTFET and CMOS at 3 different power supplies (0.9v, 1.0v, 1.1v). The table shows that power consumption is less in CNTFET as compared to CMOS. The % power reduction is 80.14, 81.40, 84.0 (in microwatts) for 0.9v, 1.0v, 1.1v respectively.

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POWER SUPPLY	0.9V	1.0V	1.1V
CMOS	5.39	8.12	11.88
CNTFET	1.07	1.51	1.90
% POWER REDUCTION	80.14	81.40	84.0

Table 1: Power dissipation (Watts)

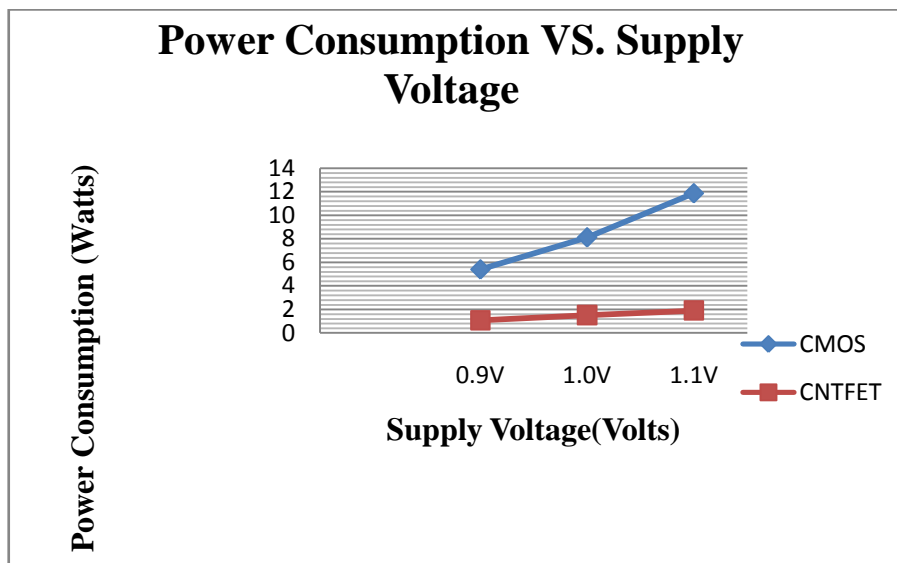


Fig 5: Power dissipation graph

### Results for Propagation Delay:

Table 2 shows the propagation delay for CMOS and CNTFET at 3 different voltages: 0.9v, 1.0v and 1.1v. The results of delay verify that CNTFET has less propagation delay when compared to CMOS.

POWER SUPPLY	0.9V	1.0V	1.1V
CMOS	45.69	45.98	46.20
CNTFET	0.09	0.13	0.16

Table 2: Propagation delay in ns

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(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

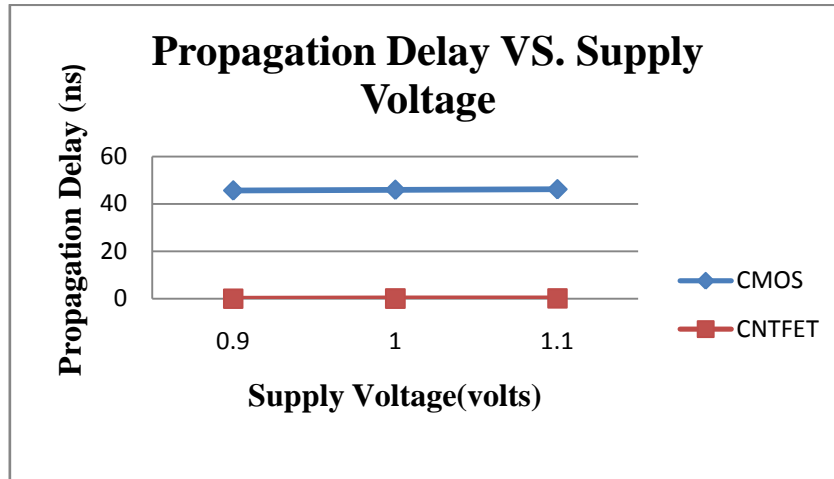


Fig 6: Propagation delay graph

### Results for Power Delay Product:

Table 3 shows the power delay product for CMOS and CNTFET at 3 different voltages: 0.9v, 1.0v and 1.1v. The results of power delay product verify that CNTFET has less power delay product when compared to CMOS.

Table 3: Power delay product in pJ

POWER SUPPLY	0.9V	1.0V	1.1V
CMOS	0.24	0.37	0.54
CNTFET	0.09	0.19	0.30

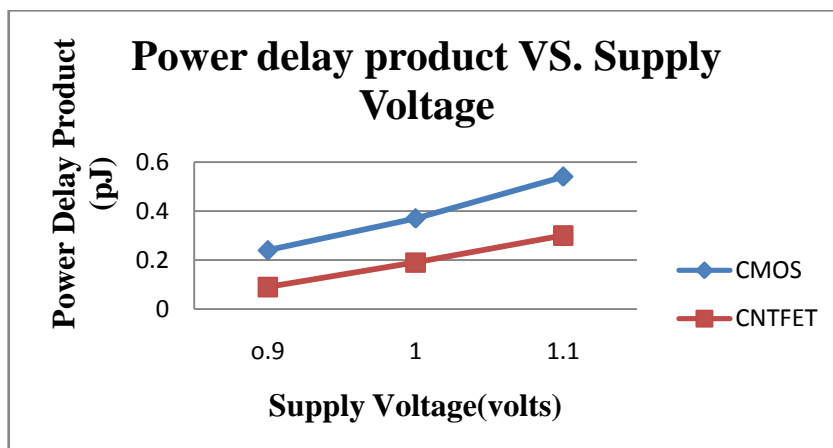


Fig 7: Power delay product

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(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

## VI. CONCLUSION

We have The Carbon Nanotube Field Effect Transistor (CNTFET) is one of the upcoming devices among the various new technologies to replace Si MOSFET efficiently. As the characteristics of a CNTFET is different from conventional bulk CMOS, new design method must be established. As demand of new design method, this project analyze the characteristics of CNFET, CNT interconnect technologies and propose new methodologies to design circuits such as digital, memory etc. In the designing of CNFET circuit, many parameters are taken into account such as the diameter at certain chirality, threshold and the pitch.

To prove the effectiveness of the proposed circuit, simulation has been performed using HSPICE version B 2008.09. Finally the comparison is made between proposed CNTFET based full adder and CMOS based full adder where we witness that CNTFET is better than CMOS in terms of power dissipation, propagation delay and power delay product. Results have demonstrated that the proposed design is both effective and practical.

## REFERENCES

- 1) Aliakbar Rezaei, Mehdi Masoudi, Fazel Sharifi, Keivan Navi, *A Novel High Speed Full Adder Cell based on Carbon Nanotube FET (CNFET)*, Int. J. Emerg. Sci.(IJES), issue 4(2),pp. 64-74, June 2014.
- 2) Ali Ghorbani and Ghazaleh Ghorbani, *energy efficient full adder cell design with using carbon nanotube field effect transistors in 32 nanometer technology*, International Journal of VLSI design & Communication Systems (VLSICS) Vol.5, No.5, October 2014.
- 3) Ali Ghorbani and Mehdi Sarkhosh and Elnaz Fayyazi and Neda Mahmoudi, *A novel full adder cell based carbon nano tubes field effect transistor*, International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012 .
- 4) Bipin Pokharel, Priya Gupta, Umesh Dutta, *Designing CNTFET and Force Stacking CNTFET Inverter for the Analysis of Average Power and PDP at Different Low Supply voltage*, International Journal of Engineering Research and Applications (IJERA) Vol. 3, Issue 4, Jul-Aug 2013, pp.1845-1855.
- 5) Data from google and Wikipedia.
- 6) Dafeng Zhou, *Circuit-level Modelling and Simulation of Carbon Nanotube Devices*, doctoral dissertation, Southampton University, 2010
- 7) Djamil RECHEM and Saida LATRECHE, *Nanotube Diameter Effect on the CNTFET Performances*, 5th International Conference: Sciences of Electronic, Technologies of Information and Telecommunications March 22-26, 2009 – TUNISIA.
- 8) "HSPICE User Guide: Simulation and Analysis" Version B 2008.09.
- 9) H.Upadhyay, A.choubey,K.Nigam, "*comparison among different CMOS inverterwith stack keeper approach in VLSI Design*" IJERA, vol .2, issue 3, may-jun 2012, page 640-646.
- 10) Institute of Electrical and Electronics Engineers. Vhdl analysis and standardiza-tion group, 2008. <http://www.eda.org/vhdl-200x/>.
- 11) Tanner tool user manual version 14.1
- 12) J. Deng, *Device Modeling and Circuit Performance Evaluation for Nanoscale Devices: Silicon Technology beyond 45 nm Node and Carbon Nanotube Field Effect Transistors*, doctoral dissertation, Stanford University, 2007.
- 13) M.H. Moaiyeri, K. Navi, and O. Hashemipour, "*Design and Evaluation of CNFET-Based Quaternary Circuits,*" *Circuits, Syst.,Signal Process.*, vol. 31, no. 5, Oct. 2012, pp. 1631-1652.
- 14) P A Aui, K M Lal, MJ Siddiqui, *carbon nanotubes field effect transistor: A review*,Indian Journal Of Pune And Physics, vol.43, Dec 2005, pp.899-909.
- 15) Pushpa Saini et.al. "*Leakage Power Reduction in CMOS VLSI Circuits*" International Journal of Computer Application, pp. 42-48, vol-55- no. 08 , October 2012.