

A Study and Analysis of Parameters of Two Stage Single Ended CMOS Operational Amplifier

Komal Rohilla¹, Shafali Ruhil², Ritu Pahwa³M.Tech Student, Vaish College of Engineering and Technology, M.D.U, Rohtak, Haryana, India^{1,2}Assistant Professor, Vaish College of Engineering and Technology, M.D.U, Rohtak, Haryana, India³

ABSTRACT: As we know PMOS and NMOS technology having many drawbacks .In this having speed is very slow and circuit complexity is increased and power dissipation is very high and low noise margin. So the designers are looking for new technology. CMOS was developed in 1963 by FRANK WANLASS AND CHIN-TANG SHAN OF FAIRCHILD to overcome the drawbacks of PMOS and NMOS. CMOS has its structure similar to PMOS and NMOS but in this both PMOS and NMOS are fabricated on same chip so due to power dissipation is less and speed high. In this paper we have focused on the various parameters like Gain, Phase margin and slew rate of CMOS based two stage single ended operational amplifiers under 0.35um and 0.130um CMOS technology. Designing of high gain CMOS operational amplifier with decreasing length CMOS is a challenge for designer. All the work has been carried out on Tanner EDA V14.1 software. Circuit designing has been done on S-edit and simulation has been carried out using T-spice. Waveform has been obtained on W-edit. The simulation result for different CMOS Op Amp have been compared and analyzed. The first section contains introduction, second section contains the study of proposed circuit and its parameters, third section contains simulation and result of parameters, , and the last section presents the conclusion and references.

KEYWORDS: CMOS, OPERATIONAL AMPLIFIER, CMOS BASED TWO STAGE OP AMP, SLEW RATE, GAIN, PHASE MARGIN, TANNER TOOL VERSION 14.1.

I. INTRODUCTION

The last few years, the electronics industry has exploded. Operational amplifiers are key elements in analog processing systems. Operational amplifiers are an integral part of many analog and mixed signal systems. As the demand for mixed mode integrated The persistent development of electronics, information technology (IT), and communications has been mainly enabled by nonstop development in silicon-based complementary metal-oxide-semiconductor (CMOS) technology. This nonstop development has been maintained frequently by its dimensional scaling, that results in exponential development in both gadget compactness and production. The decrease in cost-per-function has gradually been increasing the financial efficiency with all new technology generation.[3] Today CMOS ICs are random and indispensable circuits increases, the design of analog Circuits such as operational amplifiers (op-amps) in CMOS technology becomes more critical [1].Operational amplifiers (op-amps) with moderate DC gains, high output swings and reasonable open loop gain band width product (*GBW*) are usually implemented with two-stage structures [2]. In our life, ranging from moveable electronics to telecommunications and transportation [4] Operational amplifiers are an integral part of many analog and mixed signal systems. It can amplify signals having frequency ranging from 0 MHz to 1 MHz. This means that op-amp can be used to amplify D.C. signals as well as ac input signals. It is a complete amplifier and designed in such a way that external components like resistors, capacitors, etc. can be connected to its terminals. So that external characteristics can be changed. Advantages of op-amp are small size, reduced cost, high reliability, less power consumption than discrete circuits. Op-amp with vastly different levels of complexity is used to realize functions ranging from dc bias generation to high speed amplification or filtering. Common function op amps

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can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many applications. The design of op-amps continues to pose a challenge as the supply voltage and transistor channel length scale down with each generation of CMOS technologies. [5]

In a linear amplifier:

$$\text{Output} = A \times \text{Input Signal}$$

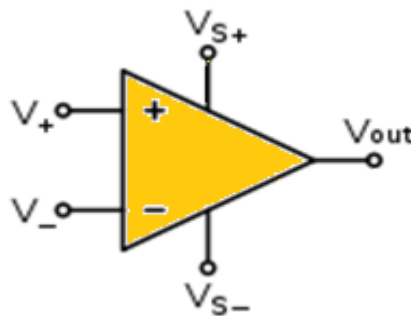


Fig 1: Circuit Diagram Symbol of Op-amp

- V_+ : non-inverting input
- V_- : inverting input
- V_{out} : output
- V_{S+} : positive power supply
- V_{S-} : negative power supply

CMOS Op-amp can be used very efficiently for practical consequences e.g. designing of a switched capacitor filter, analog to digital converter etc. In this case the designs of the individual op amps are combined with feedback and by various parameters that affect the amplifier such as input capacitance, output resistance, etc.[6]

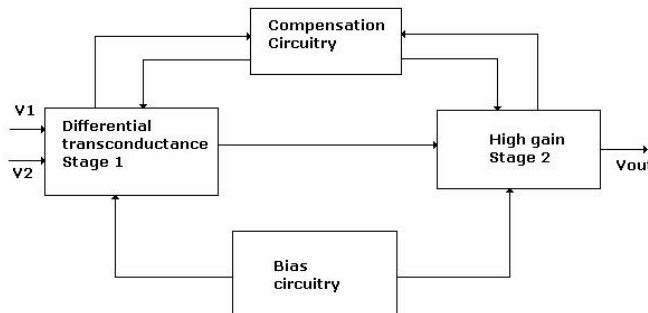


Fig 1.1: A general two stage CMOS Op-amp

The specific two-stage CMOS op-amp we consider is shown in Fig 1.1. The circuit consists of an input differential trans-conductance stage forms the input of the op-amp followed by common-source second stage. The common source second stage increases the DC gain by an order of magnitude and maximizes the output signal swing for a given voltage supply. This is important in reducing the power consumption [7-8]. If the Op-Amp must drive a low resistance load the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing [9-10]. Bias circuit is provided to establish the operating point for each transistor in its quiescent stage. Compensation is required to achieve stable closed loop performance [11-12]. However, due to an unintentional feed forward path through the Miller capacitor, a right-half-plane (RHP) zero is also created and the phase margin is degraded. Such a zero, however, can be removed if a proper nullifying resistor is inserted in series with the Miller capacitor [13].

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II.RELATED WORK

PERPOSED CIRCUIT OF CMOS BASED TWO STAGE SINGLE ENDED OPERATIONAL AMPLIFIER

The CMOS Op Amp circuit in Fig.2 is a Two Stage single ended Op Amp. It consists of 8 MOS Transistors. PMOS 4 and 5 along with NMOS 1 and 2 forms first differential stage and PMOS 3 with NMOS 3 forms the second stage. To increase the open-loop gain, a few steps were taken. One step was to decrease the width of current reference mirroring MOSFET, PMOS 1, so that it would cause a larger mirror of currents to the stage one and two current sources, M7 and M6. Also, the differential input positive. And negative transistors had their widths increased. Also, the differential input positive and negative transistors had their widths increased. This benefited in a larger gm for the first stage of signal amplification. A focus was made on increasing the gm of stage one because it had the smaller transconductance of the two gain stages. This was done primarily to the first stage of the op-amp because it had a lower gm.

The values of different circuit elements are:

- Current source, $I=5\mu A$
- Capacitor=4 and 4.5 pF
- Resistance=2.2K Ω

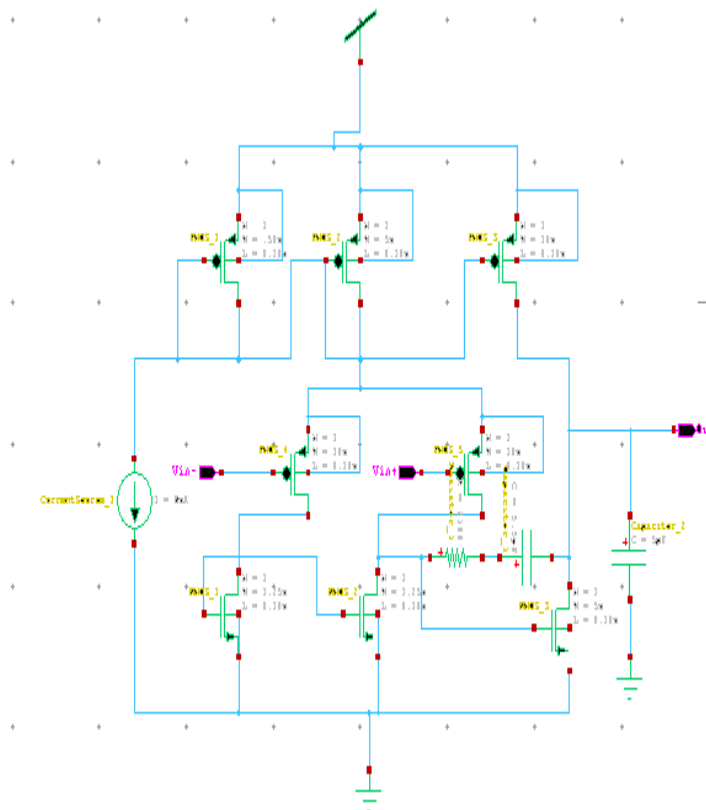


Fig 2: Two stage single ended CMOS Op Amp

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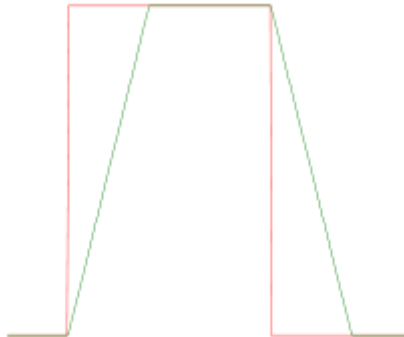
Table: 2.1 W/L ratio of transistors in Two stage single ended Op Amp

TRANSISTOR	W/L RATIO
PMOS 1	10/2
PMOS 2	100/2
PMOS 3	200/2
PMOS 4	200/2
PMOS 5	200/2
NMOS 1	25/2
NMOS 2	25/2
NMOS 3	100/2

II.I DESIGN PARAMETERS

SLEW RATE: slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed as volt per second. Limitations in slew rate capability can give rise to non linear effects in electronic amplifiers.

$$SR = \max \left(\left| \frac{dv_{out}(t)}{dt} \right| \right)$$



slew rate effect on a square wave: red= desired output, green= actual output

GAIN: Gain is a measure of the ability of a two port circuit (often an amplifier) to increase the power or amplitude of a signal from the input to the output port by adding energy converted from some power supply to the signal. It is usually defined as the mean ratio of the signal amplitude or power at the output port to the amplitude or power at the input port. It is often expressed using the logarithmic decibel (dB) units ("dB gain").

PHASE MARGIN: The phase margin (PM) is the difference between the phase, measured in degrees, and 180°, for an amplifier's output signal (relative to its input), as a function of frequency. Typically the open-loop phase lag (relative to input) varies with frequency, progressively increasing to exceed 180°, at which frequency the output signal becomes inverted, or anti phase in relation to the input.

III. RESULT & SIMULATION PROCESS

In this paper work we will use TANNER TOOL version 14.1. In tanner tool I will make use of S-edit for making circuit. T SPICE will be used for coding and simulation. Wave forms obtained on W-edit circuit simulator. You can use it to simulate electrical circuits in steady-state, transient, and frequency domains. T SPICE is used for fast and accurate circuit simulation.[14]

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The simulation is carried out on 35nm technology and 130 nm technology for Vdd 5v, and Vss -1v. And compare between them.

III.I SIMULATION RESULT AT L=0.35um

For L=0.35um we have selected Vdd=5v, Vss=-1v.
The result for the simulation obtained on W-edit is as shown below.

III.I.I FREQUENCY RESPONSE

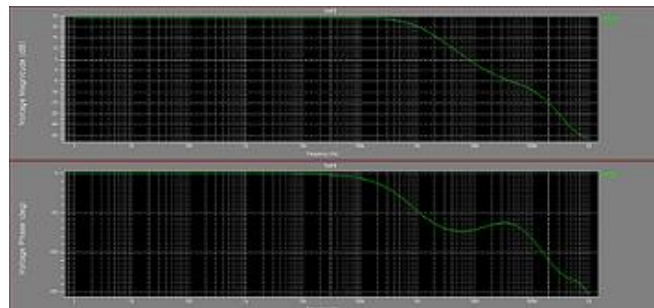


Fig: 3.1.Frequency response at L=0.35um

III.I.II SLEW RATE

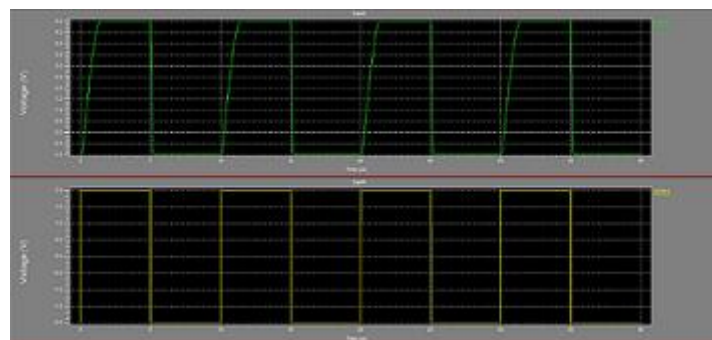


Fig: 3.2. Slew rate at L=0.35um

III.II SIMULATION RESULT AT L=0.13um

For L=0.13um we have selected Vdd=5v, Vss=-1v.
The result for the simulation obtained on W-edit is as shown below.

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III.II.I FREQUENCY RESPONSE

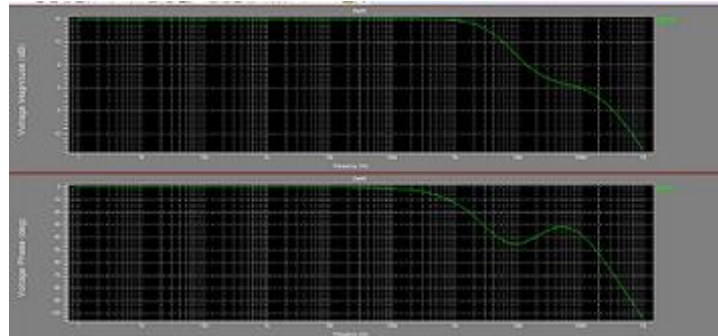


Fig:3.3.Frequency response at L=0.13um

III.II.II SLEW RATE



Fig:3.4. Slew rate at L=0.13um

The above figures shows the simulation result at L=0.35um and 100nm technology.

The simulation has been carried out on Tanner EDA.

Based on the simulation analysis following results has been obtained.

For the two-stage op-amp in 0.35 μm technologies with $V_{\text{dd}}=5\text{v}$ and $V_{\text{ss}}=-1\text{v}$, gain is 24 dB, phase margin is 120degrees and slew rate 4.54V/us for rising edge has been observed. For the two-stage op-amp in 0.13 μm technologies with $V_{\text{dd}}=5\text{v}$ and $V_{\text{ss}}=-1\text{v}$, gain is 15 dB, phase margin is 148degrees and slew rate 25V/us for rising edge has been observed.

Based on the above results we can draw a comparison table as shown below:

Table.3.1: Comparison of results for different CMOS Op Amp

PARAMETER	35nm CMOS OP AMP	130nm CMOS OP AMP
GAIN	24 db	15 db
PHASE MARGIN	120°	148°
SLEW RATE	4.54v/ μs	25v/ μs

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IV. CONCLUSION

. This work presents a study and analysis of the CMOS operational amplifier using 0.35 μm and 130nm CMOS technologies. The circuits named two-stage single ended op-amp have been simulated in Tanner EDA. The variation of parameters like gain, phase margin and slew rate with respect to input voltage and VDD has been simulated using the tool. For the two-stage op-amp in 0.35 μm technologies with $V_{\text{dd}}=5\text{v}$ and $V_{\text{ss}}=-1\text{v}$, gain is 24 dB, phase margin is 120 degrees and slew rate 4.54V/us for rising edge has been observed. For the two-stage op-amp in 130 nm technologies with $V_{\text{dd}}=5\text{v}$ and $V_{\text{ss}}=-1\text{v}$, gain is 15dB, phase margin is 148 degrees and slew rate 25 V/us for rising edge has been observed.

Hence from present study we conclude that with increasing in channel length of transistor gain decreases but slew rate increases. Hence it is a challenge for designer to increase the gain with use of nanotechnology of CMOS in channel length of transistor. Results have demonstrated that the proposed design is both effective and practical.

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