

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

A Low Transition Test Pattern Generation of Multiple SIC Vectors Based on Bist Schemes

T.Jeeva¹, G.Mohanraj², A.Sathish Kumar³, S.Saravanan.⁴

P.G. Student, Department of ECE, Maha Barathi Engineering College, Chinnasalem, Tamil Nadu, India¹

Assistant Professor, Department of ECE, Maha Barathi Engineering College, Chinnasalem, Tamil Nadu, India²

Assistant Professor, Department of ECE, Maha Barathi Engineering College, Chinnasalem, Tamil Nadu, India³

Professor & Head, Department of EEE, Muthyammal Engineering college, Rasipuram, Tamil Nadu, India⁴

ABSTRACT: A novel TPG (Test Pattern Generator) is proposed for L-BIST (Logical-Built In Self Test) schemes. Unlike conventional TPGs, the proposed TPG generates the MSIC vectors (Multiple single input changes) while traditional systems like seed generator and conventional XOR-seed generator clocked by two non-overlapping clocks generates SIC vectors for test the entire CUT (circuit-under test). Besides some of the schemes which are used for testing in not flexible for both test-per clock as well as test per scan scheme but this scheme is not a constraint. The two sub-modules are combined together to achieve the minimum transitions sequence thus MSIC vectors namely “reconfigurable Johnson-counter and old seed-generator” (XOR base) the outputs of both systems are finally XOR with one another. So an n-bit seed generator and m-bit Johnson counter generates the X_{mn} output vectors for testing the CUT. Due to this vector, a large amount of test coverage is achieved then fault coverage. The entire testing scheme is designed as well as simulated using Quartus II 9.1 simulated design software. In future this work will be extended in to modify TPG without affecting the MSIC vector and low-transition density. However the design through software verification only provides the sufficient results to users and this TPG named as “BIPARTITE-LFSR”.

KEYWORDS: BIST, Low Power, LFSR.

1. INTRODUCTION

Built-in Self Test, is the technique of designing additional hardware and software feature into integrated circuits to allow them to perform self-testing, i.e., Testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE).

The main drivers for the widespread development of BIST technique are the fast-rising costs of ATE testing and the growing complexity of integrated circuits. It is now common to see complex devices that have functionally diverse blocks built on different technologies inside them. Such complex devices require high-end mixed signal testers that posses special digital and analog testing capabilities. BIST can be used to perform these special tests with additional on-chip test circuits, eliminating the need to acquire such high end testers.

Logical Built-in Self Test, which is designed for testing random logic, typically employs a pseudo-random pattern generator (PRPG) to generate input patterns that are applied to the device’s internal scan chain, and a multiple input signature register (MISR) for obtaining the response of the device to these test input patterns. An incorrect MISR output indicates a defect in the device.

BIST is fast becoming an alternative solution to the rising costs of external electrical testing and increasing complexity of devices. This approach will find greater deployment in a wider variety of circumstances as more and better BIST techniques are developed. This does not mean, however, that BIST will eventually replace external electrical testing altogether. Still, BIST proponents are optimistic that BIST will someday be the preferred mode of testing, instead of being merely an alternating to external ATE testing as it is today.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

1.1 BIST ARCHITECTURE

The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a pattern generator, a response analyzer, and a test controller. Examples of pattern generators are a ROM with stored patterns, a counter, and a linear feedback shift register (LFSR). A typical response analyzer is a comparator with stored responses or an LFSR used as a signature analyzer. A control block is necessary to activate the test and analyze the responses. However, in general, several test-related functions can be executed through a test manager (or test controller) circuit. Consider a hierarchical application of the BIST concept.

The system consists of several circuit boards. Each board may contain several VLSI chips. The test manager at the system level can simultaneously activate self-test on all boards. The test manager on each board, in turn, activates self-test on each chip on that board. A chip test manager is responsible for executing self-test on the chip and then transmitting the result to the test manager of the board containing the chip. The board test manager accumulates test results from all its chips and transmits them to the system test manager. Using these results, the system test manager can isolate faulty chips and boards. The effectiveness of this diagnosis procedure depends on the thoroughness of the self-test implemented on chips. Thus, fault coverage is a major issue in BIST designs. Other important issues are area overhead and its impact on chip yield, additional pins required for test, and performance penalty.

At the chip level, BIST involves the application of test patterns to the logic to be tested and observation of the corresponding responses. Often, the test engineer modifies on-chip logic, using some DFT technique such as scan, so that latches and flip-flops can be controlled independently of the circuit's combinational logic. Thus, in most but not all cases, the circuit under test (CUT) consists of combinational logic.

II. PREVIOUS WORK

The low power Test pattern generator (TPG) for built-in self-test was proposed and this system generates multiple single input change (MSIC) vectors in a pattern, i.e., each vector applied to a scan chain is an SIC vector. A reconfigurable Johnson counter and a scalable SIC counter are developed to generate a class of minimum transition sequences. The proposed TPG is flexible to both the test-per-clock and the test-per-scan schemes [1]. In conventional BIST architectures, the linear feedback shift register (LFSR) is commonly used in the test pattern generators (TPGs) and output response analyzers. A major drawback of these architectures is that the pseudorandom patterns generated by the LFSR lead to significantly high switching activities in the CUT which can cause excessive power dissipation. They can also damage the circuit and reduce product yield and lifetime [2] - [4]. In a low-power BIST for data path architecture is proposed, which is circuit dependent. However, this dependency implies that non detecting sub sequences must be determined for each circuit test sequence. [5]- [7]

III. PROPOSED DESIGN

3.1 RECONFIGURABLE JOHNSON COUNTER

This paper develops two kinds of SIC generators to generate Johnson vectors and Johnson code words, i.e., the reconfigurable Johnson counter and the scalable SIC counter. For a short scan length, we develop a reconfigurable Johnson counter to generate an SIC sequence in time domain. As shown in Fig.3.1, it can operate in three modes.

- 1) Initialization: When RJ_Mode is set to 1 and Init is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than 1 times.
- 2) Circular shift register mode: When RJ_Mode and Init are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 1 times.
- 3) Normal mode: When RJ_Mode is set to logic 0, the reconfigurable Johnson counter will generate 2l unique SIC vectors by clocking CLK2 2l times.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

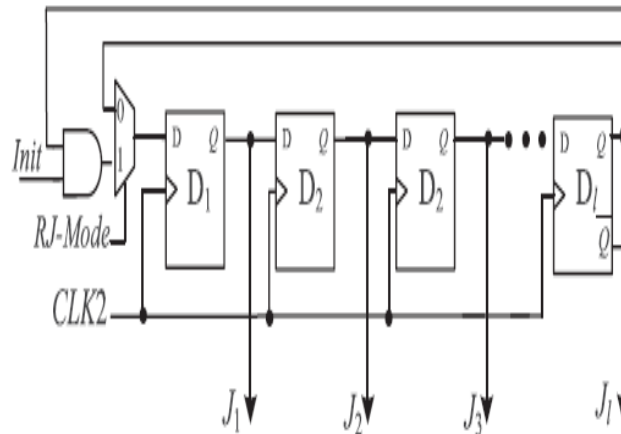


Fig: 1 Reconfigurable Johnson Counter.

3.2 SCALABLE SIC COUNTER

When the maximal scan chain length l is much larger than the scan chain number M , we develop an SIC counter named the “scalable SIC counter.” As shown in Fig. 3.2, it contains a k -bit adder clocked by the rising SE signal, a k -bit subtractor clocked by test clock CLK2, an M -bit shift register clocked by test clock CLK2, and k multiplexers. The value of k is the integer of $\log_2(l - M)$. The waveforms of the scalable SIC counter are shown in Fig.3.3 The k -bit adder is clocked by the falling SE signal, and generates a new count that is the number of 1s (0s) to fill into the shift register. As shown in Fig. 3.2, it can operate in three modes.

- 1) If $SE = 0$, the count from the adder is stored to the k -bit subtractor. During $SE = 1$, the contents of the k -bit subtractor will be decreased from the stored count to all zeros gradually.
- 2) If $SE = 1$ and the contents of the k -bit subtractor are not all zeros, M -Johnson will be kept at logic 1 (0).
- 3) Otherwise, it will be kept at logic 0 (1).

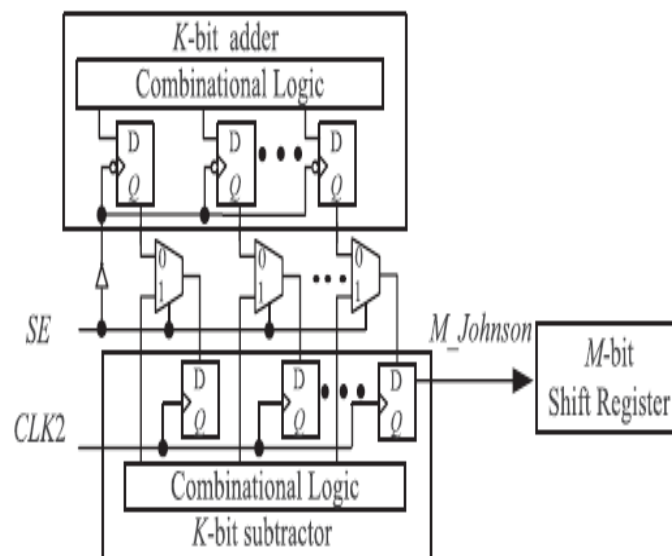


Fig: 2 Scalable SIC Counter.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

3.3 MSIC-TPGs FOR TEST-PER-CLOCK SCHEMES

The MSIC-TPG for test-per-clock schemes is illustrated in Fig. 3.3. Each grid has a two-input XOR gate whose inputs are tapped from a seed output and an output of the Johnson counter. The outputs of the XOR gates are applied to the CUT's PIs. A seed generator is an m -stage Bipartite-LFSR, and operates at low frequency CLK1. The seed generator generates a new seed by clocking CLK1 one time and the Johnson counter generates a new vector by clocking CLK2 one time. The process is repeat until $2l$ Johnson vectors are generated and also the expected fault coverage or test length is achieved.

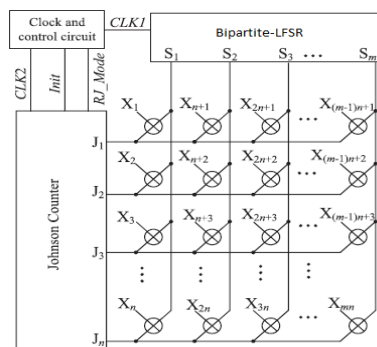


Fig: 3 Tests for Clock Scheme.

3.4 MSIC-TPGs FOR TEST-PER-SCAN SCHEME

The MSIC-TPG for test-per-scan schemes is illustrated in Fig. 3.4. The stage of the SIC generator is the same as the maximum scan length, and the width of a seed generator is not smaller than the scan chain number. The inputs of the XOR gates come from the seed generator and the SIC counter, and their outputs are applied to M scan chains, respectively.

The seed circuit generates a new seed by clocking CLK1 one time. RJ_Mode is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time. After a new Johnson vector is generated, RJ Mode and Init are set to 1. The reconfigurable Johnson counter operates as a circular shift register, and generates l Code words by clocking CLK2 l times. Then, a capture operation is inserted. The process is repeated until $2l$ Johnson vectors are generated and also the expected fault coverage or test length is achieved.

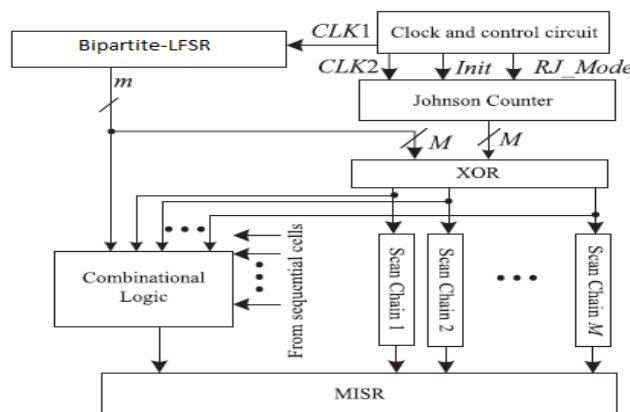


Fig: 4 Test for Scan Scheme.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

IV. RESULT

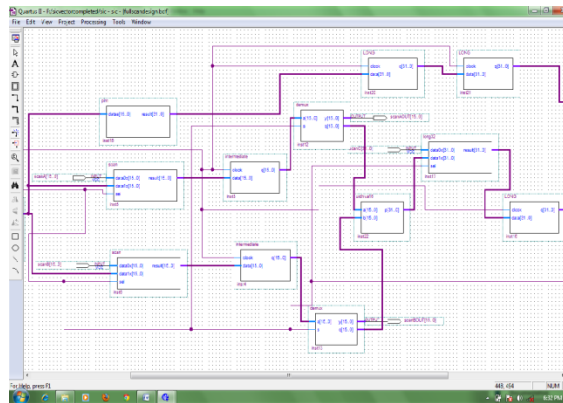


Fig: 5 Scan mode test.

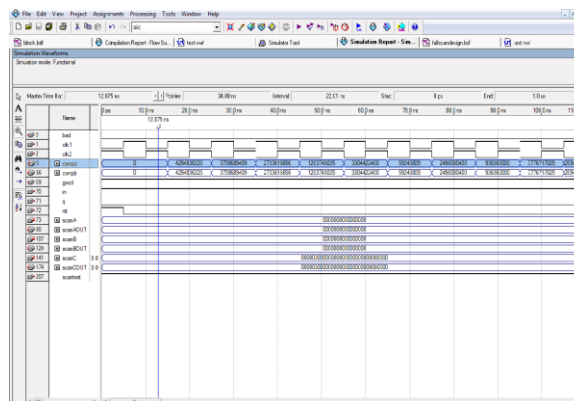


Fig: 6 Scan mode test wave form.

V. CONCLUSION

This project has proposed a low-power test pattern generation method that could be easily implemented by hardware. It also developed a theory to express a sequence generated by linear sequential architectures, and extracted a class of SIC sequences named MSIC. Analysis results showed that an MSIC sequence had the favourable features of uniform distribution, low input transition density, and low dependency relationship between the test length and the TPG's initial states. Combined with the proposed reconfigurable Johnson counter or scalable SIC counter, the MSIC-TPG can be easily implemented, and is Flexible to test-per-clock schemes and test-per-scan schemes. For a test-per-clock scheme, the MSIC-TPG applies SIC sequences to the CUT with the SRAM-like grid. For a test-per scan scheme, the MSIC-TPG converts an SIC vector to low transition vectors for all scan chains. Experimental results and analysis results demonstrate that the MSIC-TPG is scalable to scan length, and reduced the average power.

REFERENCES

- [1] Feng Liang, Luwen Zhang, Shaochong Lei, Guohe Zhang, Kaile Gao, and Bin Liang "Test Patterns of Multiple SIC Vectors: Theory and Application in BIST Schemes"(2013)
- [2] A. Abu-Issa and S. Quigley, "Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 28, no. 5, pp. 755–759, May 2009.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

- [3] N. Basturkmen, S. Reddy, and I. Pomeranz, "A low power pseudorandom BIST technique," in Proc. IEEE Int. Conf. Comput. Design: VLSI Comput. Process., Sep. 2002, pp. 468–473.
- [4] S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, "Low-power scan design using first-level supply gating," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 3, pp. 384–395, Mar. 2005.
- [5] F. Corno, M. Rebaudengo, M. Reorda, G. Squillero, and M. Violante, "Low power BIST via non-linear hybrid cellular automata," in Proc. 18th IEEE VLSI Test Symp., Apr.–May 2000, pp. 29–34.
- [6] P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, and H. Wunderlich, "A modified clock scheme for a low power BIST test pattern generator," in Proc. 19th IEEE VTS VLSI Test Symp., Mar.–Apr. 2001, pp. 306–311.
- [7] X. Kavousianos, D. Bakalis, and D. Nikolos, "Efficient partial scan cell gating for low-power scan-based testing," ACM Trans. Design Autom. Electron. Syst., vol. 14, no. 2, pp. 28-1–28-15, Mar. 2009.
- sss