

IG-FinFET Based 6T-SRAM Design Using SVL Technique

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ABSTRACT: CMOS devices are shrinking to nanometer regime, increasing the consequences in short channel effects and variations in the process parameters which lead to cause the reliability of the circuit as well as performance. To solve these issues of CMOS, FinFET is one of the promising and better technologies without sacrificing reliability and performance for its applications and the circuit design. To minimize short channel effects, FinFET is used. In previously proposed SVL leakage reduction techniques, SRAM is designed using a CMOS technology and that technique gives a 98% advantage of reducing a leakage power. This paper shows the design of FinFET based SRAM using Self Controllable Voltage Level and Stack Technique. Power consumption and delay is reduced when compared with FinFET 6T- SRAM. The power consumption and delay is less for Stack and SVL technique.

KEYWORDS: FinFET, Stack Technique, Self Controllable Voltage Level Technique, SRAM, Short Channel effects.

I. INTRODUCTION

FinFETs have been proposed as a promising alternative for future technologies because of their better gate control of the channel with that of conventional bulk MOSFET. Among the different DG devices the quasi-planar structure of FinFETs device width can be increased only in quanta of the fins height and effective gate width is $2nh$, where n is the number of fins and h is the fin height. FinFET is a double gate device in which second gate is connected opposite to first gate.

With today's technological changes there is a huge demand for finding out devices with low power. The demand of low power becomes the key of the VLSI designs rather than high speed particularly in embedded SRAMs and caches. Static Random Access Memory which are the key elements in register files and caches are severely affected due to aging. An SRAM cell storing the same value for a large period of time undergoes highly unbalanced stress causing substantial reduction in its reliability characteristics. A SRAM cell involves of a latch, therefore the cell data is kept as long as power is turned on and refresh operation is not compulsory for the SRAM cell. SRAM is mainly used for the Cache memory in microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to high speed and low power consumption. Static Random Access Memory continues to be one of the most fundamental and vitally important memory technologies today. Each bit in an SRAM is stored on four transistors that form two cross coupled inverters. High-performance on chip caches is a crucial component in the memory hierarchy of modern computing systems.

II. HISTORY OF WORK

In this Work, FinFET based 6T-SRAM design using Self Controllable Voltage Level and Stack technique is targeted. The leakage power and delay is reduced by using these techniques. In the Stack technique, each NMOS and PMOS transistor in the logic gates is split into two transistors. The proposed FinFET technology and SRAM memory cell consumes low power during read and write operations compared to conventional MOSFET based SRAM design. A new

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leakage current reduction circuit called “improved Self-Controllable Voltage Level” circuit is developed and included to reduce the leakage power of 10T SRAM. Leakage is the only source of energy consumption in an idle circuit.

The main contributions of this paper are given below

- It describes how SRAM cells can be designed using FinFET technology by using Self Controllable Voltage Level Technique.
- The circuit for SVL and Stack technique is discussed.
- The simulation results of modified FinFET based 6T-SRAM using Self Controllable Voltage Level and Stack Technique

III. LEAKAGE CURRENT REDUCTION TECHNIQUES

In modern high performance integrated circuits, more than 40% of the total active mode energy is consumed due to leakage currents. Furthermore leakage is the only source of energy consumption in an idle circuit. FinFET SRAM arrays are important sources of leakage since the majority of transistors are utilized for on-chip memory in today’s high performance microprocessors and systems-on-chips (SoCs). The design of a low leakage FinFET SRAM cell is, therefore, highly desirable.

In addition to the leakage power issues, the degradation of data stability in FinFET SRAM cells is another growing concern with the scaling of device dimensions and voltages in each new technology generation. The FinFET SRAM cell stability is further degraded due to process variations in deeply scaled CMOS technologies.

A new FinFET SRAM cell with reduced leakage power consumption and enhanced data stability is proposed in this paper. The leakage power consumption of the new FinFET SRAM cell is reduced by 99.99% as compared to the conventional SRAM cells. The FinFET SRAM cell provides two separate data access mechanisms for the read and write operations. During a read operation, the data storage nodes are completely isolated from the bit lines, using different approach in FinFET SRAM to minimize the power.

1. FinFET SRAM Cell using stacking Technique,
2. Self-controllable Voltage Level (SVL) Technique.

1. FinFET SRAM cell using stacking technique

This improves SRAM bandwidth compared to DRAMs. A SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents.

The basic idea behind our approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. This is based on the observation made that “a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path.” In our method, we introduce two leakage control transistors in each inverter pair such that one of the leakage control transistor is near its cutoff region of operation. Two leakage control transistors (PMOS) and (NMOS) are introduced between the nodes and of the pull-up and pull-down logic of the inverter.

The drain nodes of the transistors are connected together to form the output node of the Inverter. The source nodes of the transistors are connected to nodes of pull-up and pull-down logic respectively. The switching of transistors is controlled by the voltage potentials at nodes respectively. This wiring configuration ensures that one of the leakage control transistor is always near its cutoff region, irrespective of the input. Hence the resistance of will be lesser than it’s OFF resistance, allowing conduction. Even though the resistance of is not as high as it’s OFF state resistance, it increases the resistance of to ground path, controlling the flow of leakage currents, resulting in leakage power reduction. Thus, the introduction of leakage control transistors increases the resistance of the path from supply voltage to ground.

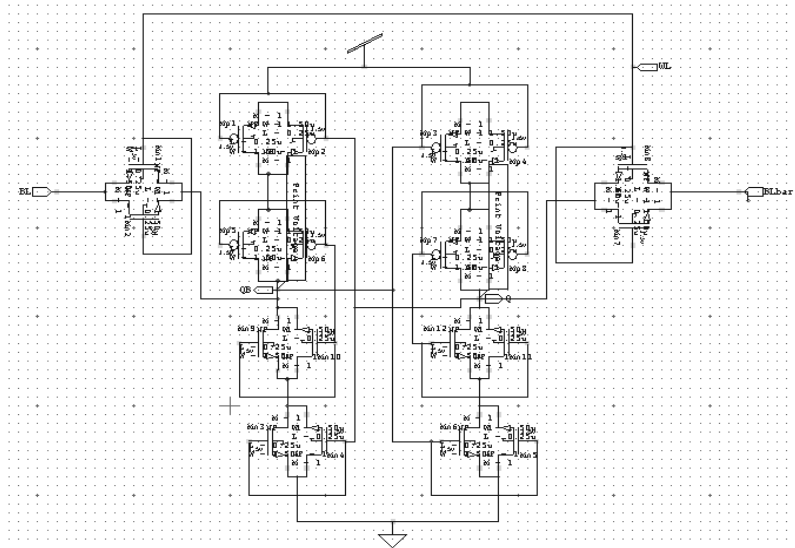


Fig.1. FinFET SRAM cell using Stacking technique

III. FinFET SRAM USING SELF-CONTROLLABLE VOLTAGE LEVEL TECHNIQUE

A FinFET SRAM which provides low leakage power is designed in this paper. A new leakage current reduction circuit called an “improved Self-controllable Voltage Level (SVL)” circuit is developed and included to reduce the leakage power of FinFET SRAM.

There are two well-known techniques that reduce leakage power (P_{st}). One is to use a multi-threshold-voltage CMOS (MTCMOS). It effectively reduces P_{st} by disconnecting the power supply through the use of high V_t MOSFET switches. However, there are serious drawbacks with the use of this technique, such as the fact that both memories and flip-flops based on this technique cannot retain data. The other technique involves using a variable threshold-voltage CMOS (VTCMOS) that reduces P_{st} by increasing the substrate-biases. This technique also faces some serious problems, such as a large area penalty and a large power penalty due to the substrate-bias supply circuits requires low leakage power.

IMPROVED SELF-CONTROLLABLE VOLTAGE LEVEL CIRCUITS

Upper SVL circuit

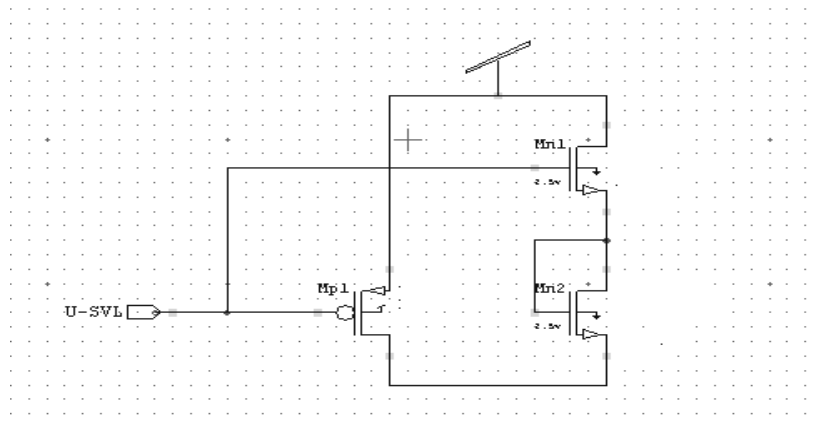


Fig.2. Upper SVL circuit

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In the above figure shows Upper SVL circuit. The impedance of a MOS transistor increases with the width of the transistor. PMOS1 in the above circuit having width means it offers very high resistance in that path between V_{dd} and V_d . So that leakage in this SVL mode is very less. And also NMOS1 and NMOS2 forms a working in normal mode of the cell. NMOS2 acts as a resistor to reduce current in active mode. By connecting above way the leakage is further reduced.

Lower SVL circuit

In the above circuit represents lower SVL circuit. NMOS3 work in the SVL mode and PMOS2 and PMOS3 work in the normal mode of the cell. PMOS2 acts as a resistor to reduce leakage. These two techniques reduce leakage current compared to the previous SVL.

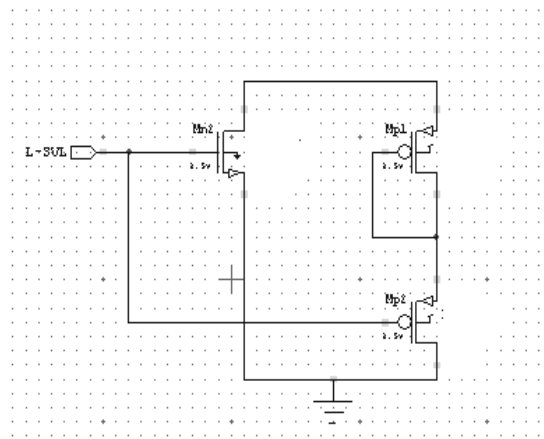


Fig.3. Lower SVL Circuit

Table 1. SRAM Cell SVL operation

Mode	Upper SVL circuit	Lower SVL circuit
Active	PMOS switch is turned on	NMOS switch is turned on
	VDD is supplied	VSS is supplied
Stand-mode by	NMOS switch is turned on	PMOS switch is turned on
	$V_D(<V_{DD})$ is supplied	$V_S(>V_{SS})$ is supplied

The role of SVL circuits is to reduce leakage currents in standby mode or hold mode because so much leakage power in standby mode can destroy the cell. So we need to reduce that leakage. The proposed improved SVL circuits can reduce leakage more. By observing the table for inputs logic 1 and 0 to the SVL circuits we can say that the cell operates in hold mode, In this mode NMOS8 on in upper SVL circuit and PMOS4 on in lower SVL circuits to reduce the leakage.

Table 2. SRAM Cell operation with SVL

u-svl	l-svl	wr	Rd	bl	blb	Qbar	q	operation
1	0	0	0	x	x	0/1	1/0	Hold
0	1	0	1	1	1	0/1	1/0	Read
0	0	1	0	0	1	1	0	Write 0
0	0	1	0	1	0	0	1	Write 1

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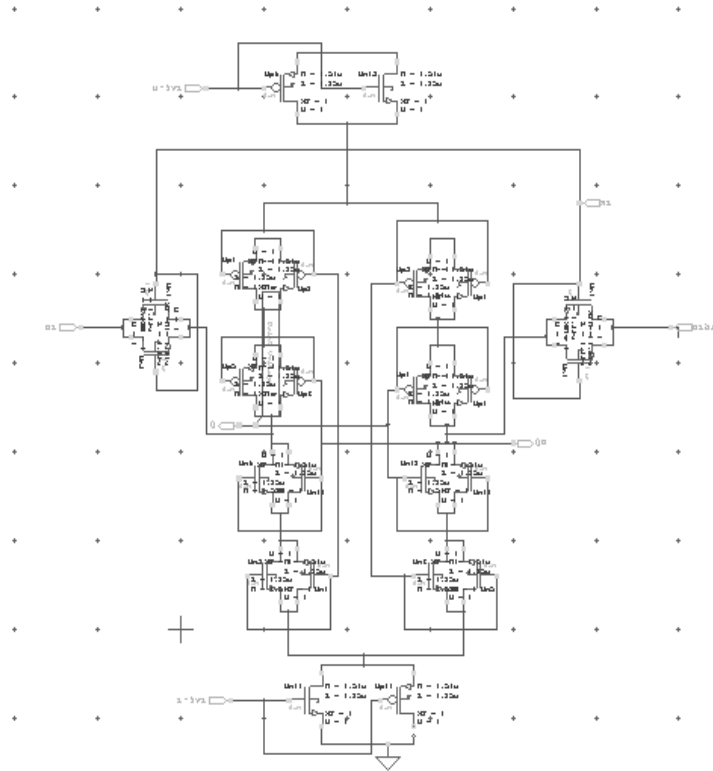


Fig.4 FinFET SRAM Cell with Normal SVL Circuits Using Stacking Technique

The above circuits work with normal SVL circuits. The circuit consists of normal FinFET SRAM cell Using Stacking Technique and upper SVL circuit and lower SVL circuits and operation of the circuit explained with the table below.

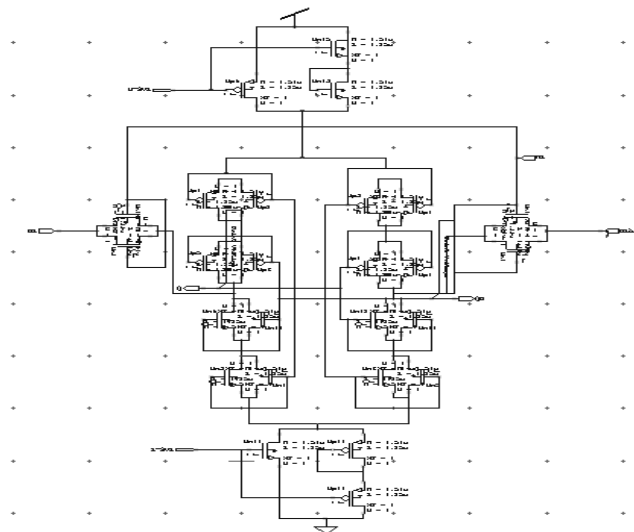


Fig.5. FinFET SRAM Cell with Improved SVL Circuits Using Stacking Technique

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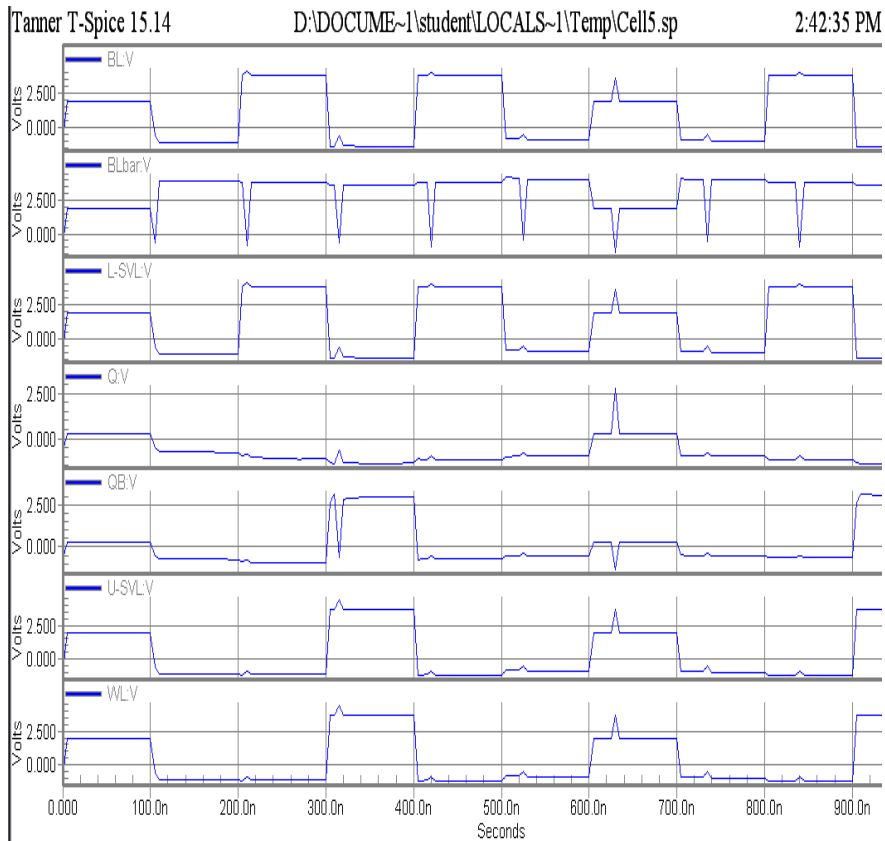
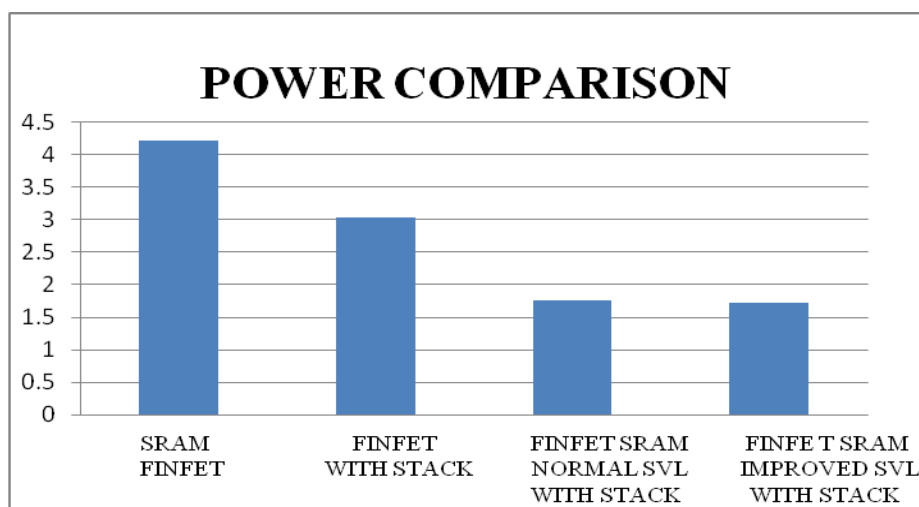


Fig.6. Simulation Result of FinFET SRAM with Improved SVL Circuits Using Stacking Technique

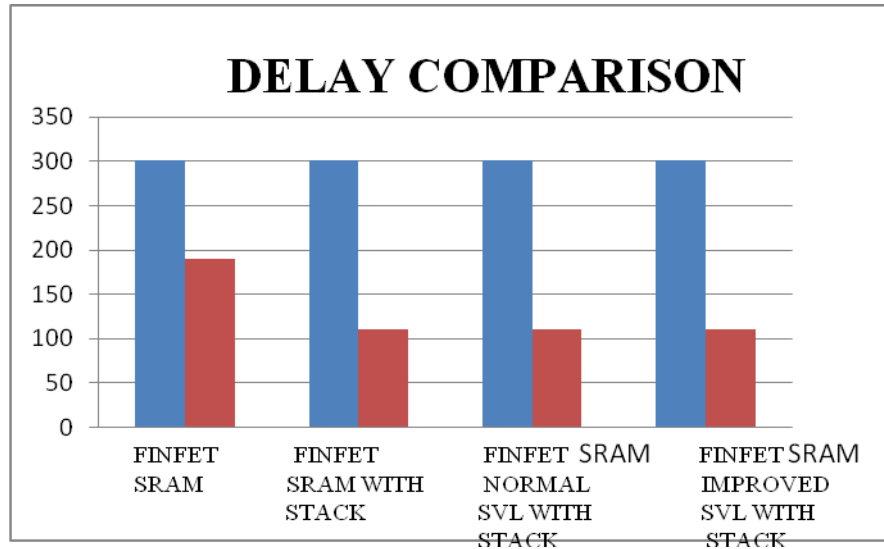
IV. SIMULATION RESULTS



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A. Power Consumption

Table.3. Power Consumption

TECHNIQUE	POWER CONSUMPTION (e-003 watts)
FinFET SRAM	4.210677
FinFET SRAM with Stack	3.033448
FinFET SRAM Normal SVL with Stack	1.755685
FinFET SRAM Improved SVL with Stack	1.730365

B. Delay comparison

Table.4. Delay consumption

TECHNIQUE	DELAY (Nano Second)	
	INPUT:BLB OUTPUT:Q	INPUT:BL OUTPUT:QB
FinFET SRAM	301.90472	190.27985
FinFET SRAM with Stack	301.80027	111.01457
FinFET SRAM Normal SVL with Stack	300.55516	110.30902
FinFET SRAM Improved SVL with Stack	300.65293	110.22285

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V. CONCLUSION

Improved SVL circuit will play a major role in future. The effect of the improved SVL circuit on the leakage current through the load circuit (i.e., reduction in current) was examined. The improved SVL circuit and the load circuit were designed using FinFET technology. Sub-threshold memory design has received a lot of attention in the past years, but most of them use large number of transistor to achieve sub threshold region operation. The new technique inherently process variation tolerant, this makes the new approach attractive for Nano computing in which process variations is a major design constraint. In this circuit we have several advantages in different modes that is in operating mode high V_{ds} to load circuits for high speed operation, in stand-by mode high V_t through -On MOS switches to load circuits for minimum stand-by leakage power, data retention, high noise immunity, small stand-by power dissipation, negligible speed degradation, negligible area overhead, high noise immunity, data retentions at stand-by mode. In this circuit the standby leakage power is reduced by which total average power also reduced and delays in FinFET SRAM Cell.

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