

Design of an Efficient Pulse Shaping FIR Filter Architecture for Digital Up Converter

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ABSTRACT: Most of the area occupied in the design of FIR filter is the multiplier. The low power and area architecture of pulse shaping FIR filter for digital up converter was designed. In the existing system, the two bit binary common sub-expression based binary common sub-expression elimination algorithm and shift and add method was used to generate the partial products. In this paper, carry save adder is used instead of shift and add method and also the simple arithmetic adders of multiplexer unit is replaced by carry save adder. The number of additions and multiplications are reduced using this technique. The designed pulse shaping FIR filter is synthesized and simulated using Xilinx ISE 12.1.

KEYWORDS: BCSE, shift and add method, FIR filter, Carry Save Adder, Digital up converter.

I. INTRODUCTION

Software Defined Radio (SDR) technology is significantly used in wireless communication and it refers to the class of reconfigurable radios in which the physical layer behavior can be flexible through reconfiguration. In the SDR system, FIR filters are mostly used in Digital Up Converter and Digital Down Converter. Digital Up Converter (DUC) is widely used in communication systems for converting the signal sample rate. It is needed when the signal is transmitted from baseband signal to Intermediate band. The input signal which is given to the DUC is filtered and transformed into higher sampling rate and then the signal is modulated with carrier signal. The various sections of Digital Up Converter (DUC) have been optimized individually and then compound in concert. The digital signal processing application using variable sampling rates can improve the flexibility of a software defined radio. It reduces the need for expensive anti-aliasing analog filters and enables processing of different types of signals with different sampling rates. It allows partitioning of the high-speed processing into parallel multiple lower speed processing tasks which can lead to a significant saving in computational power and cost.

Ankita Mandal [1] had surveyed the reconfigurable FIR filter architectures by analyzing various methods for low power consumption. While using the Common Sub-expression Elimination (CSE) method, it limits the filter coefficients and adder operation was reduced. So that the overall area consumption was increased and the number of registers also increased. Then Canonic Signed digit (CSD) was analyzed and it is not suitable for reconfigurability and the number of adders was minimized. Constant Shift Method (CSM) had been analyzed; by constant shifts the multiplication operation was performed. When using this method, it consumes more power and speed of the operation also increased. Programmable Shift method was reviewed, the speed of the operation was reduced due to the delay occurred.

Baha Ali Nasir [3], designed the architecture of MAC FIR filter for SDR system to make area efficient and to reduce the multiplication operation. For this, in the FIR filter, polyphase multiply accumulate (MAC) was used to consume the power by the reduction of multiplication operation. It supports the multichannel data operation and also it supports the polyphase decimators and interpolators for all the type of filters. To avoid the overflow, the internal paths are provided inside the MAC unit. To optimize the error, the programmable FIR filter was developed. The linear phase equiripple was used to eliminate the interference. In this MAC filter architecture was reviewed and analyzed by using Xilinx.

Durairajaa,N.[4] intended the low power and area efficient reconfigurable FIR filter architecture with low complexity. CSE algorithm was used to consume the power and the identical bit patterns are ignored without increasing the filter coefficients. It is merely depend on the extension of conventional two nonzero bit Common Sub-expressions (CSs) in

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to form three nonzero bit and four nonzero bit Super Sub-expressions (SSs) by identical shifts between a 2-bit CSs and a third nonzero bit or between two bit CSs. The CSE techniques used the CSs that takes place within the CSD representation of the filter coefficients called Horizontal Common Sub-expressions (HCSs) and that occur among the adjacent coefficients called Vertical Common Sub-expressions (VCSs) to eliminate redundant computation.

Jijina,G.O.[5] designed the FIR filter architecture with reconfigurable for SDR system. Programmable Shift Method (PSM) was used where the Processing Element comprises of programmable shifters, hence the area and the power consumption of the designed filter were minimized.

Mahesh, R.[7] designed the FIR filter architecture with reconfigurability and low complexity. In this, programmable shift method and constant shift method was used to compact the area and power. The programmable shift method was used to maximize the operation speed. Then constant shift method was used to minimize the area and power.

Marcos Martínez-Peiro,[8] designed the high speed multiplierless filter based on the non-recursive signed Common Sub-expression algorithm. For this, CSE method was used, in which it is based on graph dependence algorithm that produce unique coefficients depends on previous value. This method had been altered and demonstrated, in which the logical depth was increased and the Logical Operators (LO) were minimized. Then non-recursive Signed CSE algorithm was presented which uses similar LO and the LD was reduced. From that, it achieves the better performance in terms of area and power. Then it also maximizes the speed of the operation.

Pramod Kumar Meher[11] developed the FIR filter based distributed arithmetic using systolization to accomplish area and power. In the developed system, parallel and pipeline processing and multipliers were used to yield high throughput and the systolic architectures were introduced for simplicity, so that, it maximizes the area of the design. Then multiplierless Distributed Arithmetic (DA) based technique was used, through which it achieves high throughput but it limits the area. It uses LUT which is well suited for shift and add operation. DA based Least-Mean-Square (LMS) method and FIR filter based PARO design methodology was presented for subsequent memory decomposition and also to equalize the memory.

Rajendra Rewatkar, M.[12], had presented the optimization of multirate polyphase decimator using Multiple Constant Multiplication (MCM). Then digit serial architecture were used to shrinking the hardware complexity. In the developed system, multirate rate filters were used, so that it relates with decimation and interpolation factor, hence the order of the factor was increased. To reduce this, multistage multirate filters were used which have large sampling frequency conversions. Low Pass Filter was presented for efficient transmission to overcome the large sampling rate. In the described system, the multirate polyphase filter was structured as direct form, transposed form by MCM and digit serial architecture. Direct form was mostly preferred due to its speed and performance. Then, polyphase filter was designed by using MCM and digit serial adders where the complexity was reduced and power can be consumed which improves the performance. In the digit serial architecture, the complexity of the operation was reduced using the operation of shift and add.

Thenmozhi, M. [15], reviewed the architecture of FIR filter using common sub-expression elimination algorithm. In the described system, the power and area consumption was high due to the complexity of the multiplication operation. To reduce the complexity, the addition/subtraction operations in each coefficient of the multiplier were reduced. The reduced coefficient was used in the Canonic Signed Digit (CSD) based Common Sub-expression Elimination (CSE) technique. The architectures of Constant Shift Method (CSM) and Programmable Shift Method (PSM) with reconfigurability were presented in which the complexities of the architecture were reduced. To multiply the multiple constants with single input, MCM technique was used that has been optimized. CSE technique was used to ignore the redundancy. To ignore the redundant computations in coefficient multipliers BCSE technique was used by reusing the most common binary bit patterns present in coefficients.

In this paper, the power and area can be reduced using carry save adder instead of shift and add method and also the simple arithmetic adders were replaced by carry save adder. Hence, in theoretical, the architecture of the designed filter has been reduced.

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II. METHODOLOGY

A. Data Generator

When the clock signal is applied to the data generator, the data has been mechanically furnished by sampling the input signal. The input data is sampled based on the selected value of the selection lines of multiplexer. The fig.1 shows the flow diagram representation the RRC filter.

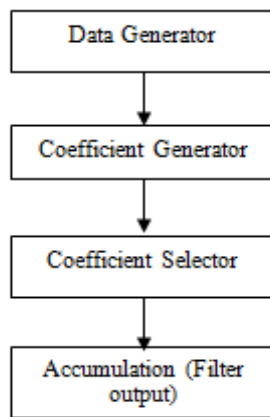


Fig .1 Flow diagram of RRC filter design

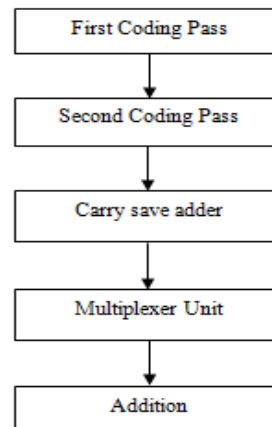


Fig.2 Flow diagram of Coefficient Generator

B. Coefficient Generator

Coefficient generator comprises of first coding pass, second coding pass, Partial Product Generator, multiplexer unit and addition. The multiplication operation between the inputs and the filter coefficients is performed by coefficient generator. The hardware usage has been reduced by two-phase optimization technique. Each of the blocks in coefficient generator are structured using multiplexer. The operation performed by the first coding pass and the second coding pass are similar.

i) First Coding Pass

It takes the input from the output produced by the data generator. The inputs are selected from the data generator are processed and the outputs are produced based on the selected values of the selection lines of multiplexer.

ii) Second Coding Pass

The operation of the second coding pass is similar to the first coding pass. It takes the input from the produced output by second coding pass. It produced the output based on the inputs selection which are processing then based on the selected values of the selection lines of the multiplexer, the output has been produced.

iii) Carry Save Adder

Carry save adder is used to generate the partial products. While using this method, the steps of addition are reduced as three to two. So that delay can be reduced and the speed has been increased. It comprises of full adders to process then it compute the sum b shifting the sequence of carry left by one and zero is appending in which the sequence is summed up with ripple carry adder. Then carry is rippled and 16-bit sum can be computed as the output.

iv) Multiplexer Unit

The output of carry save adder is shifted and it is given as the inputs to the multiplexer. It will choose the required data from the carry save adder based n the coded coefficients. The selected inputs are processed and the outputs that are produced from the mux unit are again summed up with carry save adder.

v) Addition

For addition unit, the inputs are taken as the input from the output of multiplexer unit which gets added using carry save adder and the produced outputs are varied depending on the sign magnitude and then it is given to multiplexer and produces the output.

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C. Coefficient Selector

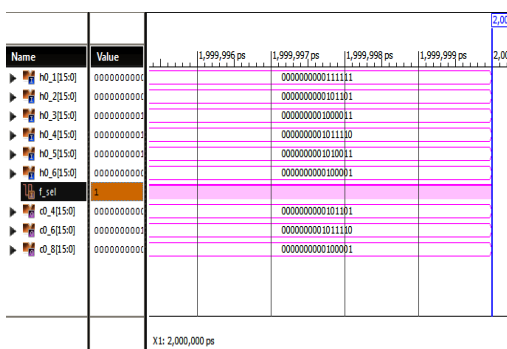
The inputs are taken from the output of the coefficient generator which selects the required data for processing. Then the selected inputs are then multiplied using the operation of AND then based on the multiplexer's selection line, outputs will be produced.

D. Accumulation

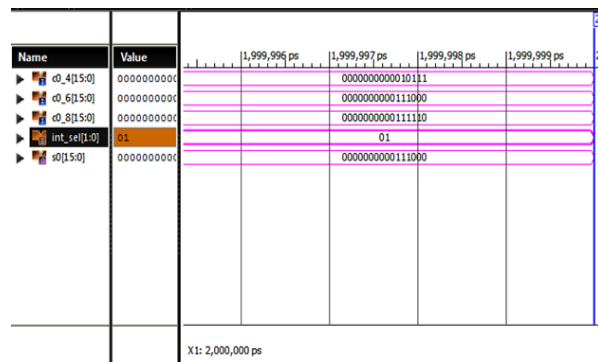
The inputs for accumulation were taken from the output of the data generator, coefficient generator and coefficient selector which are then added and the filter output will be produced.

III. RESULTS AND DISCUSSION

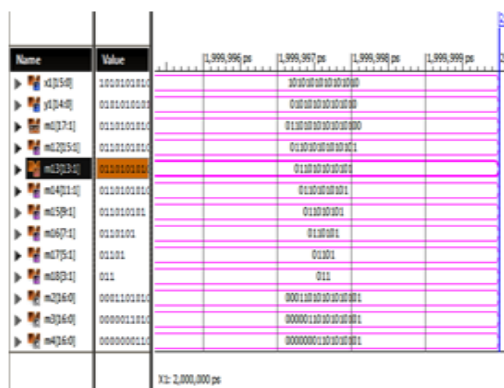
The low power and area efficient architecture of pulse shaping FIR filter for digital up converter has been designed and simulated using Xilinx. The parameters considered for the designed architecture are area and speed. The serial input data is passed to the data generator to sample the input which are then processed and produced the output based on the selected values of the selection lines of the multiplexer. In coefficient generator, the sections are first coding pass, second coding pass, partial product generator, multiplexer unit and addition unit are processing the inputs and produced the output based on the coded coefficients. For coefficient generator, the inputs are taken from the output of the data generator. Each section of the coefficient generator produces the 16-bit output. Then coefficient selector takes the input from the output of the coefficient generator and it will steer the proper data based on selection lines. Finally, the final accumulation block produces the filter output by summing up all the outputs. The output of each block is described and shown below.



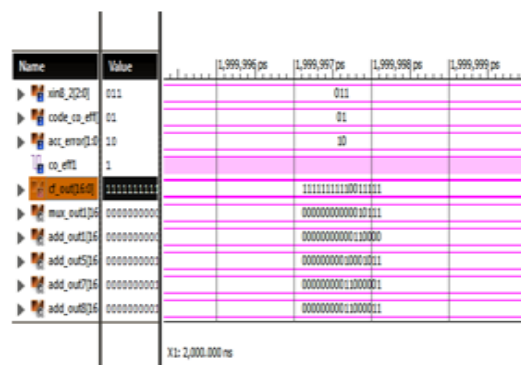
(a)



(b)



(c)



(d)

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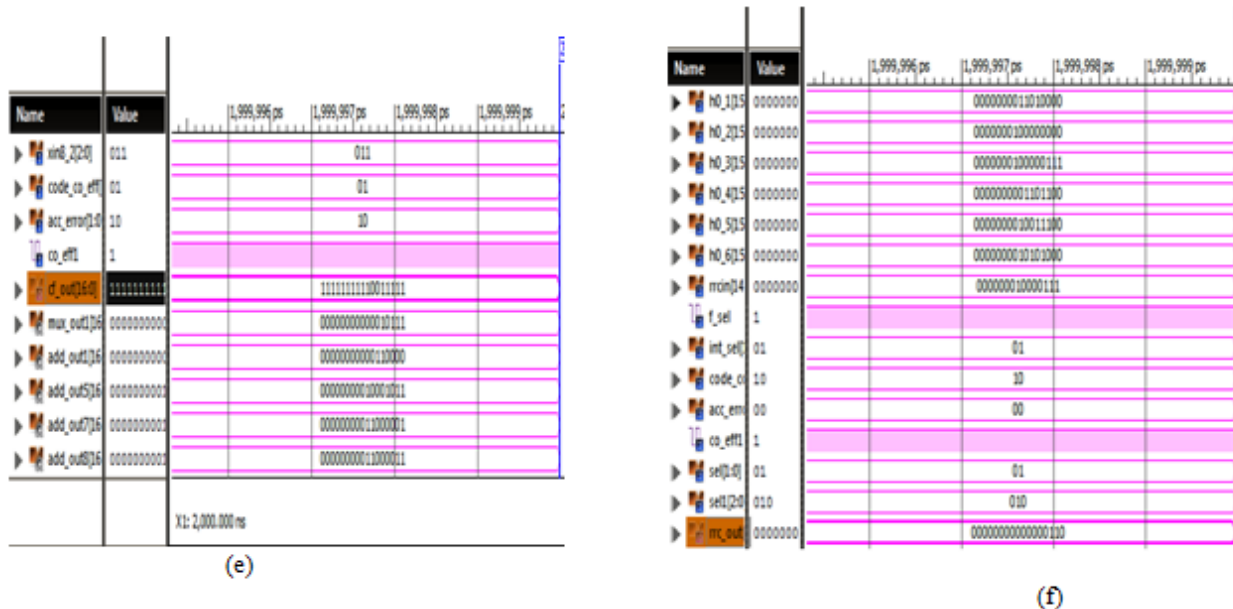


Fig.3.a output of first coding pass of coefficient generator. b. output of Second coding pass of coefficient generator. c. output of carry save adder of coefficient generator. d. output of coefficient selector. e. output of multiplexer and final addition unit.

Figure (a) shows the output of first coding pass of coefficient generator. In the first coding pass of coefficient generator, the given inputs are multiplexed and based on the selected value of the selection lines of the multiplexer; it will produce the output as 16-bit.

Figure (b) shows the output of Second coding pass of coefficient generator. It is also similar to the first coding pass of the coefficient generator. Based on the inputs multiplexed, it provides 16bit output based on the selected value of the selection line.

Figure(c) shows the output of carry save adder of coefficient generator. In this, the output from the Second Coding Pass block is then multiplexed depending on the selection line to form coded coefficient. Then carry save adder is used for the multiplying the input and filter coefficient to produce partial product output.

Figure (d) shows output of coefficient selector. In this, based on the selected values of the selection lines of multiplexer, the coefficient selector will select the required data for processing, the output will be produced based on the selected values of the multiplexer's selection line.

Figure (e) shows the output of multiplexer and final addition unit. In this, the outputs will be produced based on the inputs to the multiplexer.

IV. CONCLUSION

In this paper, reconfigurable pulse shaping FIR filter was designed for multistandard digital up converter for Software Defined Radio system. The complexity of area is caused by the multipliers. The modification to the architecture is included by which carry save adder was used to reduce the power and area consumption. So that the speed of the operation gets increased and also area of the architecture gets minimized. While using this technique, the additions and multiplications were reduced for generating the partial products. From the result, the power consumption is 0.052 of the designed filter which has been incurred using Xilinx ISE 12.1.

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