

Clock-Gated Double-Edge Triggered Flip-Flop for Effectual Power Reduction

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ABSTRACT: In recent years, mobile and portable information systems are pushing electronics and its development process. The only driving force behind the need for dramatic reduction of power dissipation in IC is to drive low-power designs. For asynchronous designs, the power consumption is mainly due to the storage elements and the clock distribution. Energy reduced from clock elements plays critical role in low-power designs. Clock gating is one of the efficient techniques to reduce the dynamic power. The use of double edge triggered flip flop instead of single edge triggered flip flop may result in significant power reduction. However incorporating the clock-gating technique with the DETFF reduces dynamic power consumption but introduces an asynchronous data sampling. Two solutions are proposed to suppress this issue in DETFFs. Each solution has its own limitations. Thus in order to overcome the drawback of the existing method, we hereby propose the DETFF method in which the positive flip-flop and negative flip-flop are connected in parallel. It is designed using one transmission gate and two inverters and the output is fed to the MUX as input. The output of MUX is then strengthened using the inverters. Thus the flip-flopped data is sent to the inverter to get absolute data at the output. This proposed method can reduce about (3-5) % of power consumption.

KEYWORDS: Clock-gating, low-power, asynchronous sampling, DETFF, MUX, inverters.

I. INTRODUCTION

In digital systems, energy consumption is the most important factor. Hence it is mandatory to reduce the energy in high-density circuits which will extend the battery life in portable systems with wireless communication capabilities. Flip-flop is the most energy consuming components of digital circuits. As a timing component in the IC, flip-flops are widely used in finite state machine (FSM) controllers, pipelined circuits and storage elements. The method of deactivating the clock can reduce power consumption to a greater extent but synchronous systems require the clock that dictates the temporal behaviour of the system. In some applications such as sequential multipliers and accumulators, energy savings of about 25% and 50% have been obtained by clock activation. Hence clock deactivation cannot effectively employ to meet the power consumption issue. In SETFF, half of the clock edges remains inactive, which leads to emergence of DETFF to utilize the idle clock edges. Hence by halving the clock frequency, the dual-edge clocking strategy can save power by about 50% of the power consumed by the clock distribution network and relax the design, while paying virtually no penalty in throughput. DETFF clocking strategy can capture the value of the input after both rising and falling clock transitions while otherwise, DETFF is non-transparent that holds the captured value only at the output. A DETFF can be classified as Latch-MUX and pulsed latch. Latch-Mux structure consists of two latches, connected in parallel and transparent latches on opposite levels of the clock and a multiplexer that selects the output of the non-transparent latch at any time. Latch-Mux is a DET counterpart of the master-slave latch clocked with the complementary clock phases. Pulsed latch consists of clock pulse generator and a transparent latch. The clock pulse generator creates a short pulse after both clock edges, which is used as the input to the transparent latch. Pulse width should be long enough to satisfy all timing requirements to implement the pulsed latches style. DETFFs can be applied to low-power application –specific integrated circuit (ASIC) designs and employed in high-level synthesis as the primary storage elements. In order to save the power dissipation on the clock-tree, power reducing techniques can be implemented with DETFFs. Clock gating is a major technique in large digital system to reduce power consumed on idle circuitry in the design. It can be done in both behavioural and circuit level. Many researchers have extended the

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

clock-gating technique with DETFFs. However the combination of clock-gating technique with double edge-triggered techniques can leads to an asynchronous data sampling. In clock-gated technique, the internal clock is isolated from global clock. Internal clock controls the gated circuits. In case the internal clock is out of phase with global clock, internal clock switches immediately to match the global clock. Hence improper synchronization of internal clock and global clock leads to an asynchronous sampling while output toggles between the clock edges. Every clock transition can result in asynchronous data sampling those results in power consumption. Two gating circuits are proposed for DETFFs to filter out the sampling issue by resuming connection between the internal and global clock The method utilizing an un-gated flip-flop can realize clock gating for original flip-flop but is ineffective for power and area. Though this minimizes the additional hardware complexity, the added complexity on timing is a serious concern while in effort to remove asynchronous data sampling. The paper is organized as follows. Section II describes the basic mechanisms with clock gated DETFF that leads to asynchronous data sampling. Two solutions are proposed and discussed in section III.

II. ASYNCHRONOUS DATA TRANSITION MECHANISMS WITH CLOCK GATING IN DETFFS

The paper describes the following terminology which discusses the operational modes of the flip-flops. **CLK**, global clock signal; **C** the (internal) gated clock signal; **CG** clock gating control signal; **D** input data; and **Q** output data. All transitions on **Q** are assumed to be synchronized with an active clock edge. To overcome the issue of data miscommunication errors due to asynchronous data sampling, clock gating technique is applied. It is done on the condition when $D=Q$ since it would be unnecessary to sample the same signal value to store into the flip-flop. Transitions on **D** assert the **CG** signal. The internal clock pulse **C** triggers the flip-flop. Two modes are observed in this paper namely non-gating mode and gating mode. During gating mode, the **C** maintaining its value throughout instead of generating an active edge. During non-gating mode, **C** changes after transition on **CLK**. When **D** changes resulting in non-gating mode, and $C \neq CLK$, output reflects asynchronous data transition. Fig 1 illustrates the data error due to asynchronous data sampling. When **D** is asserted, **CG** is disserted. A pulse appears between two clock edges that do not overlap with the setup and hold time. Hence flip-flop operates normally. The appearance of input due to asynchronous data sampling, at the output is undesirable. But the input will be passed to the output with flip-flops acting as a transparent latch.

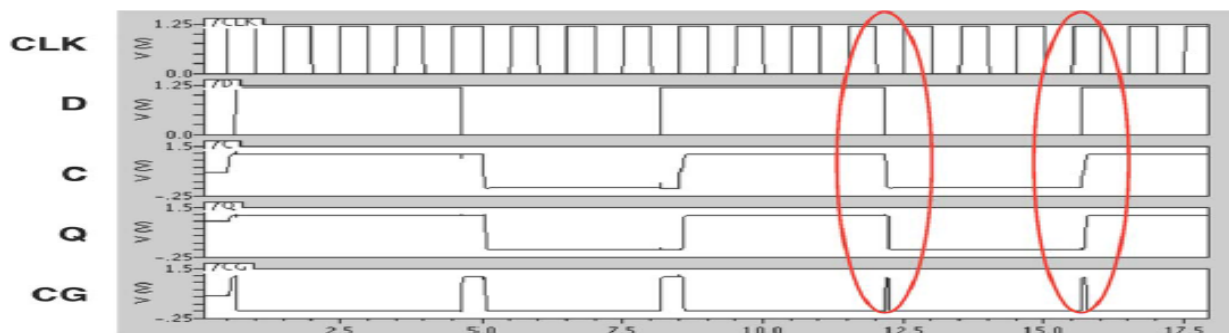


Fig.1. GDETFF's simulation of all possible switching cases and output behaviors, CLK is the external clock; D is the input; C is the internal clock; Q is the output; CG is the clock-gating signal.

The simulation is performed with CMOS 180-nm technology. C Is the Internal Clock; CLK is the Global Clock; D and Q are Input and Output, respectively; X2 and X3 are nodes. Tables I show simulation results of three ratios modified for targeted behaviours. (1) Balanced size – The rise time and fall time are similar (2) Modified I – Two possible transitions occurs at a time.(3) Modified II – Two transitions are removed. In order to analyse the asynchronous data sampling, relatively small combinations were selected for transistor sizes while balancing the rise time and fall time. There are other combinations of transistor sizes that could be used to show or hide the asynchronous transition. For Modified I, the asynchronous transitions appear for both possible cases that can be observed in Table I.

International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 4, Special Issue 6, May 2015

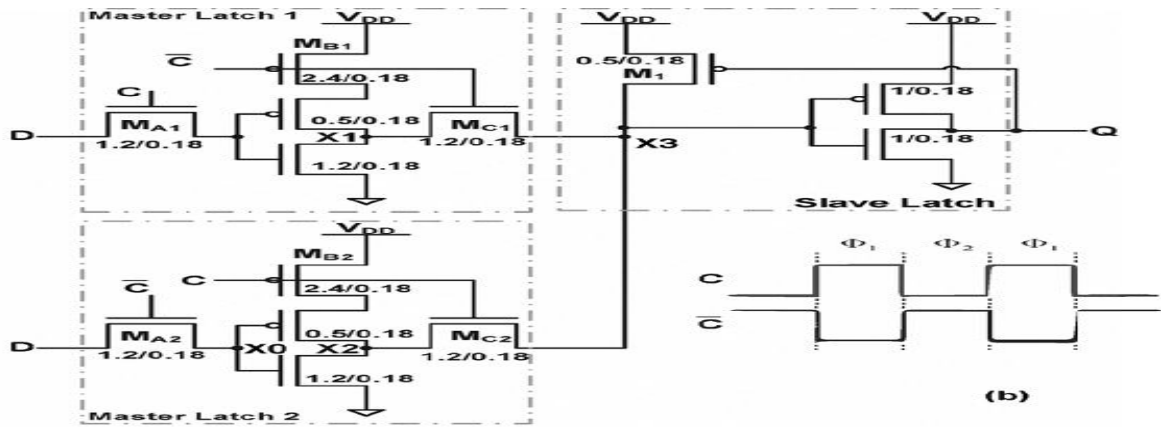
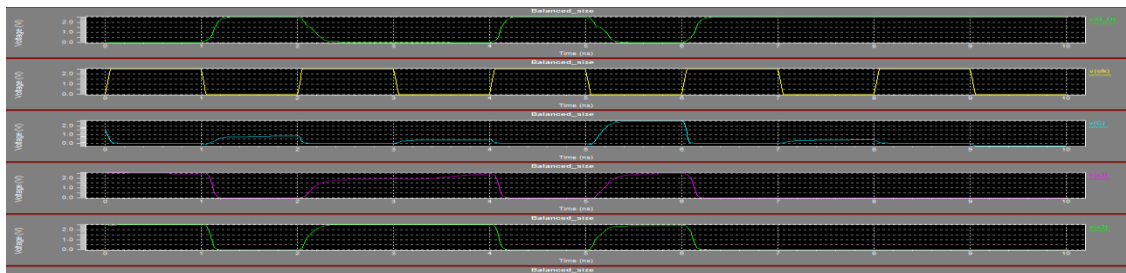
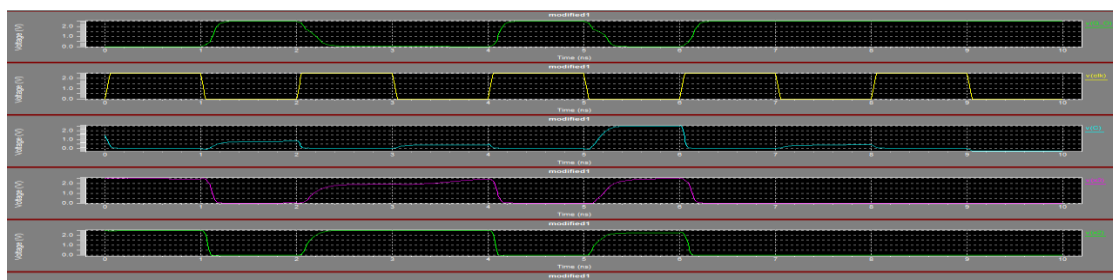


Fig.2. DHSCGFF Flip-flop circuitry Master Latch is referred to as the upper path and Master Latch 2 is referred to as the lower path.



MODIFIED I



MODIFIED II

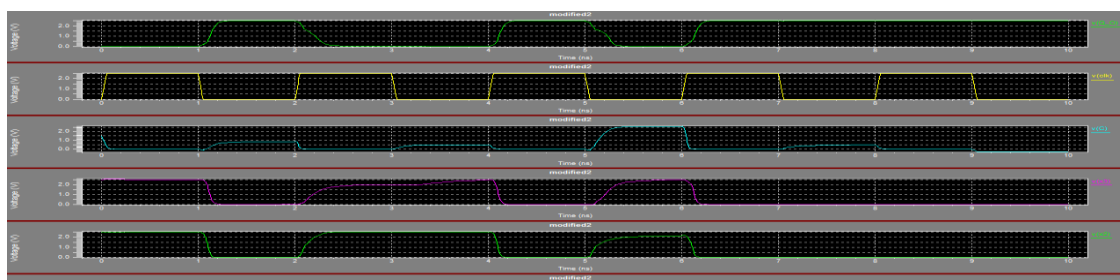


Fig.3.Simulation results of the balanced size, Modified I and Modified II module.

International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 4, Special Issue 6, May 2015

Scheme I

D and Q are compared and CLK is controlled. If D and Q varies, CLK will pass to second comparator. The CLK and C are compared and control the switch T2. This comparator removes asynchronous data sampling. However T2 remains OFF when CLK and C are not equal. Hence C will synchronize with C and in next cycle when CLK=C, T2 turns ON but the flip-flop will not be triggered. Meanwhile, the delay element creates a time delay between CLK edge and CLK & C comparator output signal. It facilitates the capturing of input data. The time delay varies with different technologies and is 68.6 ps in scheme 1 of method A.

Scheme II

The C=0 until D changes. When CLK=1, transistor P2 will be OFF at moment and C will be constant. When CLK=1, P2 will be ON and P1 also will be ON due to delay element. P1 remains same till the time to trigger the flip-flop. Hence by using IBM 90-nm PDK, the time delay is 33.6 ps. In the implementation of Method A, though D changes and comparator result is ready, the ON transmission gate T1 generates ON signal only at clock edges. The pulse generator is responsible for generating positive pulse for every clock edge. It has to be long enough to capture data. It must be minimum of 113 ps for this design. After implementation of all schemes, there exists some drawbacks.

1. Extra gates consumes more power for functionality.
2. Extra delay to remove asynchronous transition leads to D-Q prolonged time.
3. Time delay is critical for flip-flop proper operation yet it has to be tested and verified by designers.
4. The pulse generator in method B is ungated and hence constantly consumes power.

Fig. 6 shows simulation waveforms of all two schemes used to remove the asynchronous transitions. Fig. 4 is for Scheme I of Method A, Fig. 5 is for Scheme II of Method A. For each simulation, four data switching cases have been tested respectively, from left to right.

- 1) D changes from 1 to 0 before a falling edge
- 2) D changes from 0 to 1 before a rising edge
- 3) D changes from 1 to 0 before a rising edge
- 4) D changes from 0 to 1 before a falling edge.

Scheme II has better performance on power consumption. Scheme I and Scheme II of Method A have a pulse of the internal for every data switching, the DETFF will be triggered twice. Based upon the global CLK, the DETFF only triggers at one type of clock edge, which makes it a DETFF that behaves like a single-edge-triggered flip-flop (SETFF). One way to amortize the power consumed on this pulse generator is to treat the pulse generator as a global component. One pulse generator can connect to multiple flip-flops within the design. Multiple pulse generators may be needed for large circuits. The pulse generator should be carefully placed and routed to avoid the signal skew.

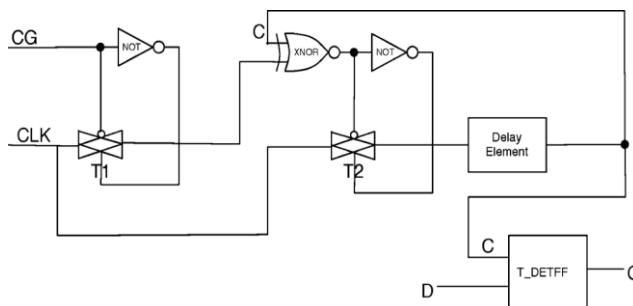


Fig. 4. Scheme I of Method A

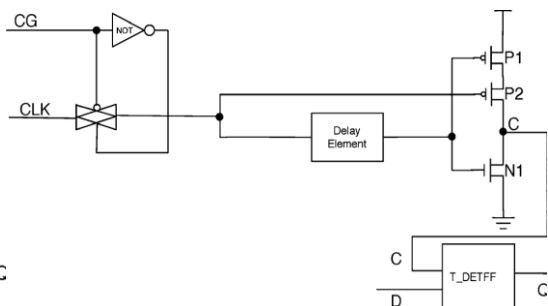


Fig. 5. Scheme II of Method A

III. COMPARISON WITH OTHER GATING STRATEGIES FOR DETFF

For the designs we studied, the clock-gating circuits that also use double edge-triggering have overlooked the asynchronous sampling problem. Two additional clock-gating schemes for DETFF have been proposed.

1. Use of another DETFF inside of the gating cell to synchronize the gating signal with the clock. It doubled the hardware cost, and moreover, the built-in DETFF is not gated.
2. Use the comparison result of the clock (CLK) and the gated clock (C) signal as a second decision condition along with the gating signal to avoid the asynchronous transition that may occur when the clock does not match the gated clock. This idea is similar to Method A Scheme I in Fig 4. The drawback is that C is always compared with CLK in this gating-cell logic, which is not power efficient. In Method A Scheme I CLK and C are only compared when necessary (i.e., new input data arrived).
3. Toggle the gated clock (C) for each clock edge when the gating signal (CG) is inactive. The same drawback occurs that uses an un-gated DETFF inside of a DETFF, which is an inefficient realization of clock gating.

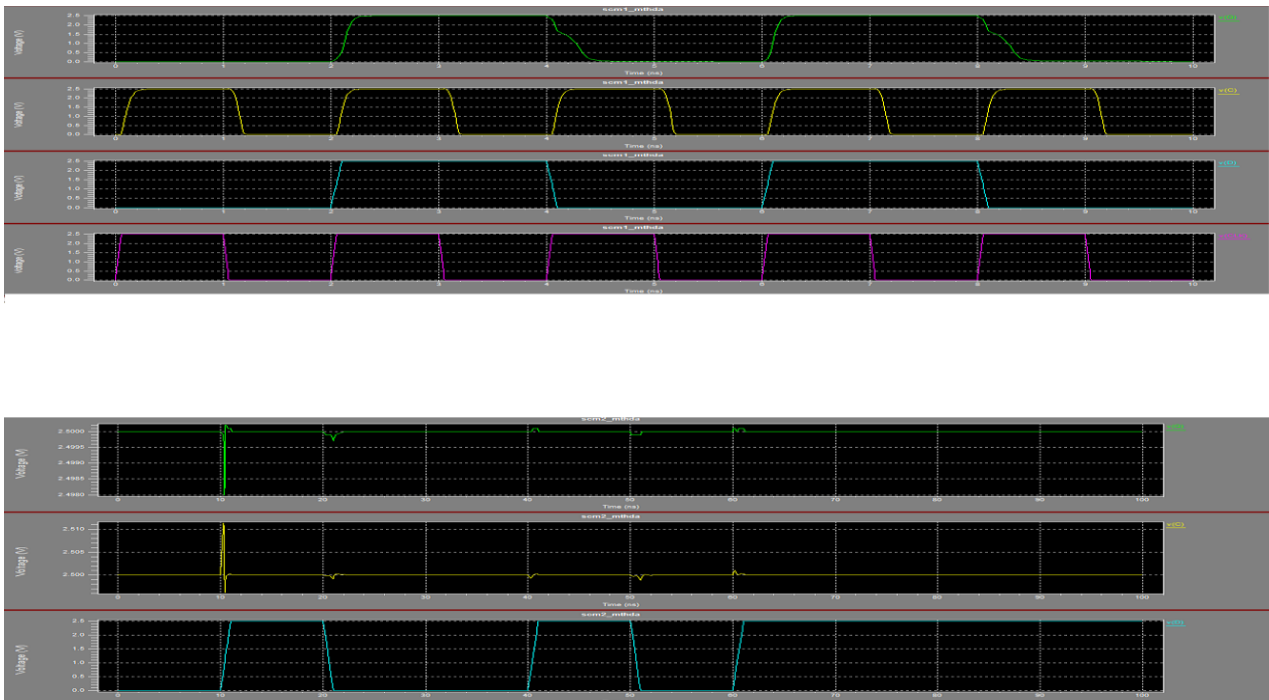


Fig. 6. Simulation results of (a) Scheme I of Method A, (b) Scheme II of Method A.

IV. THE PROPOSED DETFF FOR EFFECTUAL POWER REDUCTION

In the proposed DETFF, positive flip-flop and negative flip-flop are connected in parallel as shown in Fig.7. These flip-flops are designed using one transmission gate and two inverters connected back to back and the output of both the flip-flops are connected to 2:1Mux as input. Mux is designed using one PMOS and one NMOS connected in series and gates are connected together and derived by the inverted CLK. Output of Mux is connected to the inverter for strengthening the output. Back to back connected inverters hold the data when transmission gate is *OFF* and at the same time Mux sends the flip-flopped data to the inverter to get the correct D at the output.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

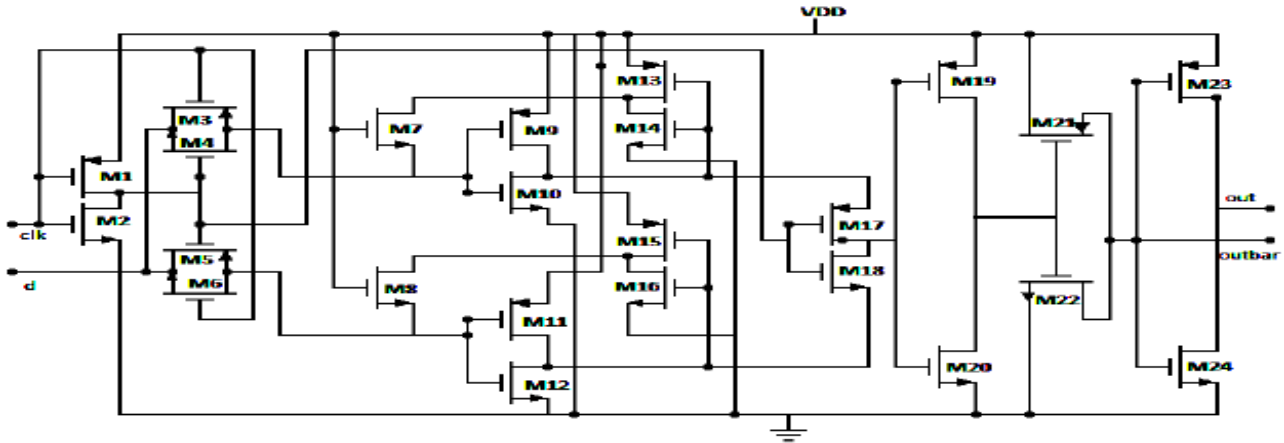


Fig. 7. Proposed DETFF with positive and negative flip-flop in parallel.

The proposed DETFF works as follows. When the CLK is low M3, M4 and M18 are ON and M5, M6 and M17 are OFF. Hence data hold by negative Flip-flop is transparent to Q. When CLK is high M5, M6 and M17 are ON and M3, M4 and M18 are OFF. If input D remains the same, Q also remains unchanged. On the other hand, if D is changed before the CLK then D will be hold by positive Flip-flop and the same value will be send to the output when CLK changes from Low to high and similarly for the transition of CLK from high to low. Thus it shows the better performance in power efficient compared to other D-Flip-Flop. It reduces the power to a greater extent, also focusing on the asynchronous sampling issue which leads to power consumption at clock edges.

IV. SIMULATION RESULTS OF PROPOSED SYSTEM

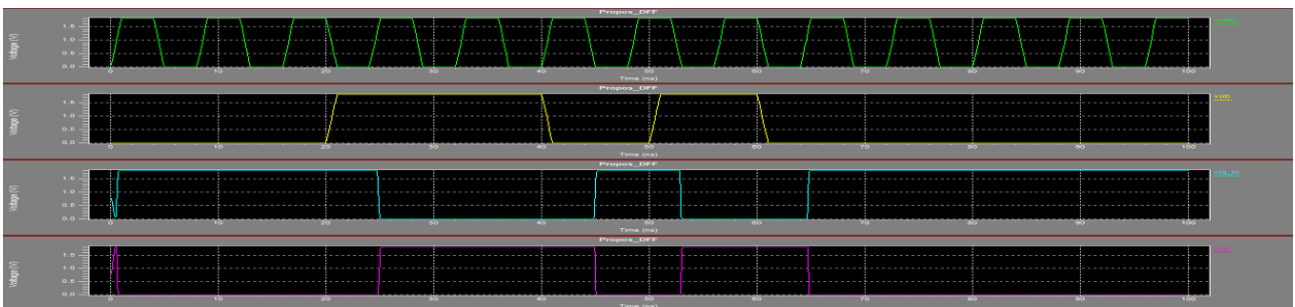


Fig. 8. Simulation result of Proposed DETFF with positive and negative flip-flop in parallel.

TABLE II
Average Power consumption

	Scheme_1 of Method A	Scheme_2 of Method A	Proposed DETFF
Average Power Consumption(μW)	118.5627	77.8880	30.564

V. CONCLUSION

In modern mobile communication systems, the flip-flops are the targets for optimization and improvement. A variety of power reduction techniques can cater the high demand of mobile devices. The DETFF integrated with clock-gated

International Journal of Innovative Research in Science, Engineering and Technology

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technique reduce dynamic power consumption. Both when used separately, data transition appear at the output between clock edges due to asynchronous data sampling that leads to more power consumption. It is considered to be a general and universal potential error condition associated with DETFF. The root cause of asynchronous transition is the uncertainty in the clock value as clock-gating signal is deasserted. If global and internal clock is not in phase, then the internal clock will change immediately, which leads to asynchronous transition. In this proposed method, the power reduction of about (3-5) % can be achieved. This method also has an added merit such as the delay of the transition to the next clock edge and the synchronization of internal and global clock. However, drawbacks of each solution in the existing method, like the prolonged Clk-to-Q time, timing uncertainty, and the increase on total power consumption are also under perception and there will be no constraints affecting these parameters.

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