

# **Area Efficient Parallel Multipliers Using Pass Transistor Logic (PTL)**

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**ABSTRACT:** In recent years, total power dissipation and area are one of the most important challenges in VLSI design. By reducing the number of transistors in the circuits and the design structures are may occupied small area and ultra-low power design. In this project based on AND gates and full adders are designed using pass transistor logic (PTL) and different techniques are used for low power in AND Gate, full adder and multipliers. The main aim of this paper is to reduce the power dissipation and area by reducing the transistors. In this project various types of parallel multiplier designs are performed. Multipliers are the major sources of power dissipation in DSP applications. The design analysis of delay and power comparison of the low power using different types of AND gates and multipliers. The designs are implemented delay and power results are obtained using Mentor Graphics EDA tool. The model technology file 0.18 um is use this design. The results show that the transistor counts, delay and the power required are significantly concentrated in the design.

**KEYWORDS:** Pass Transistor Logic (PTL), AND gate, Full adder, Parallel Multipliers, Total Power Dissipation, Delay.

## **I. INTRODUCTION**

Moore's law describes the requirement of the transistors for VLSI design it gives the practical observation that number of transistor density and performance of integrated circuits (IC), doubling every two years. The design of multiplier, full adders forms the basic building blocks of all digital VLSI design circuits has been undergoing a considerable improvements, being driven by three basic design goals, viz. reducing the transistor counts i.e reducing the area, minimizing the power consumption and increasing the speed of operation. Great effort has been determined on low-power microelectronics due to high-speed development of processors, digital equipment's, portable systems and cellular networks. Adder is the core element of complex arithmetic circuits as it is used in the arithmetic logic unit (ALU), in the microprocessor units, floating point units and for address generation in case of cache or memory access. To reduce the power and area requirements of the computational complexities, the size of transistors are shrunk into the deeply sub-micron region and for the most part handled by process engineering. Many design architecture and techniques have been developed to reduce power dissipation and area.

The pass transistor logic (PTL) describes numerous logic used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuits, as a replacement of as switches connected directly to supply voltages. Pass transistor logic often uses fewer transistors, runs faster, and requires less power than the same function implemented with the same transistors in fully complementary CMOS logic.

This paper is organized as following. Section II implementation of Pass transistor Logic (PTL) using AND gate design. Section III introduces implementation of full adder. Design of different types of parallel multipliers using AND gates and full adders section IV, Simulation and comparative analysis in table forms are shown in Section followed by the conclusion in Section VI.

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## II. DESIGN OF AND GATE USING PASS TRANSISTOR LOGIC (PTL)

The circuit performance improves in transistor count minimization. These logic circuits there are no main power source section. The supply will be forcing only the input patterns. If the circuit operation performed by an input digital or binary signals. The basic AND gate operation is, if the two inputs are same or any one of the input is one or zero then the output is produced by an AND gate is zero. If the inputs are forcing the values to one, then the output is one. The following fig. (1-2) are, 4T transistor, 2T transistor Schematic diagrams.

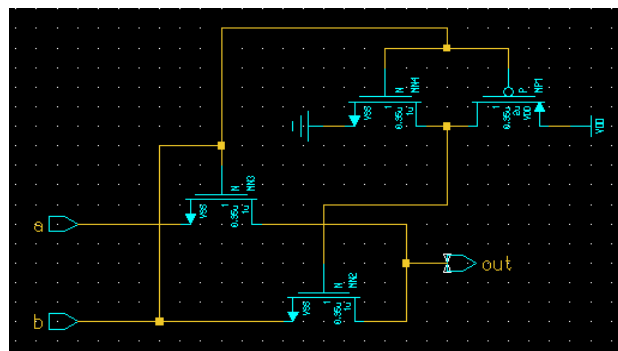


Fig.1 Four Transistor AND Gate

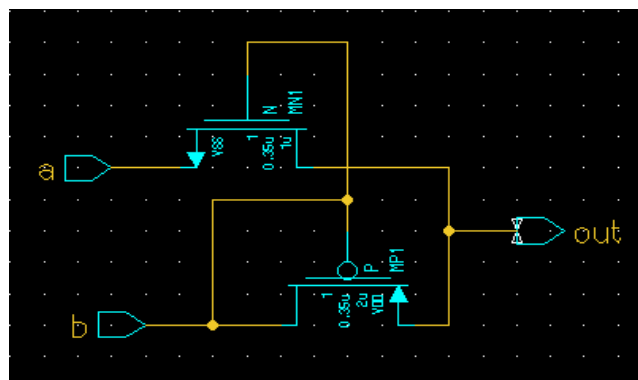


Fig.2 Two Transistor AND Gate

The four transistor AND gate is used to three NMOS transistors and one PMOS transistors and the two transistor AND gate design is used to one NMOS and one PMOS transistors. When compared to 4T to 2T the circuit occupied small area. The transistor count reduces, if the circuit Operating Speed is increased, Area and power consumption are minimized.

## III. DESIGN OF FULL ADDER USING PASS TRANSISTOR LOGIC (PTL)

The basic design of PTL full adder schematic structure, in which forms the primary building blocks of all digital VLSI design circuits, occupying more area, speed is low, and total power dissipation is high. The performance of the pass transistor logic style adders can significantly increase the performance of the full adder. The early designs are twelve or ten transistor full adders are conventionally used in most designs.

## International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 4, Special Issue 6, May 2015

The Full Adder output equation is given by,

$$\text{SUM} = A \oplus B \oplus C \text{ and}$$

$$\text{CARRY} = AB + BC + CA$$

The static CMOS Full adder is carry out by using 28 transistors. It can also minimize the number of transistors by using the CMOS Transmission gate and CMOS inverter logic. With this logic we reduce the number of transistors to 20. By using Pass transistor logic we can minimize the static power dissipation and number of transistors. Full adders design with 14 transistors, 12 transistors and 10 transistors by using Pass transistor logic, from which leads the moderate power dissipation The full adder design also implemented by using 8 transistors.

Mainly the PTL circuits are used in designing of full adder. In previous design the full adder is designed by using twelve, ten transistors. Which can dissipates more power compare to this work. The new design of 6 transistor full adder which forms the basic building blocks of all digital VLSI circuits and DSP applications. The analysis of full adders using transistor counts reduced schematic fig. (3-4) are following,

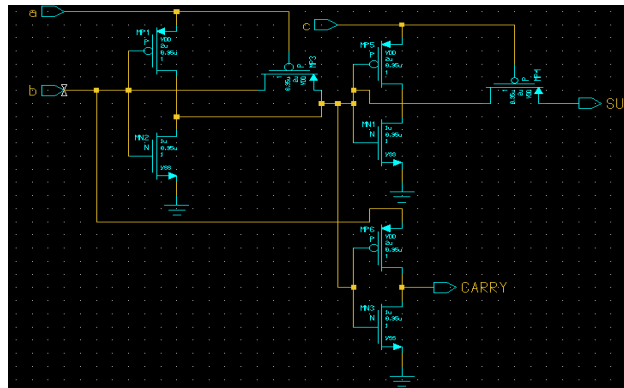


Fig.3 Eight Transistor Full Adder

In this paper the design of full adder using two transistors EX-OR gates and one inverter logic can be implemented.

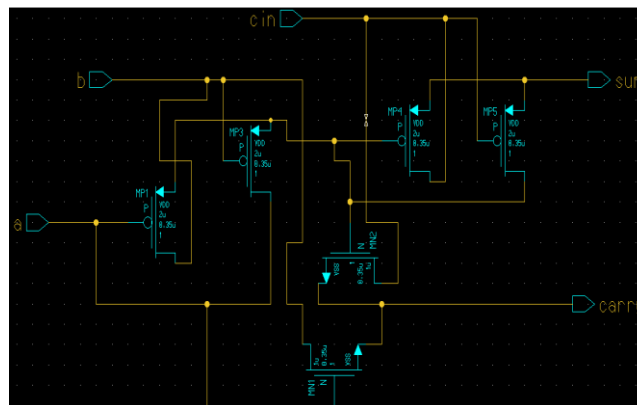


Fig.4 Six Transistor Full Adder

# International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 4, Special Issue 6, May 2015

## IV. DESIGN OF UNSIGNED PARALLEL MULTIPLIERS

High-speed multiplication is another critical function in a range of very large scale integration (VLSI) and DSP applications. Multiplications are expensive and slow operations. Multiplication is a most important basic arithmetic operation and the common operation in repetition of addition, but it is still essential for microprocessors, digital signal processors and digital calculators. Multiplication is logically carried out by a sequence of addition, subtraction and shifting operations. Therefore, high speed multiplication can be succeeded by having a high-speed multiplier. The multipliers are the structures where there will be many cascading stages of the full adders, these adders are likewise Ripple Carry Adder (RCA) and Carry Propagate Adder (CPA). So the performance of the full adders while cascading too many stages can be easily studied by analysing the power, delay, power-delay product of the various types of parallel unsigned multipliers made from different adders.

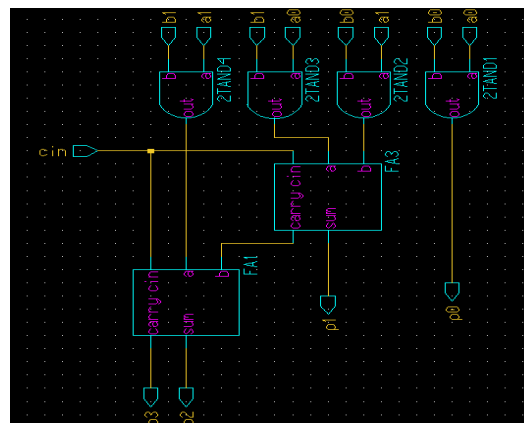


Fig. 5 2x2 Multiplier circuit

### 1. DESIGN OF BRAUN MULTIPLIER

Braun multiplier is simple parallel multiplier generally called as carry save array multiplier. The structure consists of array of AND gates and cascading of adders arranged in the iterative way and no need of logic registers. This can be called as non-addictive multipliers. In the inner structure, each products can be generated in parallel with the AND gates. Each partial product can be added with the sum of partial product which has previously produced by using the row of adders.

The carry out will be shifted one bit to the left or right and then it will be added to the sum which is produced by the first adder and the newly generated partial product. The design of full adder using Braun Multiplier diagram shown in below fig. (9-10).

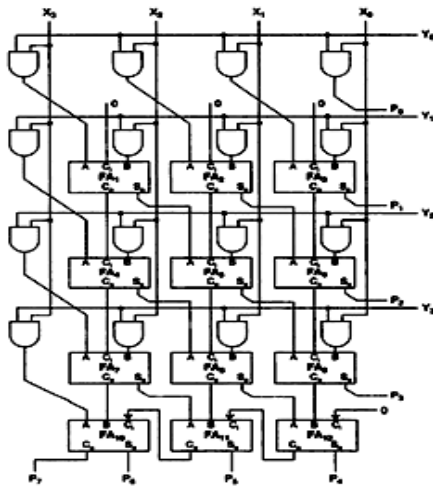


Fig. 6 Architecture of Braun Multiplier

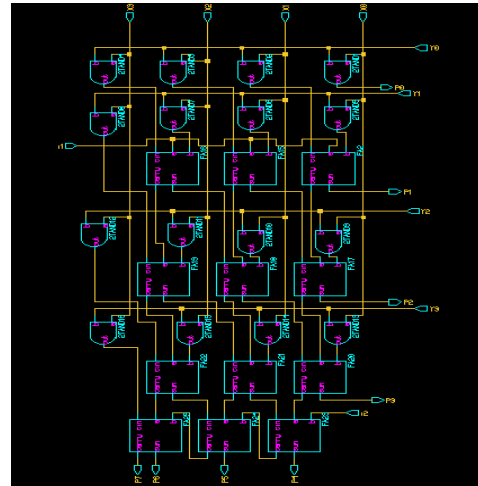


Fig. 7 Braun Multiplier circuit (4x4)

## 2. DESIGN OF ARRAY MULTIPLIER

An array multiplier very systematic structure with only short wires to nearest neighbour cells. This multiplier is very simple and efficient layout in VLSI can be easily and efficiently pipelined. Partial products are independently calculated in parallel—Consider two binary numbers  $A$  and  $B$ , of  $m$  and  $n$  bits, respectively.

$$A = \sum_{i=0}^{m-1} A_i 2^i \quad B = \sum_{j=0}^{n-1} B_j 2^j \quad \text{---- (1)}$$

$$P = A \cdot B = \sum_{i=0}^{m-1} A_i 2^i \cdot \sum_{j=0}^{n-1} B_j 2^j \quad \text{---- (2)}$$

$$P = \sum_{k=0}^{mn-1} P_k 2^k \quad \text{---- (3)}$$

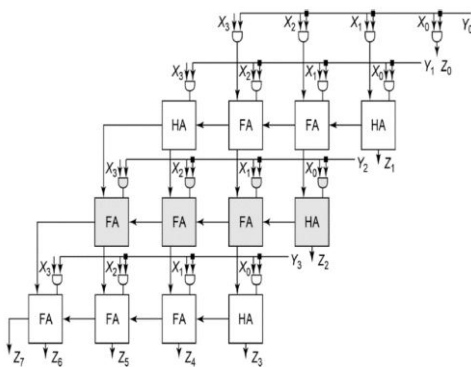


Fig. 8 Architecture of Array Multiplier

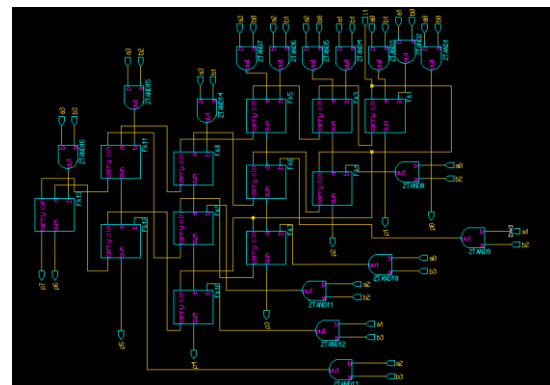


Fig. 9 Array Multiplier Circuit

# International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

Where  $P_k$  is known as the partial product term, also called the summand. There are  $m, n$  summands that are produced in parallel by a set of  $m, n$  AND gates  $n \times n$  multiplier requires  $n(n-1)$  full adders, and  $n^2$  AND gates—Worst case delay would be  $(2n+1)td$ .

### 3. DESIGN OF WALLACE TREE MULTIPLIER

A Wallace tree is an effective hardware implementation of digital circuits that multiplies two integer numbers. The Wallace tree parallel multiplier result structure is tree basis style, in this multiplier reduce the number of components and reduce the area. The Wallace tree multiplier has three steps to be followed, 1. Multiply each bit of one of the arguments, by each bit of the other, yielding results. 2. Reduce the number of partial products to two by layers of full and half adders. 3. Group the wires in two numbers, and add them with a conventional adder.

The second section works as follows. 1. Take any three wires with the same weights and input them into a full adder. The result will be an output wire of the same weight and an output wire with a higher weight for each three input wires. 2. If there are two wires of the same weight left, input them into a half adder. 3. If there is just one wire left, and connect it to the next layer.

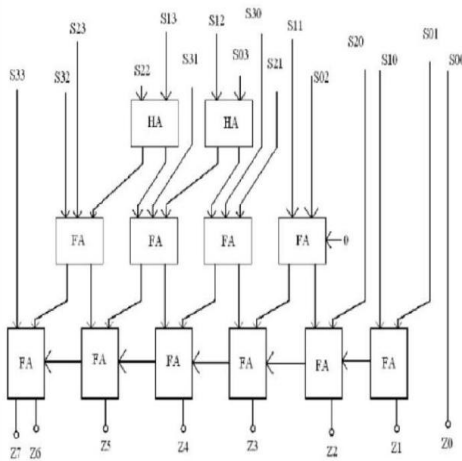


Fig. 10: 104x4 Wallace Tree Multiplier Architecture

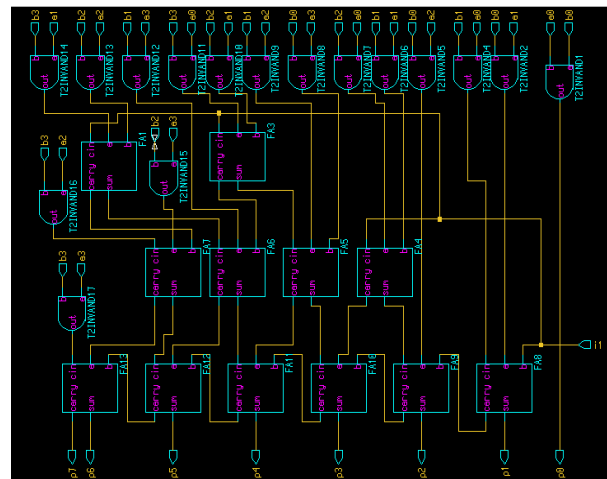


Fig. 11: Wallace Tree Multiplier Circuit

### V. SIMULATION AND COMPARATIVE ANALYSIS

In their pass transistor AND gate and full adder design shows the extraordinary improvement in power delay product. It also reduces the power consumption and minimizes the silicon area. The Consumption of power and falling and rising times which are caused due to the difference in NMOS and PMOS transistors power consumption and speed. After the simulation, the layout of circuit is drawn. Simulation results are performed by using digital schematic design tool of Mentor graphics tool. The model library files are used to 0.18um technology. The PTL AND gate, full adder and unsigned parallel Multiplier simulation results shown in fig. (12-17)

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Vol. 4, Special Issue 6, May 2015

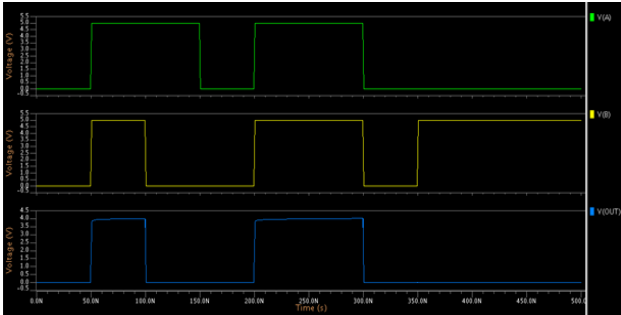


Fig. 12 Waveform of 4T AND Gate

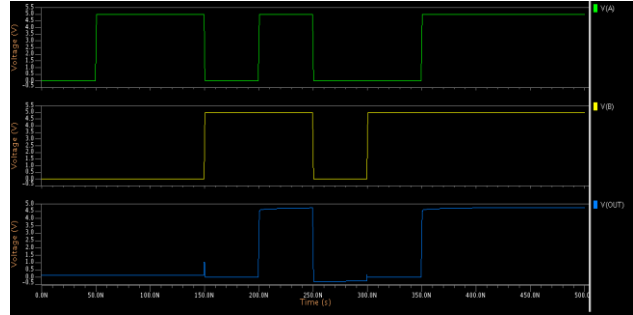


Fig. 13 Waveform of 2T AND Gate

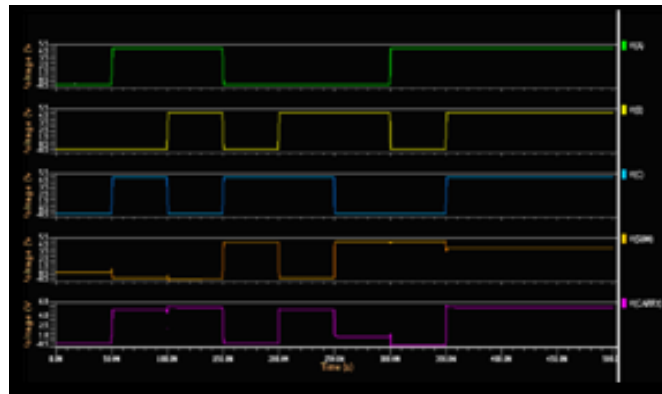


Fig. 14 Waveform of Full Adder

The output waveform of Unsigned 2x2 Parallel Multiplier is given by, inputs as a1, a0 and b1, b0, cin. Their outputs are given as P0, P1, P2 and P3.

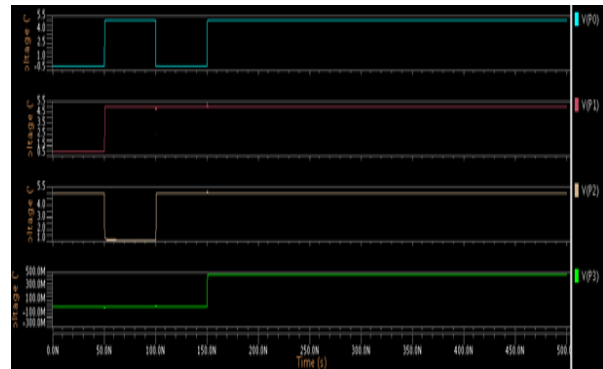
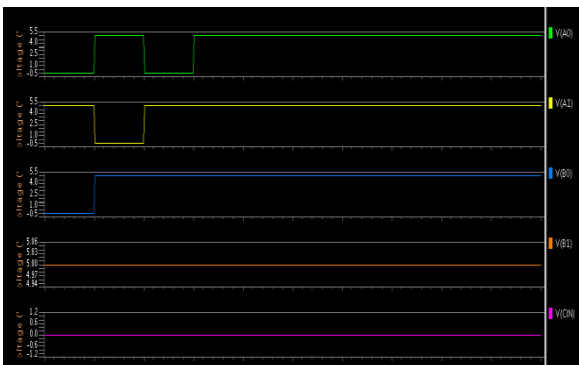


Fig. 15 Waveform of 2x2 Parallel Multiplier

The output waveform of Unsigned Parallel Multiplier is given by, inputs as a3, a2, a1, a0 and b3, b2, b1, b0, i1. Their outputs are given as P0, P1, P2, P3, P4, P5, P6, and P7.

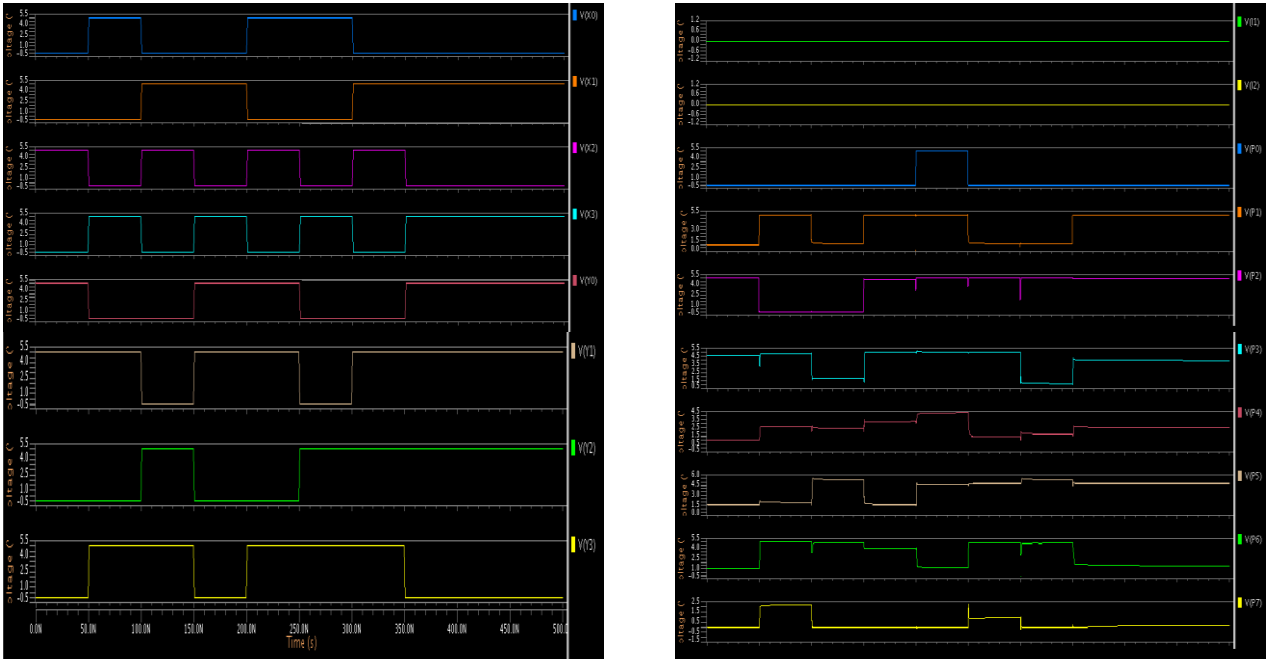


Fig.16 Waveform of Braun Multiplier

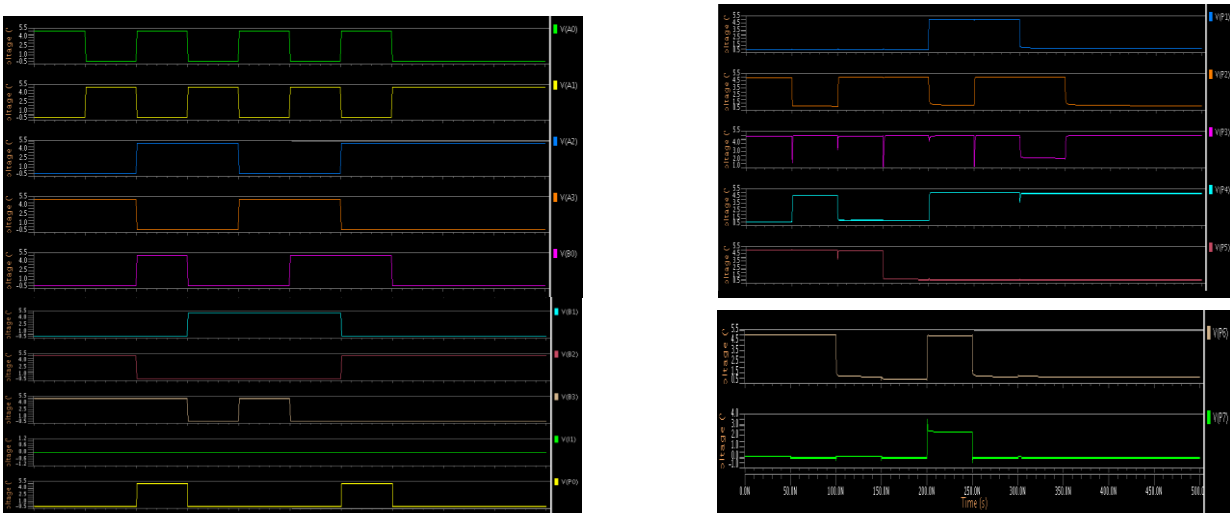


Fig. 17 Waveform of Wallace Tree and Array Multiplier

The comparison of the Pass Transistor Logic different AND gates,, Full adders and 4x4 Unsigned Multiplier are shown in tables (1-4) according to their transistor counts, delay and total power dissipation.



## International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 4, Special Issue 6, May 2015

TABLE 1 Comparative Analysis of AND Gate

AND Gate	Number of Transistors	Power	Delay
Figure 1	4T	112.509 pW	18.231 pS
Figure 2	2T	49.3442 pW	5.7829 pS

TABLE 2 Comparative Analysis of Full Adder

Full Adder	Number of Transistors	Power	Delay
Figure 3	8T	234.165 pW	50.124 nS
Figure 4	6T	124.081 pW	48.598 nS

TABLE 3 Analysis of Unsigned Parallel Multiplier using 4T AND Gate and 6T Full Adder

Multipliers	Number of Transistors	Power	Delay
2x2 Multiplier	28T	533.5184 pW	924.78 pS
4x4 Array Multiplier	136T	7.1913 nW	49.602 nS
4x4 Wallace Tree Multiplier	136T	23.1446 nW	48.617 nS
4x4 Braun Multiplier	136T	2.6140 nW	100.56 nS

TABLE 4 Analysis of Unsigned Parallel Multiplier using 2T AND Gate and 6T Full Adder

Multipliers	Number of Transistors	Power	Delay
2x2 Multiplier	20T	596.4233 pW	50.107 nS
4x4 Array Multiplier	104T	262.2485 uW	49.881 nS
4x4 Wallace Tree Multiplier	104T	2.7126 nW	18.422 pS
4x4 Braun Multiplier	104T	2.5559 nW	100.15 nS

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## VI. CONCLUSION

In this paper describes Pass Transistor logic (PTL) design families has been reviewed and evaluated based on the performance of VLSI entities like area, power, delay and transistor counts. But the previous techniques have the disadvantages of transistor count, delay and power dissipation. The 6T AND gate occupied more area and power dissipated when compared to 4T, 2T AND gate, same as for 1 8T full adders are occupied more area, power dissipation and delay when compared to 6T full adder. The unsigned parallel Multiplier is used to 4x4 binary numbers multiplied and results are efficient to previous work. In these Multiplier is used in unsigned numbers only. The future research activities may include integration of the proposed AND gates and full Adders, in both signed and unsigned numbers multiplier systems.

## REFERENCES

- [1] Khaldoon M. Mhaidat, Abdulmughni Y. Hamzah "A New Efficient Reduction Scheme to Implement Tree Multipliers on FPGAs" 2014 9th International Design and Test Symposium 978-1-4799-8200-4/14/\$31.00 ©2014 IEEE
- [2] Pakkiraiah Chakali, Adilakshmi Siliveru, Neelima Koppala "Design of High Speed Six Transistor Full Adder using a Novel Two Transistor XOR Gates". Volume 1, Issue 5, July 2012.
- [3] Pooya Asadi, "A New Optimized Tree Structure in High-Speed Modified Booth Multiplier Architecture", American Journal of Scientific Research, ISSN 1450-223X Issue 52 (2012), pp. 48-56.
- [4] S. A. Shinde, R. K. Kamat, "FPGA based Improved Hardware Implementation of Booth Wallace Multiplier using Handel C", ISSN 1392 – 1215, 2011.
- [5] C.Vinoth1, V. S. Kanchana Bhaaskaran2, B. Brindha, S. Sakthikumar, V.Kavinilavu, B.Bhaskar, M. Kanagasabapathy and B. Sharath," A Novel low power and high speed Wallace tree multiplier for risc processor" IEEE Transactions, 2011.
- [6] J.F. Lin, Y.T.Hwang, M.H. Sheu, C.C. Ho, "A novel high speed and energy efficient 10 transistor full adder design", IEEE Trans. Circuits Syst. I, Regular papers, Vol. 54, No.5, May 2007, pp. 1050-1059.
- [7] S. Goel, M.A. Elgamel, M.A. Bayoumi, Y. Hanafy, "Design Methodologies for high performance noise tolerant XOR-XNOR circuits", IEEE Transactions on Circuits and Systems – I: Regular Papers, Vol. 53, No. 4, 2006, pp. 867-878.
- [8] Jung-Yup Kang, Member, IEEE, and Jean-Luc Gaudiot, —A Simple High-Speed Multiplier Design, IEEE Transactions on Computers, Vol. 55, No. 10, October 2006, pp.1253-1258.
- [9] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 1, Feb. 2002, pp. 0– 29.
- [10] Massimo Alioto and Gaetano 'Analysis and Comparison on Full Adder Block in Submicron Technology', IEEE Transaction Very Large Scale Integration (VLSI) Systems, Vol 10, No. 6, Pp: 806 – 823, (2002),
- [11] M. Morris Mano, Digital Design, Prentice Hall of India, 2nd Edition, 2000.
- [12] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltage swing nodes," in Proc. IEEE Worksh. Signal Process. Syst., Oct. 20– 22, 1999, pp. 713–722.
- [13] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, July 1997, pp.1079–90.
- [14] E. Abu-Shama and M. Bayoumi, "A new cell for low power adders," in Proc. Int. Midwest Symp. Circuits Syst., 1995, pp. 1014–1017.
- [15] N. Zhuang and H. Wu, "A new design of the CMOS full adder," IEEE J.Solid-State Circuits, vol. 27, no. 5, May 1992, pp. 840–844.