

Removal of Asynchronous Data Sampling Error in DET Half Static and Clock-Gated D Type Flip Flop

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ABSTRACT: Now a days power consumption plays a vital role in VLSI circuits. The growing market of mobile, battery-powered electronic devices demands the design of electronic circuits with low power consumption. To design a low power circuit, energy efficiency from the clock element is an important issue. There is different technique for the energy efficiency. One of the most preferred technique is double edge triggered technique (DETFFs). To reduce the dynamic power consumption clock gating is the best technique. When we combine these two techniques it reduces dynamic power but introduces asynchronous data sampling. In this paper we are discussing two different methods to avoid asynchronous data sampling.

KEYWORDS: DETFF, clock-gating, asynchronous sampling..

I. INTRODUCTION

A conventional positive-edge-triggered flip-flop (FF) senses and responds to the control input or inputs at the time the clock input is changing from 0 to 1. It does not respond at all to changes in the opposite direction. Negative-edge-triggered FF's behave in a complementary manner. Thus, these FF's can respond at most once per clock pulse cycle. It is proposed that double-edge-triggered (DET) FF's, responding to both edges of the clock pulse, would have advantages with respect to speed and energy dissipation. One technique for efficiency is the use of double edge-triggered flip-flops (DETFFs), since they can maintain the same throughput as single edge-triggered flip-flops (SETFFs) while only using half of the clock frequency. Clock gating is another well-accepted technique to reduce the dynamic power of idle modules or idle cycles. However, incorporating clock gating with DETFFs to further reduce dynamic power consumption introduces an asynchronous data sampling (i.e., a change in output between clock edges). However an asynchronous data sampling is introduced at the output side by incorporating clock gating with DETFFs to further reduce dynamic power consumption, it causes data miscommunication error between clock edges.

This paper discusses the analysis of recent attempts to include clock-gating technique with synchronous double edge-triggered mechanisms. For a clock-gated system, the internal clock controls the gated circuits. During the gated periods, the internal clock is separated from the global clock. If the internal clock is out of phase with the global clock when the gating signal is de-asserted, then the internal clock signal switches immediately to match the global clock. This internal clock switch is extra and not synchronized with the external clock, which creates an asynchronous data sampling, evidenced by the output changing between clock edges. Each clock-gating transition has the potential to create the asynchronous sampling issue. Since the issue is not always present, the analysis in this paper examines the specific conditions that create the asynchronous data sampling. Three specialized gating circuits for DETFFs are proposed, and these circuits are evaluated for their effectiveness to address the asynchronous data sampling. Two

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approaches are designed to filter out the asynchronous data sampling by only resuming the connection between the global clock and the internal clock when they are in phase. The third approach avoids the asynchronous data sampling by synchronizing the clock-gating signal with the global clock. As a reference for comparison, another gating circuit for DETFFs has been evaluated. The design in uses an un-gated flip-flop to realize clock gating for the original flip-flop, which is inefficient for power and area. Although the mechanisms proposed in this paper minimize the additional hardware, the added complexity on timing to remove the asynchronous data sampling (e.g., uneven Hold/Clk-to-Q time) is a serious concern for applications.

II. ASYNCHRONOUS SAMPLING IN THE GATED DOUBLE EDGE-TRIGGERED FLIP-FLOP WITH TRANSMISSION GATE (G_DETFF)

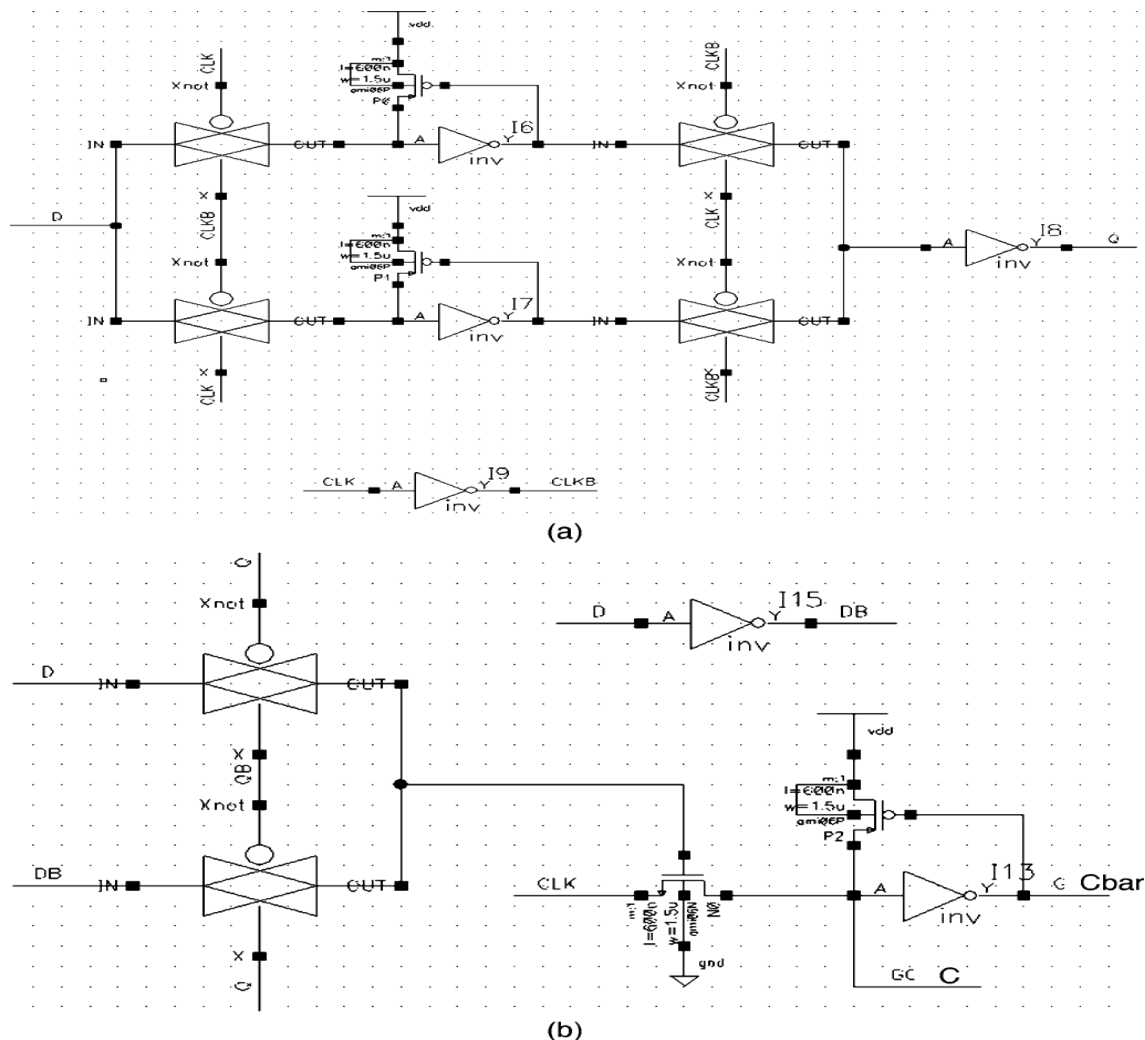


Fig. 1. Wang's design G DETFF. (a) DETFF part. (b) Clock-gating part.

This flip-flop is built with the Latch-Mux structure using transmission gates (Fig. 2). The two data paths are connected in parallel. The upper path triggers on the rising edges, while the lower path triggers on the falling edges. These two paths alternately monitor the input and provide the output, which means that the input is always preloaded into the flip-flop (i.e., only one clock edge away from the output).

Instead of generating a pulse for every transition, the clock gating part in was designed to toggle C whenever the data input changed in order to eliminate power consumption for unneeded transitions. During the gating periods, the internal C preserves the last used value before being gated. When compared to other clock gating techniques, it uses the clock signal in a more efficient way that is better suited for DETFF.

There are two variable factors when the flip-flop operates: 1) which edge triggered the flip-flop for the last transition before clock gating was applied and 2) what is the value of **CLK** when clock-gating is disserted. If the value of C does not equal the **CLK** when the circuit deactivates the clock-gating function, then the asynchronous sampling issue appears for the G-DETFF. Fig. 3 is the simulation of G DETFF that shows the existence of the asynchronous sampling issue within the design. Two asynchronous transitions occurred (circled in the figure), where D changes when $CLK \neq C$.

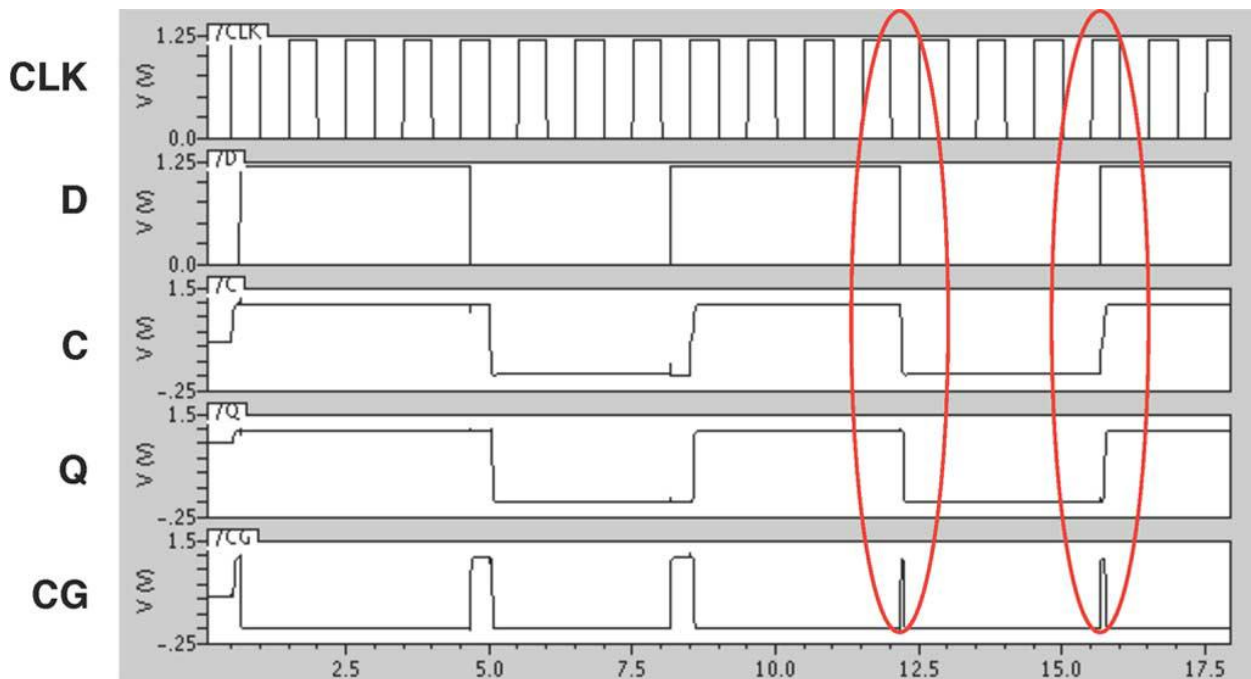


Fig. 2. G DETFF's simulation of all possible switching cases and output behaviors. CLK is the external clock; D is the input; C is the internal clock; Q is the output; CG is the clock-gating signal.

III. ASYNCHRONOUS SAMPLING IN THE DOUBLE EDGE-TRIGGERED HALF-STATIC CLOCK-GATED D-TYPE FLIP-FLOP (DHSCGFF)

The design by Tam et al uses two flip-flops and a multiplexer to implement a Double Edge-Triggered Half-Static Clock-Gated D-type Flip-Flop (DHSCGFF). The clock-gating signal is named R in Fig. 7(a). It is generated by comparing the value of input D and output Q, and is connected to a switch M_2 that controls the signal path of the global **CLK** to the internal clock C. A complementary pair of signals, C and \hat{C} , are defined by Tam et al as the internal clock signals generated from the inverter chain. Although the datapaths in Fig. 7(b) have been named as Master Latch 1 and Master Latch 2, the upper path only transmits data on the falling edge off, while the lower path transmits on the rising edge off. The gated clock signal R stays 0 when gated (inactive). So if the input data changed when $CLK=0$, then the value of C will change to 1 immediately, and \hat{C} will follow as the complement of C. An asynchronous clock edges of triggers the flip-flop, causing the asynchronous data sampling. After each data transition, the gated signal C goes back to 0 and stays low until the next transition. Master Latch 1 is always ON when the flip-flop is in standby mode. So, that means whenever a data signal is changed, Master Latch 2 will always be triggered first.

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In contrast to other Latch-Mux double edge-triggered flip-flops that place a logic keeper at Node X2 to avoid floating nodes (as well as the corresponding Node X1 in upper path), Tam's design added switches M_{B1} and M_{B2} into the latch that intentionally isolate Nodes X1 and X2. According to the schematic of Fig. 7, after the input switches and before switch M_{A2} turns OFF, the value of Node X0 starts to change. When the lower path is triggered, the switch M_{C2} turns ON, M_{B2} and M_{A2} turn OFF, and floating Node X2 drives the output. For those input events that occur during $CLK=1$ (before falling edges), the lower path would not be triggered until $CLK=0$. When it is triggered X0, has collected enough charge and is stable enough to drive X2 and allow the X2 signal to pass to X3. For transitions on D input that occur during $CLK=0$, an asynchronous pulse is generated on internal clock. Then before switch turns M_{A2} OFF, there is only a very short amount of time for Node X0 to charge or discharge. If the value of X0 is strong enough to flip the nodes to the output, then an asynchronous transition will appear at the output. Otherwise, if the first trigger of the lower path has not successfully passed the input D to the output, then the upper path serves as a backup that will be triggered at the next falling edge of C.

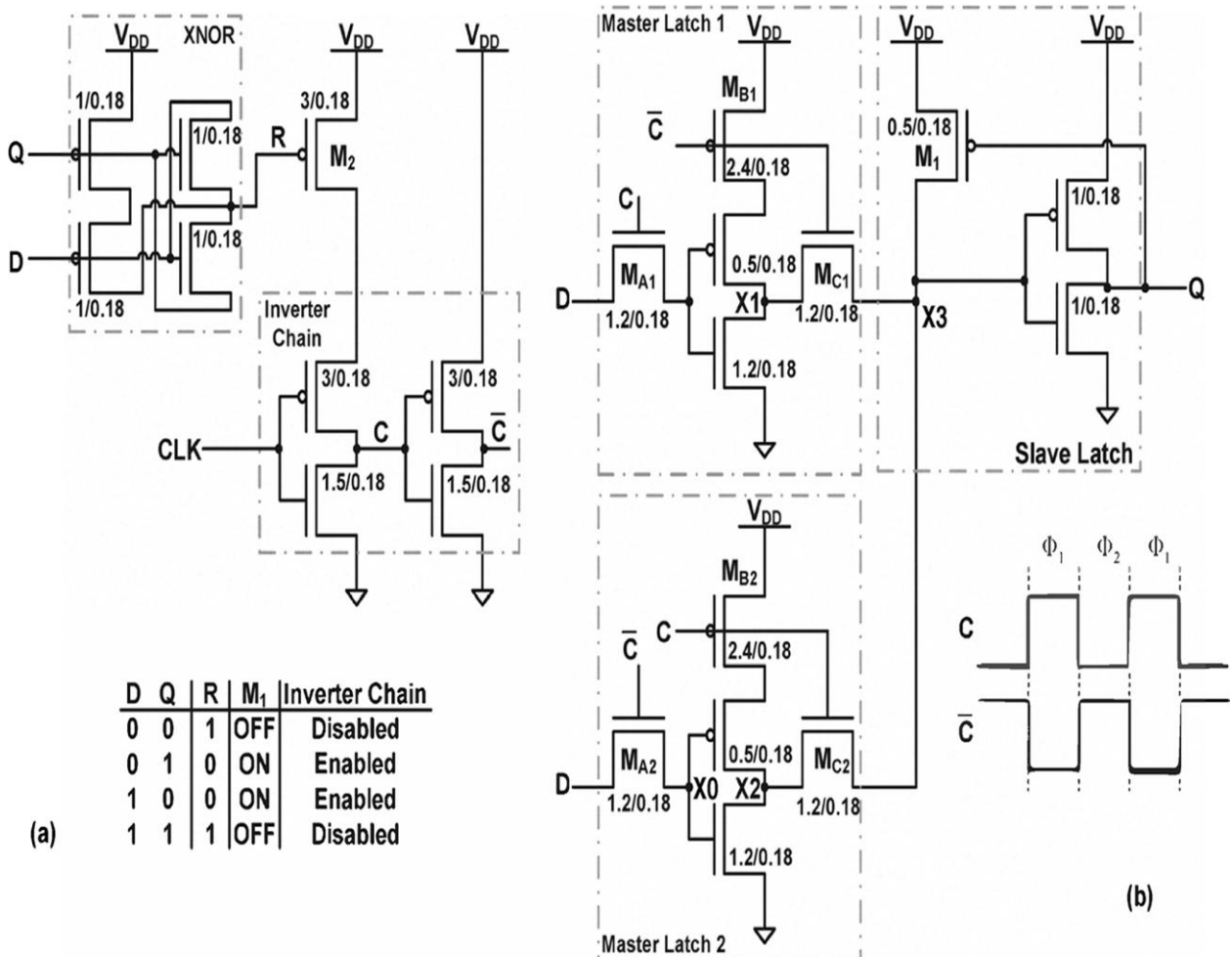


Fig.3. Tam *et al.* design DHSCGFF [22]. (a) Clock-gating and internal clock generating circuitry. (b) Flip-Flop circuitry. Master Latch 1 is referred to as the upper path, and Master Latch 2 is referred to as the lower path in this paper.

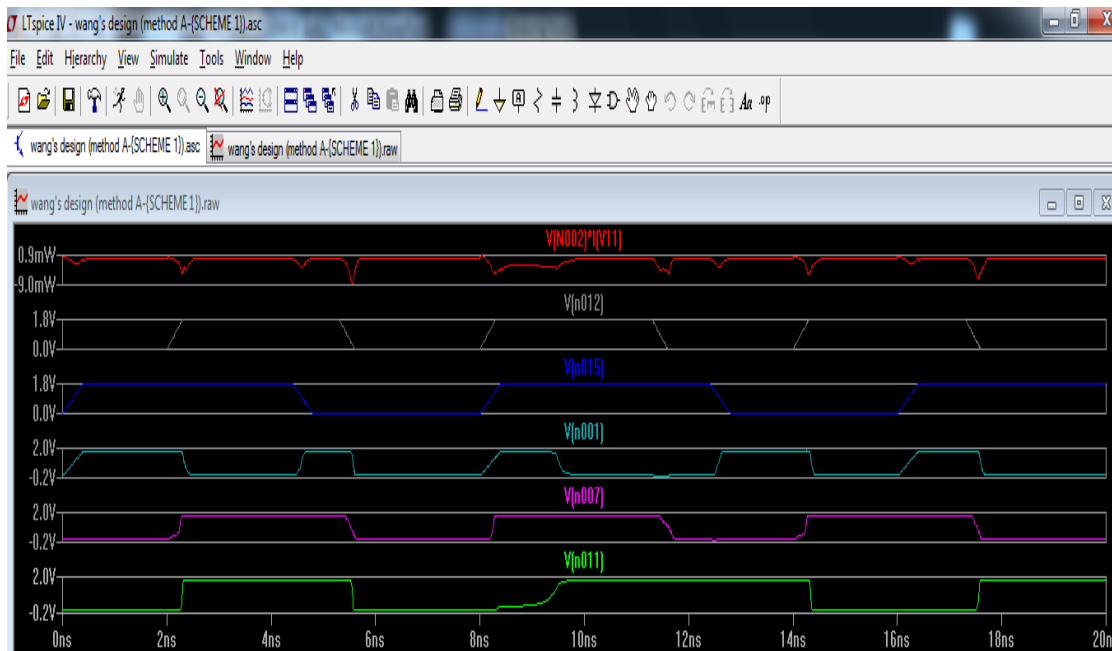
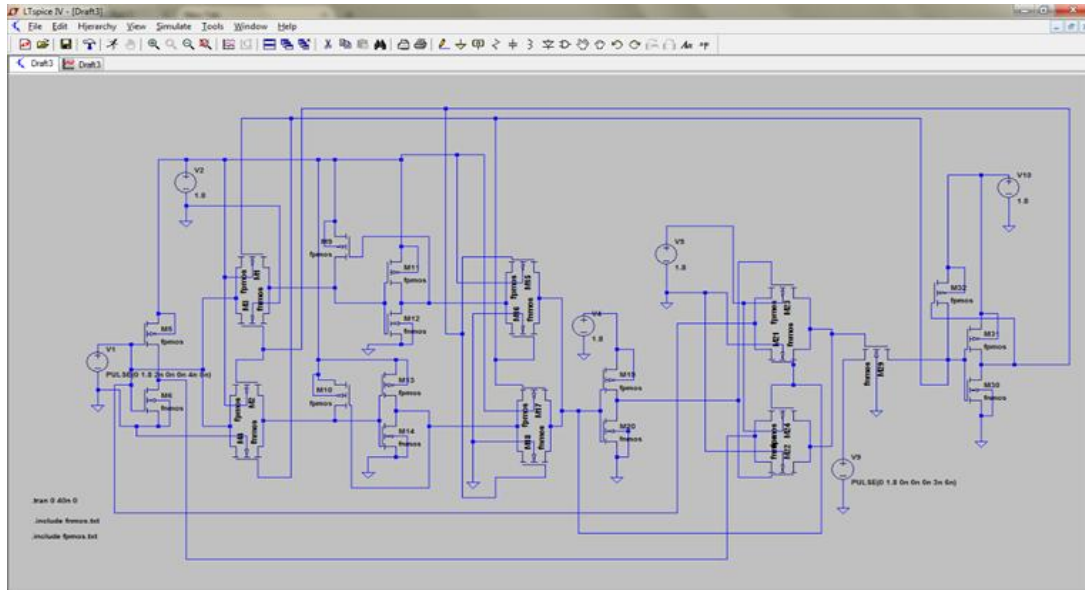
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IV. RESULTS

Asynchronous Data Sampling (G_DETFF):

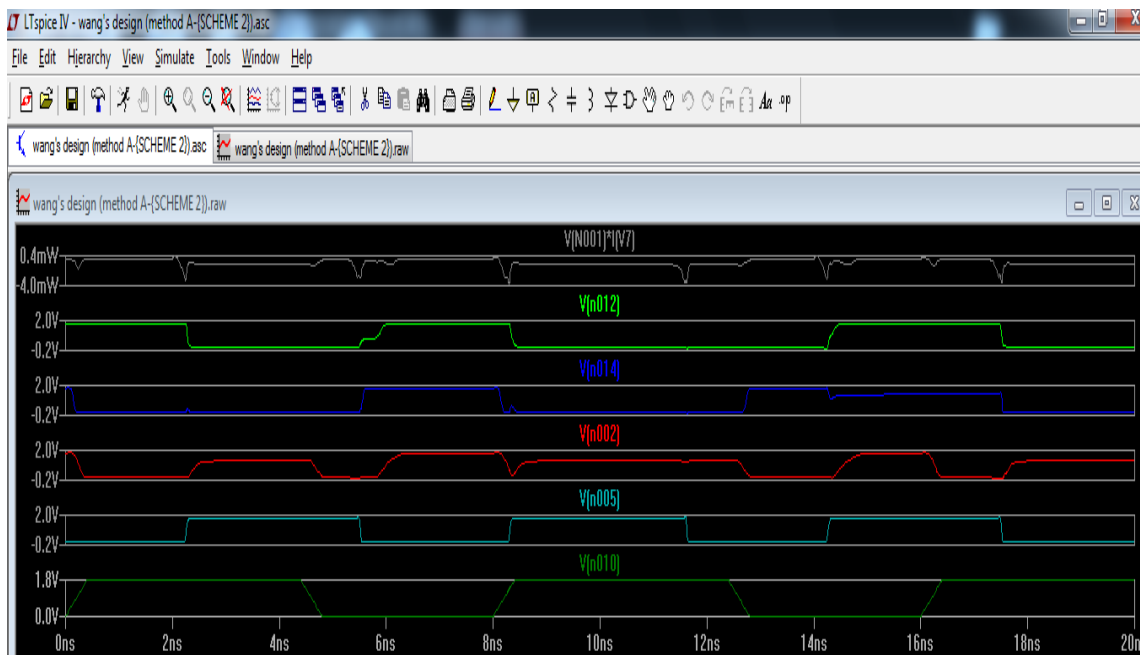
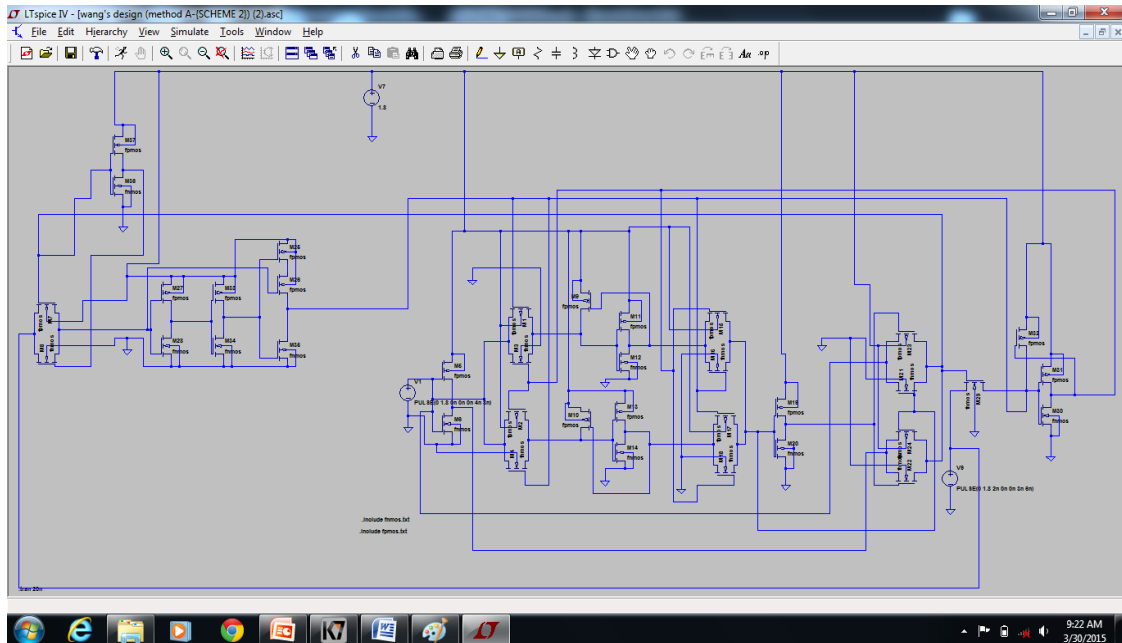


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Asynchronous Data Sampling (DHSCGFF):



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V. CONCLUSION

The asynchronous data sampling is a general and universal potential error condition associated with the clock-gated DETFF, although some asynchronous transitions may be masked because of circuit capacitances from layout and technology. In this paper, several solutions have been provided to avoid the asynchronous sampling problem in clock-gated DETFF.

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