

# Efficient Error Detection and Correction Using Decimal Matrix Code for Memory Reliability

V.Vinothini<sup>1</sup>, P.Priyanka<sup>2</sup>, J.Alphas jebasingh<sup>3</sup>, T.Kowsalya<sup>4</sup>

P.G. Student, Department of ECE, Muthayammal Engineering College, Rasipuram, Namakkal, India<sup>1</sup>

P.G. Student, Department of ECE, Muthayammal Engineering College, Rasipuram, Namakkal, India<sup>2</sup>

Assistant Professor, Department of ECE, Muthayammal Engineering College, Rasipuram, Namakkal, India<sup>3</sup>

Professor Head, Muthayammal Engineering College, Rasipuram, Namakkal, India<sup>4</sup>

**ABSTRACT:** Transient multichip upset (MCU) Problems becoming more prominent effects with large impact on memory reliability. It is necessary to protect memory cells using protection codes, for this purpose several error correction codes (ECCs) are used, but the main problem is that they require complex architecture(encoder and decode). Decimal matrix code (DMC) is used to minimize the area and delay overhead. Hamming codes have been proposed for memory protection. The main issue is that error correction capability not improved in all cases and also required large redundant .In proposed code based on divide-symbol method with encoder reuse technique (ERT) used for minimize area overhead extra circuits needed and reduce redundant bit.

**KEYWORDS:** Memory, Decimal matrix algorithm, error correction codes, multichip upset (MCU's)

## I. INTRODUCTION

### 1.1 Multichip Upset (MCU)

Nowadays, one of the main concerns in Microelectronics is the robustness of CMOS integrated circuits in relation to radiation effects. SRAM memories function can be seriously compromised by particle impacts, resulting in malfunctions of whole IC systems and in particular Systems on Chip (SOCs).

Where memories almost monopolize the overall Surface (>80%), as shown in semiconductors. At terrestrial altitudes high-energy neutrons are considered the most important radiation affecting memory ICs, hence neutron-induced MBU sensitivity has become a high priority problem among SRAM users and manufacturers. In order to properly evaluate the MBU's sensitivity, its impact on a possible ECC, and to understand the possible mechanisms involved in-depth of analysis [1]. In particular, "*multi-cell upsets (MCUs)*," which are defined as simultaneous errors more than one memory cell induced by a single event, have been under close scrutiny [11–16]. The concept of MCU, therefore, contains both upsets that can be corrected by error detection/error correction code (EDAC/ECC) as well as those which cannot. The latter is called "*multiple bit upset*" or "*multi-bit upset*" (MBU) of memory cells in the same word, and can lead, for example, to hang-ups of computer systems. Though MBUs can be avoided by a combination of ECC and the Interleaving technique [10], MCUs may still be problematic in high performance devices such as contents addressable memories (CAMs) [11] used in network processors and routers. In the case of system design, it is therefore very important to evaluate MCUs as well as soft-error rates (SERs) of the device in design phase.

## II.ERROR CORRECTION CODE

### 2.1 Hamming code

Hamming codes are commonly used to protect memories or registers from soft errors. Hamming and odd weight codes are largely used to protect memories against SEU because of their efficient ability to correct single upset with a reduced area and performance overhead[3]. Hamming code implementation is composed by a combinational block responsible to code the data, inclusion of extra bits in words that indicates parity and another combinational block responsible for

# International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 4, Special Issue 6, May 2015

decoding the data. Encoder block calculates the parity bit, and it can be implemented by set of two-input XOR gate [4]. Decoder block is more complex than encoder block, it needs not only the detect the fault but it must also correct it, which is composed of set of two-inputs XOR gates, some AND and INVERTER gate. However, it does not cope with multiple upset. Consequently more complex correcting code must be investigated.

## 2.2 Reed-Solomon codes

Reed-Solomon codes are preferred in communication and storage systems because of correction of burst and random errors. Error-correction coding attaches' redundancy, for example, parity-check symbols, to the data at the system's error correction encoder and uses that redundancy [3, 4] to correct erroneous data at the error correction decoder. All of them are based on the use of redundant element to replace defective ones, those technique vary from those applied during the manufacturing process, in the test phase to the use of built in circuit is able to repair the memory chips even during normal operation in the field with different Trade off in terms of cost and speed.

when the chip repair is performed those technique relay in a few basic redundancy schemes for instances, in redundant rows or redundant columns approach only redundant rows are included in the memory array and are used to replace defective rows detected during test also known as 1 D redundancy, the main advantage of this approach is that its implementation is very straight forward,[6] requiring no complex redundant rows and allocation algorithm. However, its repair efficiency can low, since its defective column contain multiple defective cells cannot be replaced by a single redundant rows.

## 2.3 LDPC codes

LDPC codes are block code with parity check matrices that contains only a very small number of non-zero entries. It is sparseness of H which guarantees both a decoding complexity which increases only linearly with the code length and minimum distance which is also increases linearly with the code length. Aside from the requirement that H sparse, an LDPC code itself is no different to any other block code [10]. Indeed existing block codes can be successfully used with the LDPC iterative decoding algorithm if they can be represented by a sparse parity-check matrix.

Generally however, finding a sparse parity check matrix for an existing code is not practical. Instead LDPC codes are designed by constructing a sparse parity-check matrix first and the determining a generator matrix for the code afterwards. The biggest difference between LDPC code and classical block code is how they are decoded [8]. The desirable properties of LDPC code depends on how they are to be applied. For a capacity approaching performance of low noise channel long code length and random or pseudo-random constructed irregular parity check matrices produces the performance closes to capacity [7].

## III.IMPLEMENTATION OF DMC

### 3.1 High performance of DMC

The contribution of this paper is a novel decimal matrix code (DMC) based on divide-symbol is implemented to provide enhanced memory reliability. The implemented DMC utilized decimal algorithm (decimal integer addition and decimal integer subtraction) to identify errors. By using decimal algorithm is that the error detection capability was maximized so that the reliability of memory was enhanced. Besides, the encoder-reuse technique (ERT) was implemented to minimize the area overhead of extra circuits (encoder and decoder) without disturbing the whole encoding and decoding processes, because ERT use DMC encoder itself to be part of the decoder.

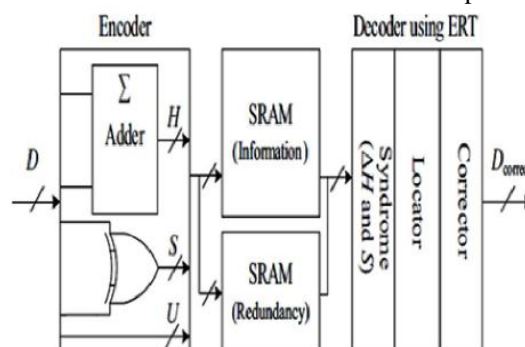


Fig.1schematic of Fault-Tolerant Memory Protected With DMC

## International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

### A. Schematic of Fault-Tolerant Memory

The schematic of fault-tolerant memory is depicted in Fig1. First, during the encoding (write) process, information bits  $D$  are given to the DMC encoder, and the horizontal redundant bits  $H$  and vertical redundant bits  $V$  are obtained from the DMC encoder. After this encoding process DMC codeword is stored in the memory. If MCUs happen in the memory, these errors can be corrected in the decoding (read) method. Due to the advantage of decimal algorithm, DMC has high fault-tolerant capability. In the fault-tolerant memory, the Encoder Reuse technique was used to decrease the area overhead of extra circuits and will be introduced in the following sections.

### B.DMC Encoder

In this DMC, first, the divide-symbol and place-matrix ideas were performed, i.e., the  $N$ -bit word was divided into  $k$  symbols of  $m$  bits ( $N = k \times m$ ), and these symbols were arranged in a  $k_1 \times k_2$  2-D matrix ( $k = k_1 \times k_2$ , here the values of  $k_1$  and  $k_2$  represents the number of rows and columns in the logical matrix respectively). Second, the horizontal redundant bits  $H$  were produced by performing decimal integer addition of selected symbols per row. Here, each symbol is regard as a decimal integer. Third, the vertical redundant bits  $V$  were obtained by binary operation among the bits per column.

### C.DMC Decoder

It should be noted both divide-symbol and arrange-matrix are implemented in logical instead of in physical. Therefore, the DMC does not require changing the physical structure of the memory. The maximum Correction capability (i.e., the maximum size of MCUs can be corrected) and the number of redundant bits are different this case, when  $k = 2 \times 2$  and  $m = 8$ , only 1-bit error can be corrected and the number of redundant bits is 80. When  $k = 4 \times 4$  and  $m = 2$ , 3-bit errors can be corrected and the number of redundant bits is reduced to 32. However, when  $k = 2 \times 4$  and  $m = 4$ , the maximum correction capability is up to 5 bits and the number of redundant bits is 72. In this paper, in order to enhance the reliability of memory, the error correction capability is first measured, so  $k = 2 \times 8$  and  $m = 4$  are utilized to construct DMC.

### D.DMC decoder structure using ERT

Decoder is prepared up of the following sub modules, and each executes a particular task in the decoding process: syndrome calculator, error locator, and error corrector. It can be observed from the fig.2 that the redundant bits must be recomputed from the received information bits  $D'$  and compare to the original set of redundant bits in order to obtain the syndrome bits  $\Delta H$  and  $S$ . Then error locator uses  $\Delta H$  and  $S$  to detect and locate which bits some errors occur in. Finally, in the error corrector, these errors can be corrected by inverting the values of error bits. In the proposed scheme, the circuit area of DMC is minimized by reusing its encoder. This is called the ERT.

The ERT can reduce the area overhead of DMC without disturbing the whole encoding and decoding processes. From Fig. 2, it can be observed that the DMC encoder is also reused for obtaining the syndrome bits in DMC decoder. Therefore, the whole circuit area of DMC can be minimized as a result of using the existent circuits of encoder. Besides, this figure also shows the proposed decoder with an enable signal  $En$  for deciding whether the encoder needs to be a part of the decoder.

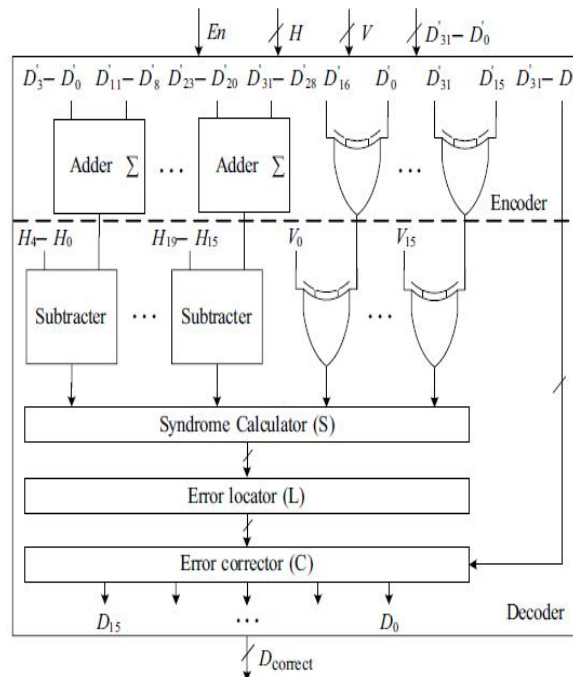
In other words, the  $En$  signal is used for distinguishing the Encoder from the decoder and it is under the control of the write and read signals in memory. Therefore, in the encoding (write) process, the DMC encoder is only an encoder to execute the encoding operations. However, in the decoding (read) process, this encoder is employed for computing the syndrome bits in the decoder. These clearly show how the area overhead of extra circuits can be substantially .

When the encoding Process has been completed the obtained DMC codeword is stored in the memory. If MCUs occur in the memory, these errors can be corrected in the decoding (read) process bits  $H4H3H2H1H$  are generated by the received. Divide-symbol and arrange-matrix ideas are performed.

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(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015



**Fig 2. DMC Decoder structure using multibit adders and XOR gates with ERT**

Extra circuit	<i>En</i> signal		Function
	Read signal	Write signal	
Encoder	0	1	Encoding
	1	0	Compute syndrome bits

### Syndrome bits

#### A. Error detection in content addressable memory

ECC code is a very powerful technique to correct MCUs in memory, as mentioned before. However, ECC implementation in CAM is significantly different from its implementation in SRAM due to simultaneous access to all the words in CAM, so that ECC code is not suitable to directly protect CAM [12]. In [14], BICS together with Hamming code is used to protect SRAM. Because BICS has zero fault-detection latency for multiple error detection, it is suitable for detection error.

For each column of CAM, BICS is added to detect the error (the basic principle and circuit of BICS are shown in [13] and [14]). When MCUs occur in a word of CAM, for each error column, a momentary current pulse is generated between power supply and ground. BICS can detect this current pulse and generate an error signal *Es*, i.e., this *Es* signal detects and locates columns which the errors occur in. At the same time, the syndrome calculation is active to detect the error row, is performed row and column.



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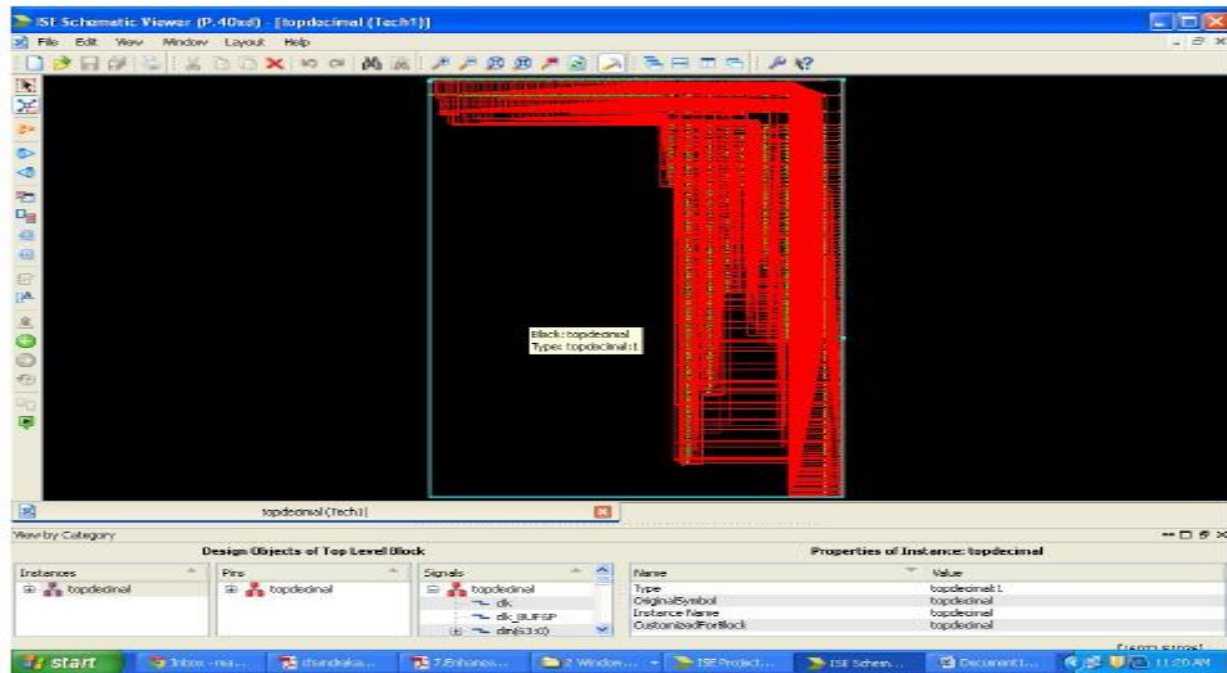


Fig 3. Technology schematic

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