

# **Design of four-core Processor with MicroBlaze using Xilinx Tool**

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**ABSTRACT:** In VLSI System design within the configuration, among the three important parameters of speed, area and power, the speed is purely determined by the delay of the design. In the delay of the design, the design delay is contributed by path delay. Now-a-days in the System design, the path delay dominates more than design delay when the architecture is larger. Because of scaling in system design, it is essential to concentrate more towards the path delay of the system to get the optimized delay so as to improve the speed of it. In this work, the design of four core multiprocessor architecture with different peripherals related to input output devices which are constructed and implemented using Spartan-3E and Virtex FPGA and the result for each block is realized using Xilinx Platform Studio..

**KEYWORDS:** Multicore processor, System design, Soft-core processor – Micro Blaze – Reconfigurable Architecture.

## **I. INTRODUCTION**

To meet the growing computation-intensive applications and the needs of low-power, high-performance systems, the number of computing resources in single-chip has enormously increased, because current VLSI technology can support such an extensive integration of transistors. By adding many computing resources such as CPU, DSP, IP in the library and custom IP etc. to build a system as System-on-Chip and Network on Chip, the interconnect between the blocks had becomes an another challenging issue. In most System-on-Chip applications, a shared bus interconnect which need arbitration logic to serialize several bus access requests and has become an adopted one to communicate with each integrated processing unit because of its low-cost and simple control characteristics.[1,5,6,7]

However, such shared bus interconnection has few things as a limitation in its scalability because only one master at a time can utilize the bus which means all buses accessing should be serialized by the arbitrator. Therefore, in such an environment where the number of bus requesters is large and their required bandwidth for interconnect is more than the current bus length, some other interconnect method has to be considered. Such scalable bandwidth requirement can be satisfied by using on-chip packet-switched micro-network of interconnects, generally known as Network-on-Chip (NoC) architecture.

The basic idea came from traditional large-scale multi-processor and distributed computing networks. The scalable and modular nature of NoCs and their support for efficient on-chip communication lead to NoC-based system implementations. Even though the current network technologies are well developed and their supporting features are excellent, their complicated configurations and implementation complexity make it hard to be adopted as an on-chip interconnection methodology. In order to meet typical SoCs or multi-core processing environment, basic module of network interconnection like switching logic, routing algorithm and its packet definition should be light-weighted to result in easily implementable solutions. [1,5,6,7]

This paper is organized as follows. Section-I gives the Introduction. Section-II deals about Xilinx Platform Studio. The features of Micro Blaze soft core processor is described in Section-III. Section-IV describes about the related work. The proposed work is briefed in Section-V. Section-VI deals with discussion and experimental results obtained, while Section VII describes about the conclusion and future work.

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## II. XILINX PLATFORM STUDIO TOOL

The ISE Design Suite Embedded System Edition includes all the tools and capabilities of the Logic Edition with the added capabilities of the Embedded Development Kit (EDK). This pre-configured kit is an integrated software solution for designing embedded processing systems, which includes the Platform Studio tool suite as well as all the documentation and IP required for designing Xilinx Platform FPGAs with embedded PowerPC® hard processor and MicroBlaze™ soft processor. This system edition provides an integrated development environment of embedded processing tool processor cores, IP software libraries, and design generators, including the following: Xilinx Platform Studio (XPS) - provides an integrated environment for creating software and hardware specification flows for embedded processor systems based on Micro Blaze and PowerPC processors. It also provides an editor and a project management interface to create and edit source code. XPS allows you to customize tool flow configuration options and provides a graphical system editor for the connection of processors, peripherals, and buses.[1,5,6,7]

Hardware Platform Generation Tool (PlatGen) - customizes and generates the embedded processor system through the use of hardware net list Hardware Description Language (HDL) files. By default, PlatGen synthesizes each processor IP core instance found in your embedded hardware design using Xilinx Synthesis Technology (XST). PlatGen also generates the system-level HDL file that interconnects all the IP cores, which can then be synthesized as part of the overall design flow.

Base System Builder Wizard (BSB) – enables the user to quickly create a working embedded system design, using any features of a supported development board or using basic functionality common to most embedded systems. After creating a basic system, then the user can customize it using the XPS and ISE software tools.

Simulation Model Generation Tool (SimGen) - generates simulation models of embedded hardware system, based on original, behavioural embedded hardware design and timing-accurate device implementation. SimGen can also incorporate the embedded software to run on the model. [1,5,6,7]

Create and Import Peripheral Wizard - helps to create the own peripherals and import them into EDK-compliant repositories or XPS projects. The wizard can create an HDL template for the custom logic and provides an interface to one of the supported IBM Core Connect or Xilinx FSL buses.

Software Development Kit (SDK) - provides a C/C++ development environment for software application projects. SDK is based on the Eclipse open source standard. SDK provides tool software project management and access to the GNU tool chain for code compilation and debug. [1,5,6,7]

GNU Software Development Tools –assist with compiling and debugging. Embedded software applications written in C, C++, in assembly which are compiled using the GNU compiler tool chain. The GNU tool chain is part of the SDK and customizes to target PowerPC and Micro Blaze processor. For detailed information about the GNU tools, including compilers and debuggers, see the “GNU Compiler Tools” and “GNU Debugger (GDB)” in the Embedded System Tools Reference Manual.

Xilinx Microprocessor Debugger (XMD) and GNU Software Debugging Tools – enables the user to debug the embedded application; either on the host development system, using an instruction set simulator, or on a board that has Xilinx device loaded with hardware bit stream.[12]

Library Generation tool (LibGen) – configures libraries, device drivers, file systems and interrupt handlers for the embedded processor system to create a software platform. Bit stream Initialize (BitInit)- updates a device configuration bit stream to initialize the on-chip instruction memory with the software executable. [1,5,6,7]

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## III. MICROBLAZE SOFTCORE PROCESSOR

AXI is an Interface standard recently adopted by Xilinx as the standard Interface used for all current and future versions of Xilinx IP and tool flows. From [5] details of AXI can be found, PLB is the legacy bus standard used by Xilinx that supports the current families including spartan6 and virtex FPGA. PLB will not support newer FPGA families, so it is not recommended for new designs that may migrate to future FPGA families [11][7]. Details on PLB can be found in the PLBv46 interface simplifications document on Xilinx.com. The tool leads through the steps necessary for creating an embedded system. Spartan 3E starter kit board utilizes Xilinx spartan3E Xilinx XC3s500E-4FG320 device. The board includes RS232 serial ports, 4 DIP switches, 4 push buttons, 8 LEDs, VGA ports, character LCD display PS/2 push button rotary encoder, SPI analog to digital converter, SPI digital to analog converter, 10/100 Ethernet port 2MB SPI flash. 16MB of parallel NOR flash and 64MB of DDR SDRAM. Push button south (RESET) is used as system reset. [1,5,6,7]

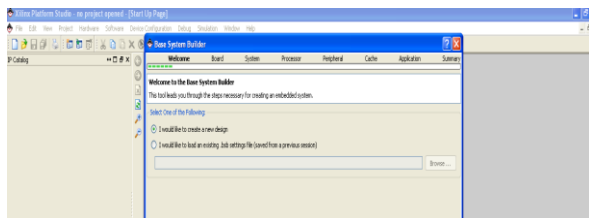


Fig.1. Embedded system design step for design specification.

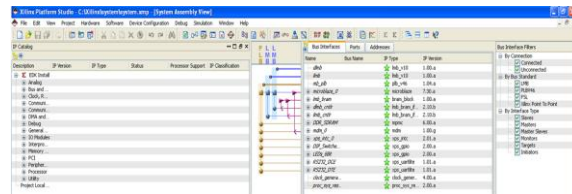


Fig.2. available IP in XILINX Platform Studio.

### Single processor:

To create a design with single processor, the wizard will let the user to configure the peripheral set and some major configuration parameters for the peripherals.

### Multi processor:

To create a design with two processor, the wizard will let the user to configure the peripheral set the processor and peripherals shared by the processors, peripheral unique to each processor and peripherals shared by the processors.

Micro Blaze specifications: the reference clock frequency: 125MHz, Type of processor: Micro Blaze, System clock frequency: 62.50

Local memory: 8B, On-chip Hardware module, Enable Floating point unit, add the peripheral from the available peripheral of the processor.

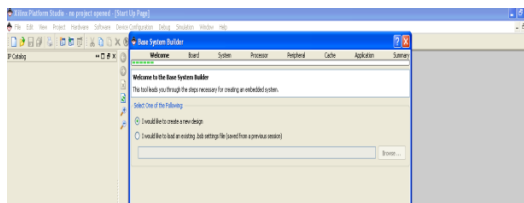


Fig.3. Embedded system design for soft-core processor choice.

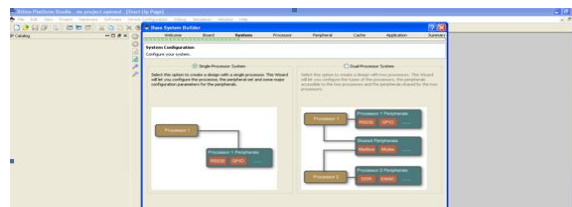


Fig.4. Embedded system design for single, multi-core choice.

The I/O devices are: Soft TEMAC, FLASH, Internal peripherals: LMB\_BRAM if controller, XPS BRAM if cntlr, XPS time base watch dog timer, XPS timer, DDR2 SDRAM, Core: mpmc, DIP switches 8 bit, Core: xps\_gpio EthernetMac, Core: xps\_ethernetlite, LEDs 8 bit, Core: xps\_gpio, Push buttons, Core: xps\_gpio, RS232\_UART1, Core: xps\_uartlite, baud rate 9600, data bits 8, SPI Flash Core: xps\_spi, DLMB\_cntlr, Core: lmb\_bram\_if\_cntlr ILMB\_cntlr, Core: lmb\_bram\_if\_cntlr, Select cache size and cash memory for single processor, [1,5,6,7]

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In MicroBlaze caches are optional and configurable. Caches are implemented using FPGA LUTs for small caches and Block RAMs are used for large sized caches. Instruction cache and data cache. Instruction cache size 64B and data cache size 64B, Below is the summary of the system which was created: Core Name, Instance Name, Base Address, High Address, The generated files were, system.xmp, system.mhs, system.ucf, runtime.opt, download.cmd, bitgen.utp, The system was generated now.

Hereafter user include any IP required to build our system as a block can be taken from the List of IPs. The available IPs are: Analog, Bus and Bus bridges, Clock, Communication, DMA, Debug, General, IO, Interpolation, , Memory, Peripheral Processor, Utility, Search on bus and bus bridges: FSL – Fast Simplex Link, PLB – Processor Local Bus, LMB – Local Memory Bus. [1,5,6,7]

### Fast Simplex Link

Types of bus interfaces that your peripheral supports or indicates that no bus interface peripheral will be supported, can be viewed in “Create and import peripheral wizard” MLB – Master processor Local bus – Select this bus interface if the master processor on the plbv4.6 interconnects. Indicate whether this master interface might generate burst transactions. SLB – Slave Processor Local bus - Select this bus interface if the peripheral operates as a slave on or on the PLBv4.6 interconnect. SDCR – Slave Direct Connect Register bus - Select this bus interface if the peripheral operates as a slave on the Direct Connect Register bus. MFSL –Master Fast Simplex Link bus - Select this bus interface if the peripheral operates as a master on Fast Simplex Link (FSL) bus. SFSL –Slave Fast Simplex Link bus - Select this bus interface if the peripheral operates as a slave on Fast Simplex Link (FSL) bus. AXI4Lite Master - Select this bus interface if the peripheral operates as a Master on AXI4lite interconnect. AXI4Lite Slave - Select this bus interface if the peripheral operates as a slave on AXI4lite interconnect. AXI4 Master - Select this bus interface if peripheral operates as a Master on AXI interconnect. AXI4 Slave - Select this bus interface if the peripheral operates as a slave on AXI4 interconnect. PLB represents Processor Local Bus, OPB represents On-Chip Peripheral Bus, LMB represents Local Memory Bus, AXI represents Advanced eXtensible Interface. [1,5,6,7]

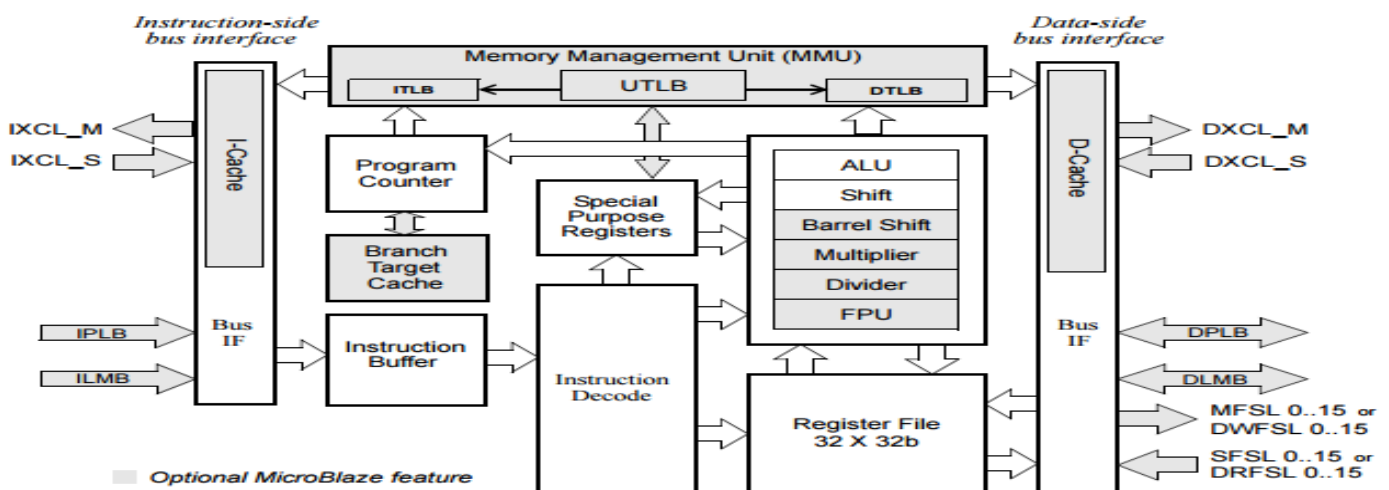


Fig.5. MicroBlaze core Block diagram

### IV. RELATED WORK

In paper [1] author illustrated the survey of NoC, in paper [2] authors FPGA based embedded system design was described in detail. In [3] multiprocessor Operating system related with thermal SoC design was briefed, but the author

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did not deals about the topology based interconnect. In the journal [4] energy efficient topology switches based on physical circuit switching in the design of SoC was briefed. This paper presents and implemented an efficient architecture which interconnects multicore processors using MicroBlaze which results in reduced delay, development time and efficient area utilization. It can quickly adapt to different interconnect pattern while changing the architecture. In this paper, topology based interconnects for multicore processor is designed using Xilinx Platform studio.

### PROPOSED ARCHITECTURE

The proposed architecture four core MicroBlaze soft-core processors are interconnected using PLB /AXI bus. Among the four processors one is designed as a master , the rest were designed as slave processors. Fig. 6.a. depicts how slave1 is in active state other slaves are isolated from the architecture due to the high impedance state of the bus. Fig. 6.b. depicts the screenshot of how slave 2 is connected with the master. Xilinx system edition (EDK & SDK version 14.3) was used to implement the interconnected architecture. The design was implemented on device Spartan-3E and Virtex.

Steps to design Embedded Single processor system is:

1. BSB Hardware with system Build
2. User IP created.
3. user ip bus,port, memory enabled as required
4. user Hardware description language is altered for our requirement design of custom IP
5. user IP incorporated with BSP.
6. hardware netlist generate, software library, debugging was done.
7. source c file modified to get inputs through gpio and display out thro COM port(RS232).

### V. DISCUSSION AND EXPERIMENTAL RESULTS

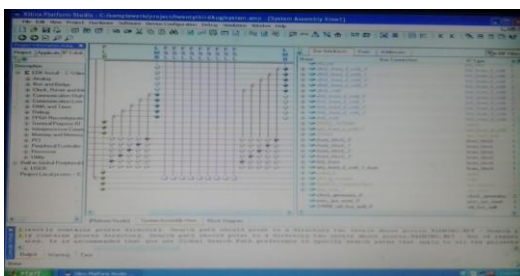


Fig.6a. four cores are connected by PLB.

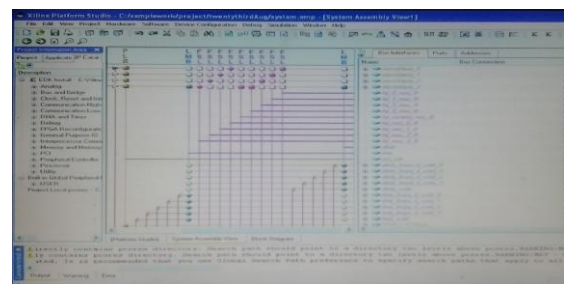


Fig.6b. four cores are connected by PLB.

This presented work the design of interconnected scheme for four core processor using a Master slave architecture. The design was implemented on Spartan 3E/Virtex FPGA. Design using MicroBlaze softcore processor provides optimized combinational path delay compared to the conventional architectures. The proposed topology based architecture finds the application in System on Chip and Network on chip design.

### VI. CONCLUSION AND FUTURE WORK

Although the focus of this work is towards the design of multi-core processor, in future this may be designed with minimized path delay in the architecture, the same can be achieved by implementing this design on the FPGA which may be interfaced by routing algorithm. Obviously if the delay in the architecture is minimized, power dissipation can also be reduced with the proposed architecture.

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- The design of Four – core Processor was done by having one as the master and others as slave with PLB/AXI bus interconnect using topology based connect between them.

### Future work:-

- The delay can also be further minimized by employing various topology as the iterative process.
- Topology interconnect can be introduced by writing OOP in C++ using SDK tool to make interaction with the system design.

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### BIOGRAPHY

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