

Modified Design of Double Edge Triggered Flip-Flop Based On a Signal Feed through Scheme

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ABSTRACT: A low power flip-flop design featuring an explicit pulse triggered flip-flop structure and a clock pulse generated based on a signal feed through scheme successfully solves the long discharging path problem in dual edge-triggered flip-flop design and reduced performance in a critical-path. In the proposed design an explicit pulse dual-edge triggered flip-flop is presented, which provides comparatively less power consumption than pulse triggered flip-flop besides providing same performance as the single edge-triggered flip-flop, also it achieves low power consumption in clock distribution network.

KEYWORDS: double edge triggered, single edge triggered, clock generated.

I INTRODUCTION

Flip-flops and latches are one of the most important circuit elements in synchronous VLSI chip. The power consumption of the clocking sub-system which is composed of the clock distribution network and the clock storage elements is about 30% to 60% of the total system energy. The clock distribution networks is composed of buffers and wires. And the clock storage elements are flip-flops and latches. To minimize the circuit complexity, the pulse-triggered FFs have been considered as the most popular alternative to the conventional master-slave based FFs. The pulse-triggered FF consists of a pulse generator (also known as transition detector) for strobe signals and a latch for data storage. Since the pulses are generated on the transition edges of the clock signal and very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a pulse-triggered FF is thus greatly simplified since only one latch is used, as opposed to two latches in master-slave configuration. It can thus provide higher toggle rate than the conventional FF can and is found useful in high speed applications

Double-edge triggered pulse generator is utilized to further reduce power on the clock tree and the clocked transistors in pulse generator. Double-edge triggered flip-flops can have the same data throughput as the single-edge triggered flip-flops. The power saved in the clock distribution network is not included when we compare the power consumption. Also, clock gating can be easily applied to eliminate power consumption for the same value. Although the input load is increased, significant power saving could be achieved.

DETF implementation techniques can be commonly categorized under two basic ideas. The first idea is to insert additional circuitry to generate internal pulse signals on each clock edge. The second idea is to duplicate the pathway to enable the flip-flop to sample data on every clock edge. The DETFF increases the rate of data processing or alternatively reduces the clock rate by half, thereby, either increasing the data throughput or reducing the power consumption in the clock circuit respectively. Thus reduced power consumption and high speed operation is possible.

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II. IMPLEMENTATION TECHNIQUES OF DETFF

Pulse triggered consists of pulse generator for strobe signal and latch for data storage .because of its single latch structure and its circuit simplicity, the power consumption by this pulse triggered will be lower when compared to conventional and master slave.

The implicit and explicit are the two types of pulse flip-flop the explicit type provides better improvement in speed and power because of its logic separation of pulse generation and latch circuit.

In classic explicit pulse flip-flop, which is named as DCO consists of nand-logic based pulse generator and a semi dynamic true single phase –clock (TSPC) structured latch design. The four inverter I1, I2, I3, I4 are used for this design. The inverter I3and I4 are for latch is data, inverter such as I1, I2 are responsible for holding the internal node X. While holding these internal node X, it gets discharged on every rising edge of the clock, instead of heavy static input ‘1’ .due to this discharging of the node X. The large switching power dissipation will occur. To overcome this type of dissipation, Conditional Discharging Flip-Flop (CDFF) technique is used. This conditional discharge technique consists of extra nMos transistor MNX which is to be controlled by the output signal q-fdbk. This flip flop design is shown in figure 1. By this discharging of internal node does not occur.in addition to extra nMos transistor inverter plus pull up MOs transistor is used for simplification of internal node x. Further improvement in the flip-flop design can be done and its design is shown in figure 2 by using static latch structure which is named as Static Discharge Flip-Flop (SDFF). So the internal node storage x is exempted from the periodical precharge. However Both CDFF and SDFF design has improvement in the power, delay caused by this design will be higher. To overcome this type of delay the Modified Hybrid Latch Flip-Flop (MHLFF) was designed and it is shown in figure.3 which consists of single static latch. This keeper logic at x is removed.A weak pull up transistor which is described in the previous design controlled by the output signal Q and it maintains the level of node X when Q is equal to 0.

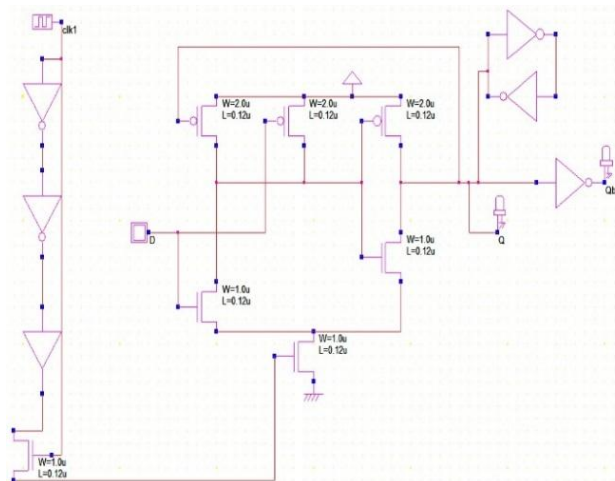


Fig. 1 Conditional discharge flip-flop

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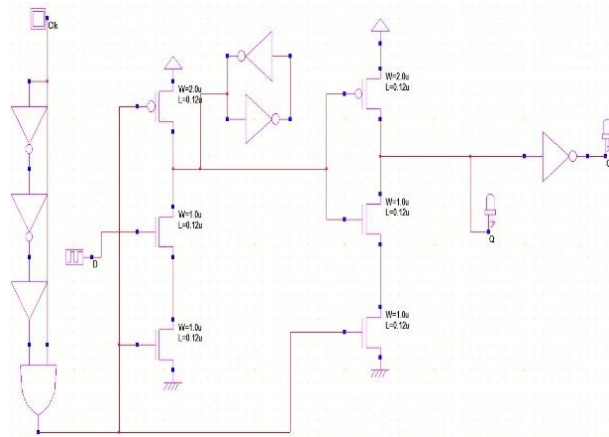


Fig. 2Explicit data close output (ep-DCO) flip-flop

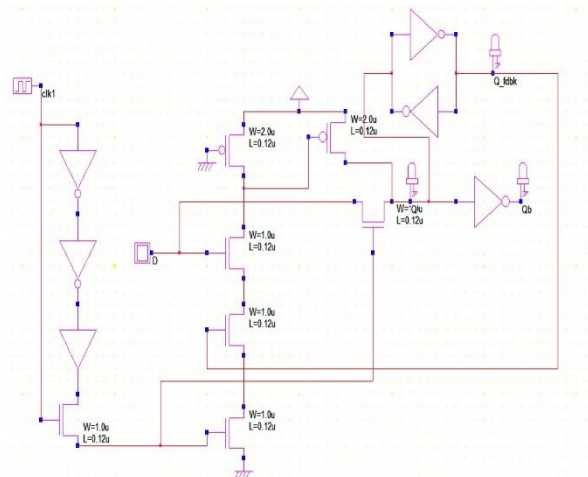


Fig. 3 Modified hybrid latch (MHLFF) flip-flop

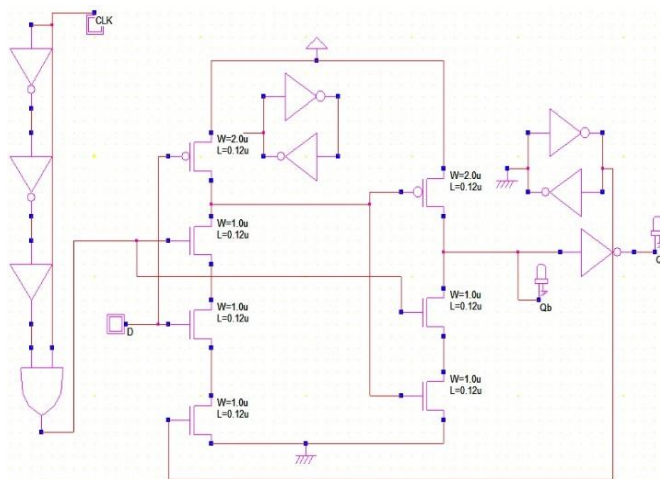


Fig. 4Static conditional discharge flip-flop

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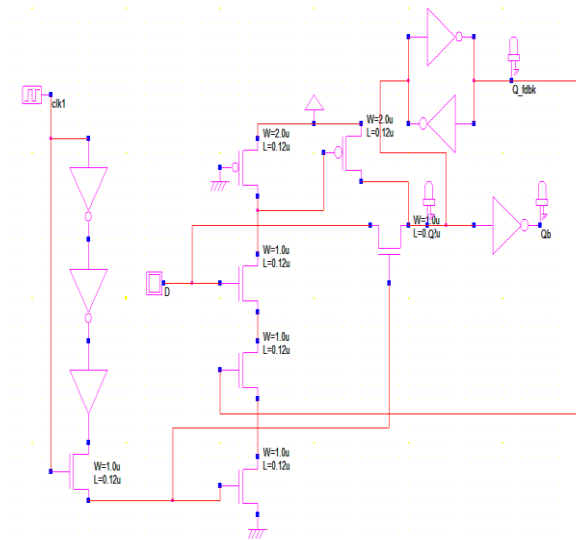


Fig. 5 Traditional TSPC flip-flop

The figure.4 shows the flip- flop design of static conditional discharge. In this design, the logic gate OR is used to consume low power. Then the figure.5 shows the traditional TSPC flip-flop which is similar to hybrid latch flip-flop design. So it needs improvement in the design.

In this paper, Dual edge triggered flip –flop is used to consume power and delay of the design.

III. METHODOLOGY

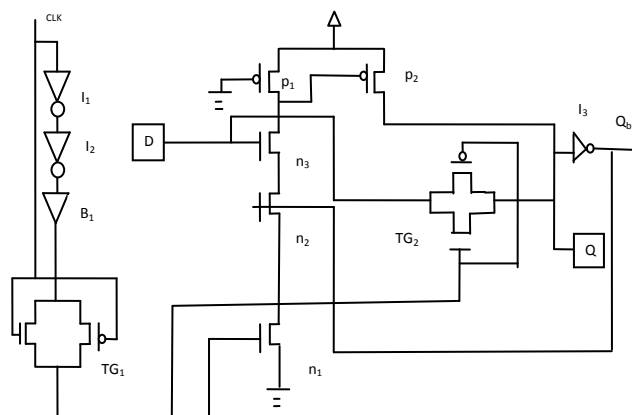


Fig. 6 Developed flip flop design

Working Principle:

In the developed design, the true single phase clock (TSPC) circuit is implemented. The input 'D' is provided to the n3 transistor (TSPC logic). The "CLK" input is provided to the n1 transistor through buffers and transmission gate TG₁. The figure.6 clearly shows the modified flip-flop design using transmission gate. The P1 transistor is grounded in the design. The gate input of transmission gate transistor TG₂ is obtained from TG₁ and the input to TG₂ is from 'D'. I₁, I₂ in the circuit operates as buffer. This buffer is provided to hold the CLK signal. Hence the transition of the TG is not rapid. The CLK is the gate input for TG₁. When the CLK is high, the Transmission gate is ON and the input to TG₁ is

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obtained as the output from TG1. When the output from the TG1 is high then transistor n1 is ON and hence it is grounded. The output Qb is feedback to the transistor n2. Thus When CLK and 'D' are HIGH, then the output Q is High and Qb is low. When both CLK and D is low, then the previous state output is retained. From the TG2 transistor, the output is obtained with minimum voltage degradation.

MICROWIND

MICROWIND is truly integrated EDA software encompassing IC designs from concept to completion, enabling chip designers to design beyond their imagination. MICROWIND integrates traditionally separated front-end and back-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities. It tightly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification – providing an innovative education initiative to help individuals to develop the skills needed for design positions in virtually every domain of IC industry.

The MICROWIND 2 program allows designing and simulating an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND2 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

IV. RESULTS DISCUSSION

Since the pmos transistor P1 is always ON the dynamic power dissipation across it will be low. The signal feedback from Qb to the n2 transistor helps in lesser computation time. This proposed design eliminates the long discharging path problem in the pulse triggered Flip-flop. The comparison of the speed and power of various methods has been done and the proposed design achieves high performance and speed with less dynamic power dissipation and delay. The figure.7 shows the micro- wind schematic diagram of the developed DETFF flip-flop design.

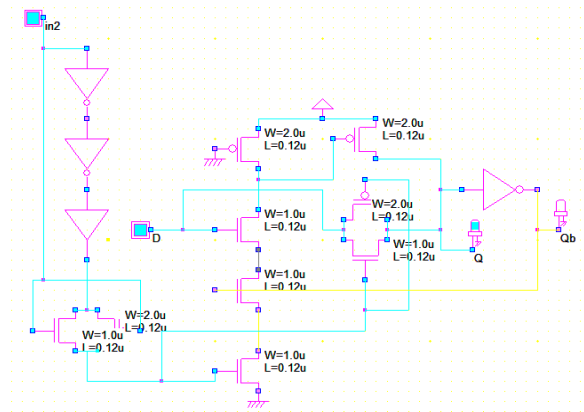


Fig. 7Developed DETFF flip-flop design

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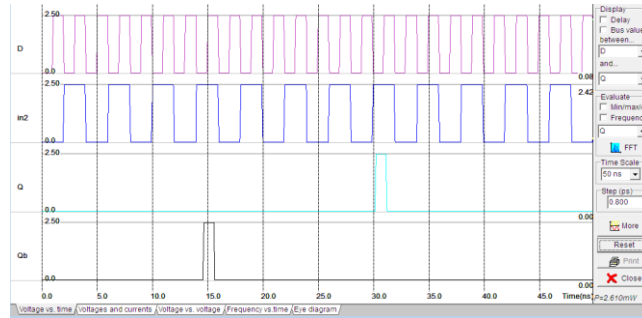


Fig. 8Simulation result of developed system

The figure.8 shows the simulation result of the developed DETFF flip-flop design. The figure. 9 shows the layout of the DETFF flip-flop design.

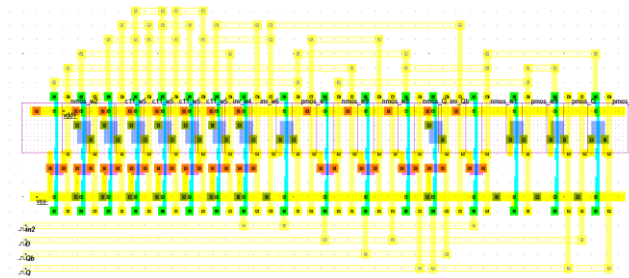


Fig. 9Layout of developed system

Table.1 Parameter Comparison

LOGIC	POWER DISSIPATION (mW)	DELAY (ps)	AREA (μM^2)
CDFP	0.614	166	1592.6
Ep-DCO	0.626	188	1232.0
MHLFF	0.954	178	1093.3
Static CDFP	0.551	170	1424.5
Traditional TSPC	0.921	172	1243.9
Developed method	0.353	155	1302.0

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Table.1 shows the parameter comparison of the flip-flop design. The parameters considered here is power, area and delay.

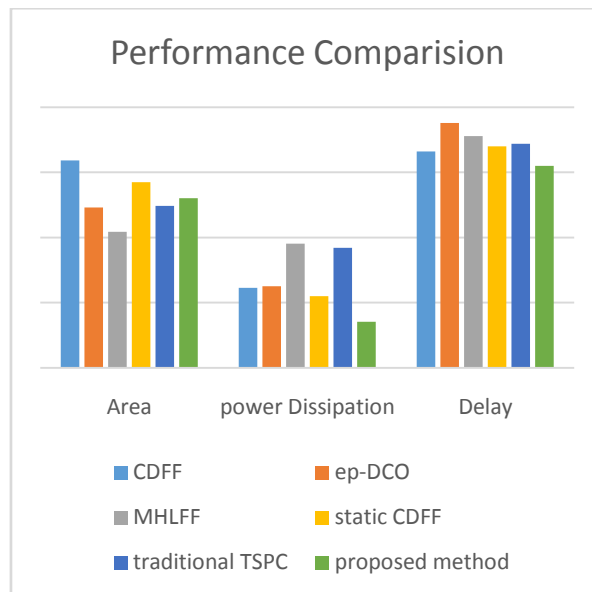


Fig. 10: Performance Comparison of the design

V. CONCLUSION

In this paper a high performance Double Edge Triggered D-Flip Flop is proposed and is designed in 90nm CMOS technology, which is static in nature. The implementation of the proposed design with the transmission gate provides the lesser power dissipation and improved performance than other implementation. The proposed DET flip-flop is having less number of clocked transistors than the other existing designs. The proposed design has lesser average power and lowest power delay product (PDP) than existing designs. Therefore the proposed design is reliable in the various implementations using DETFF.

REFERENCES

- [1]. Hung-Chi Chu, Jin-Fa Lin, and Dong-Ting Hu "Novel Low Complexity Pulse-Triggered Flip-Flop for Wireless Baseband Applications" Hindawi Publishing Corporation, ISRN Electronics, Vol 2013.
- [2]. Peiyi Zhao "High-Performance and Low-Power Conditional Discharge Flip-Flop" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 12, No. 5, May 2004 477.
- [3]. Massimo Alioto, Senior Member, IEEE, Elio Consoli, and Gaetano Palumbo, Fellow "Flip-Flop Energy/Performance versus Clock Slope and Impact on the Clock Network Design" IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 57, and NO. 6, JUNE 2010.
- [4]. M. Alioto, E. Consoli, and G. Palumbo, "General strategies to design nanometre flip-flops in the energy-delay space," IEEE Trans. Circuits Syst., vol. 57, Jul. 2010.
- [5]. M. Alioto, E. Consoli, and G. Palumbo, "Flip-flop energy/performance versus Clock Slope and impact on the clock network design," IEEE Trans. Circuits Syst., Jun. 2010.
- [6]. M. Alioto, E. Consoli, and G. Palumbo, "Analysis and comparison in the energy delay-area domain of nanometer CMOS flip-flops: Part I - methodology and design strategies," IEEE Trans. Very Large Scale Integer. (VLSI) Syst May 2011.
- [7]. B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, Aug. 2001.
- [8]. N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power-efficient dual-edge clocking," in Proc. Int. Symp. Low-Power Electron. Design, Aug. 2002,