

# **An Optimized VLSI Based MIMO Accelerator Architecture Design**

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**ABSTRACT:** In recent years, the main parameter in MIMO-OFDM communication system is energy capable optimization and quality of service. The Proposed design is used to solve the problem of multi-channel optimize to multi target in single channel optimization. It is a result for energy optimization in MIMO decoding system implemented by using various algorithms. The proposed methodology provides full compatibility for different wireless communication standards such as Wi-Fi, Wimax, 3G and also in MIMO decoding algorithm. The projected design consist of Basic blocks of Decoder accelerator such as memory Unit, Multiplier Unit, Adder/Subtractor unit, Rotation unit and controller parts. An optimized algorithm in Rotation unit is used with some functional conditions .The rotation process occurs randomly during the process. It describes the implementation used to ensure overall energy utilization of the designed accelerator without affecting programmability criteria. By using, XILINX 14.3 EDA tool the simulation results are obtained. The proposed MIMO decoding accelerator was compared against existing programmable methodologies and gives an energy efficient optimized technique.

**KEYWORDS:** Optimized MIMO (Multiple input Multiple output) decoding accelerator, CORDIC Rotation Unit, OFDM (orthogonal frequency-division multiplexing) communication system, power and delay.

## **I. INTRODUCTION**

In wireless communications systems Multiple-input–multiple-output processing and orthogonal frequency division multiplexing are two dominant technologies. MIMO is an antenna technology for wireless communications. It process multiple antennas are used at both the source and target section to reduce errors and to optimize data speed. The most existing studies mainly worked on to calculate the channel performance for MIMO communication systems. A decoder design uses a single MIMO decoding algorithm such as zero forcing (ZF), minimum mean square error (MMSE), maximum likelihood (ML), or one of the many sphere decoding (SD) variants. A system designer chooses a single MIMO decoding algorithm to be used to satisfy the condition of the standard. A hardware engineer then implements the chosen algorithm with constraints on complexity, performance, and power consumption considering the parallel processing requirements for OFDM operation. This design cycle is typically repeated for every new communication standard.

A MIMO decoder is the receiver component that separates the transmitted data streams from the signals received on the receive antennas. The proposed design consist of Basic blocks of Decoder accelerator such as Multiplier Unit, Adder/Subtractor unit, Reciprocal unit and Rotation unit. The valuable capacity of the Rotation unit with accelerator over wireless links was proposed for mobile wireless networks. The modification work essentially focused by the addition architecture. It consumes more processing time for the MIMO signal processing operation. It can be carried out by minimizing the addition processing time and to improve system performance level. So it is to be use the CSA adder design in the adder unit. The MIMO design consists the various arithmetic unit. The proposed method is carried out by improving technologies in addition unit with carry propagation level. This method is to

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analysis the quantity and consumption level. This technique is to improve the system efficiency and speed. The CSA methodology is to analysis the carry selection time and to reduce the delay level. The processing cycle and the parameterization of the MIMO accelerator Hardware Description Language (HDL) were introduced. The complete design environment is developed for user. In this paper the MIMO accelerator chip implementation and hardware take a look at results. It emphasize a number of the trade-offs and implementation choices that affected the hardware price and performance to the purpose that it currently delivers ASIC-like PDP (power delay product) performance.

Paper is organized as follows. Section II describes MIMO Hardware architecture and related work of the MIMO accelerator, Section III describes Development of Modules And its RTL View and Section IV presents experimental results showing simulation results, RTL View, Synthesis Report and Power Calculation Of proposed MIMO Accelerator. Finally, Section V presents Performance Analysis with Existing and Proposed Work. Section V presents Conclusion and References.

## II. MIMO ACCELERATOR HARDWARE ARCHITECTURE

The basic building blocks of the MIMO accelerator is shown in fig.1 MIMO decoding is based on matrix processing. It is a complex number vector based processor. The processing core module in MIMO accelerator is considered as a most important data path to perform MIMO decoding operation. It is carried out by minimum set of primitive operations.

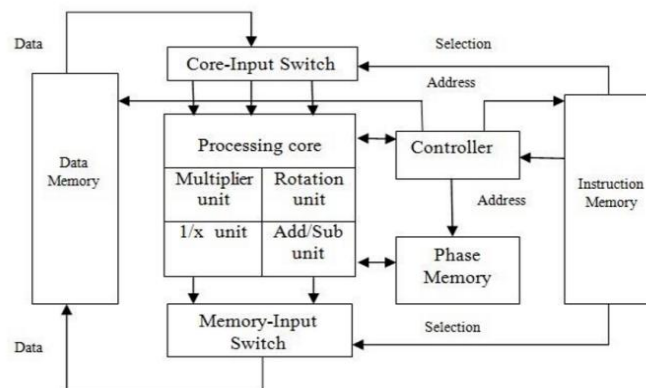


Fig. 1 Basic Block Diagram of MIMO Accelerator

The process core is split into four units. The addition unit is take into account as a primary process unit that performs adder and Subtractor operation of 2 pairs of complicated vectors at the same time. Second, multiplication unit it contains four real blocks. It computes single complex number from each block produces real of two difficult vectors. The reciprocal unit is run as a third method unit that performs function of reciprocal of numbers. It's utilized in the most for scaling the signal power. Fourth, rotation unit it consists of Coordinate rotation Blocks(CORDIC).The sub block of rotation unit are super vectoring CORDIC and super rotation CORDIC. Multiple single CORDIC units are super CORDIC it performs difficult section rotation .The section rotation is administered in signal section process unit and its output is given to rotation CORDIC.

The source of the input phases to the phase processing unit is programmable. This source can be either the super vectoring CORDIC, the super vectoring output in the previous rotation unit operation, a phase stored in a special memory(which is called the phase memory as shown in Fig. 1),or a number stored in the data memory. This flexibility gives the programmer an extra degree of freedom that will help in achieving the best utilization for the rotation unit. The phase processing unit, can also perform shift and sign inversion operations, thus extending the capabilities of the rotation unit to include real-valued Jacobi operations.

The input source for phase processing units is taken either from super vector CORDIC outputs. It is the outputs generated from previous rotation unit operation, which is programmable stored in special memory or data

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memory. The phase processing unit perform shift and sign inversion operation. So, there is availability of extra utilization in rotation unit. The part memory is termed as static RAM (SRAM) to resolve part outputs of vector CORDIC in rotation unit. It is often reused as an input to super rotation CORDIC blocks.

An instruction is used to control huge amount of words. It is used to store preceded instructions run on the MIMO accelerator. To carry out given operation processing unit is used. Instruction memory is used for data memory location of input vector operands for the processing units. It can also store the results of processing unit in location data memory. It also carried out flow controls in controller.

The core input switch is a two level multiplexing circuit. It selects and arrange the complex vectors for given processing core. The memory input performs the reverse process of data memory. It takes the output of processing units and properly to write all the data with the OFDM subcarrier in suitable data memory location. The instruction word controls the two switching circuits, helps in delivering a significant amount of flexibility.

### III. DEVELOPMENT OF MODULES AND ITS SIMULATION RESULTS

The processing of MIMO accelerator is divided into four modules. In each module data's are processed based on the instructions given. The block diagram of modules separated in MIMO accelerator is given in fig 2. And their simulation results for each module is explained and follows.

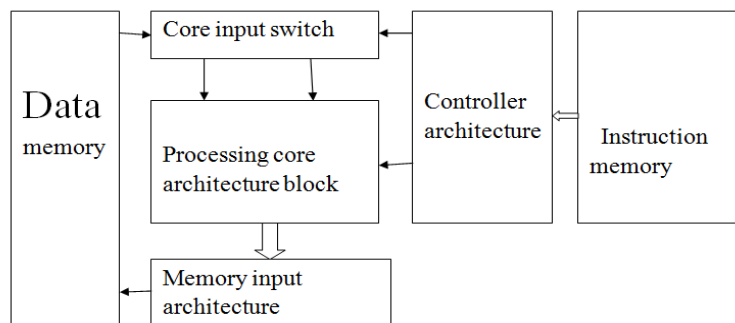


Fig. 2 Block Diagram of MIMO Accelerator Modules

#### A. MEMORY INPUT SORTING METHOD

The memory input sorting methodology is mainly used to the split the arithmetic process output bits and to apply the mux combination process and this combination process to separate the bits wise process. This methodology is to optimize the input process for required output in data memory architecture. This process to implement the MIMO decoding part. This architecture results is used to update the memory process and to access the next output data memory process and to store the output results to data memory architecture.

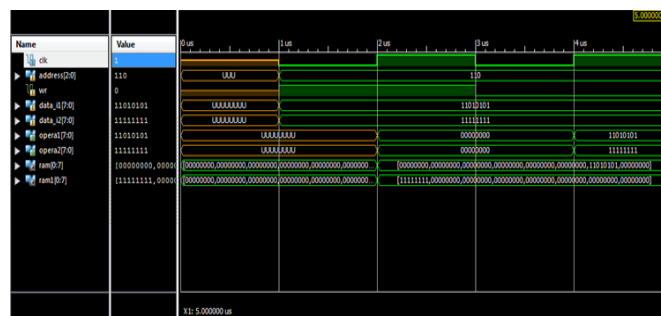


Fig. 3 Simulation Result of Memory Input Sorting Module

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## B. PROCESSING INPUT SORTING METHOD

The process input sorting methodology used to get the input operand data for the data output memory process. This process is carried out using the mux combination architecture. And to apply the mux input for the two operand data inputs. The mux combination to separate the operand data bits, this process same as to the memory input sorting mux combination process. This process is to deliver the input data bits and also using the imaginary data input bits. This process using the memory architecture and to write and read the two operand data bits.

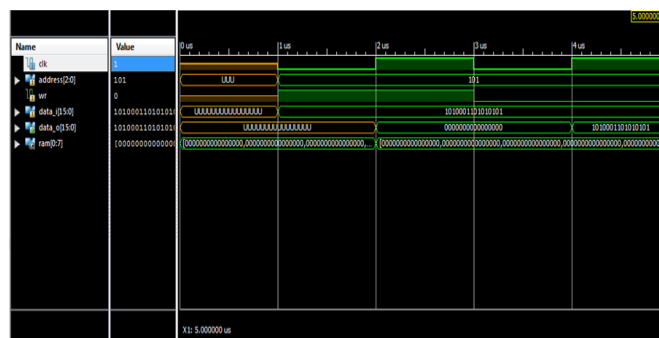


Fig. 4 Simulation Output of Processing input Sorting Module

## C. PROCESSING CORE ARCHITECTURE

The processing core architecture consists the five arithmetic process. It consists of 8-bit addition unit, subtraction unit, multiplication unit, and division unit and rotation unit. The core architecture to display the output results for the required arithmetic selection process. The mux architecture used to retrieve the input data bits from data memory architecture. Thus the input operand data bits are apply to the five arithmetic processes and to modify the addition unit architecture. This architecture used to the carry select adder process.

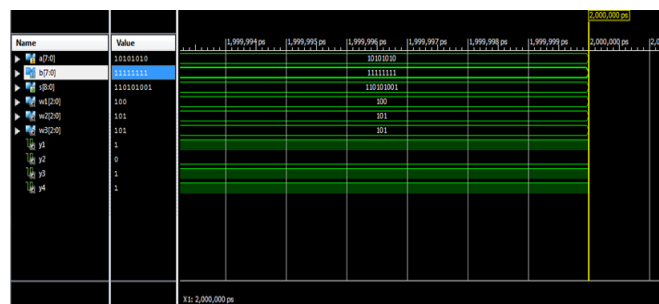


Fig .5(a) Simulation Result of Adder Unit

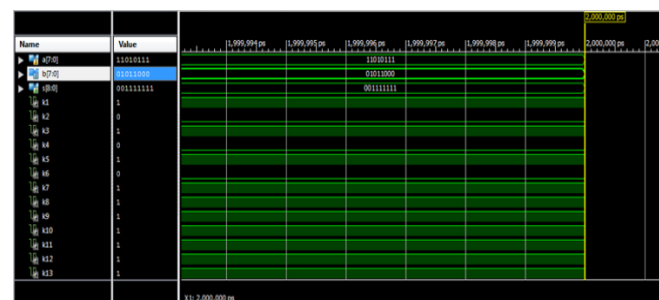


Fig .5(b) Simulation Result of Subtractor Unit

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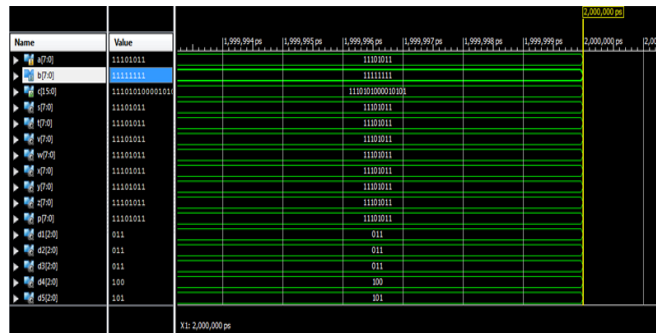


Fig .5(c) Simulation Result of Multiplier Unit

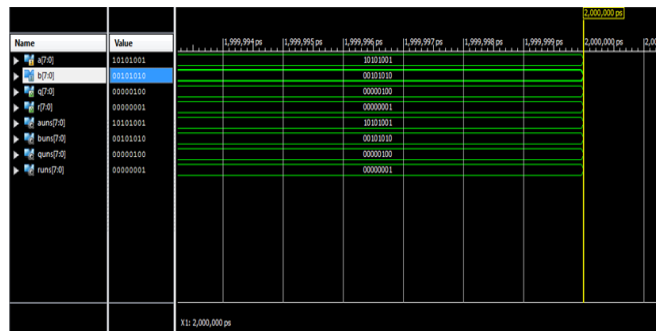
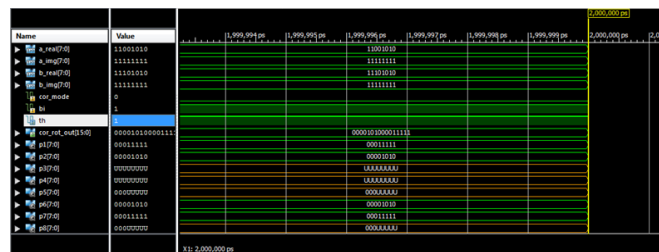


Fig .5(d) Simulation Result of Rotation Unit

## D. CORDIC ROTATION ARCHITECTURE

The CORDIC rotation architecture mainly used to the MIMO accelerator architecture unit. This unit used to optimize the MIMO process and this unit focused by the signal processing methodology. This architecture design to implement the real and imaginary data input operand data input bits. This architecture is mainly using the mode shifting methodology. The rotation unit process to develop the bit wise rotating process and to increase the system performance also. And to find the signal based rotation architecture output results.



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## IV. RTL VIEW, SYNTHESIS REPORT AND POWER CALCULATION OF MIMO ACCELERATOR

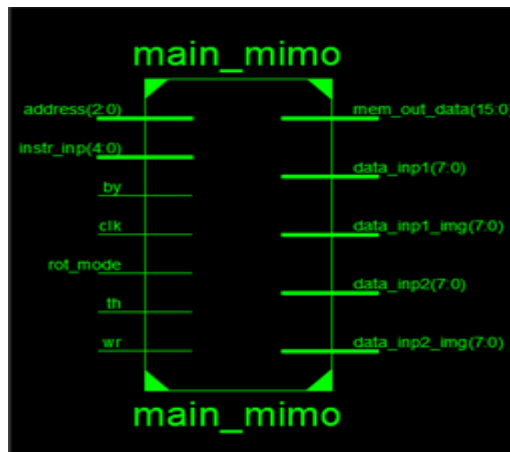


Fig. 7(a) MIMO Accelerator Module

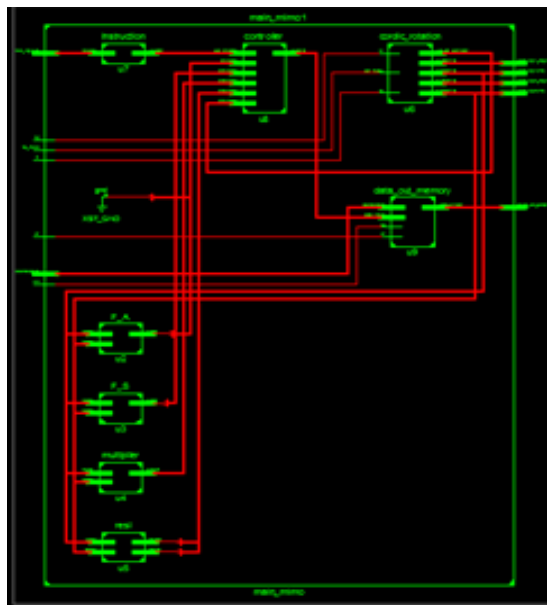


Fig. 7(b)

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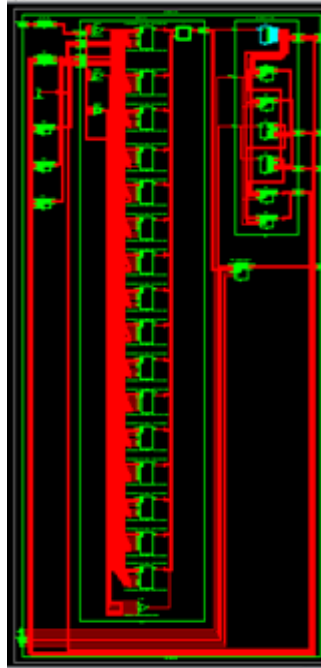


Fig .7 (c)

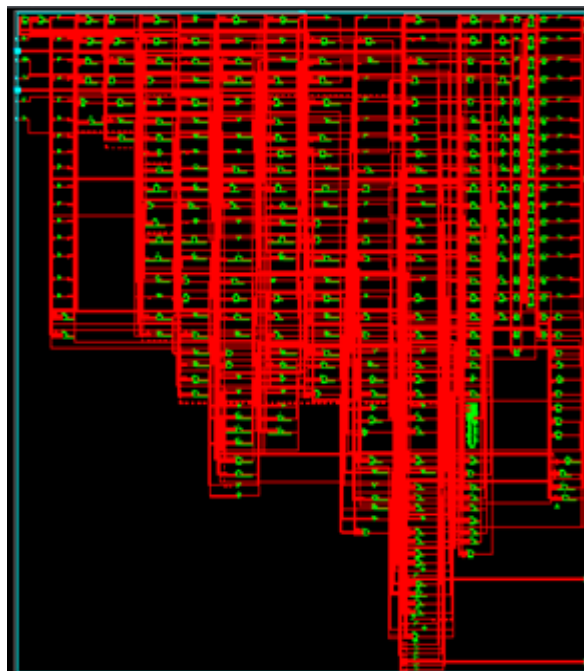


Fig .7 (d)

Fig .7(b),(c),(d) RTL view of Modules connected in MIMO Architecture Module





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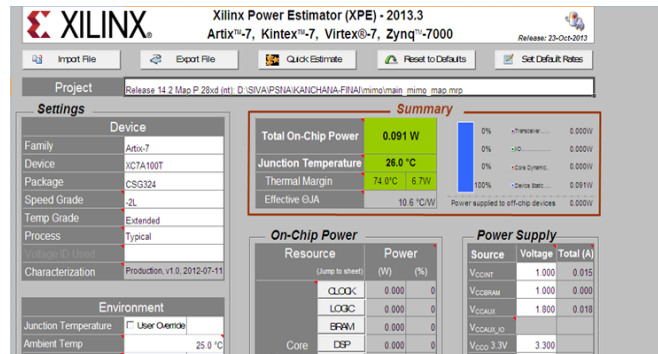


Fig. 9(a)

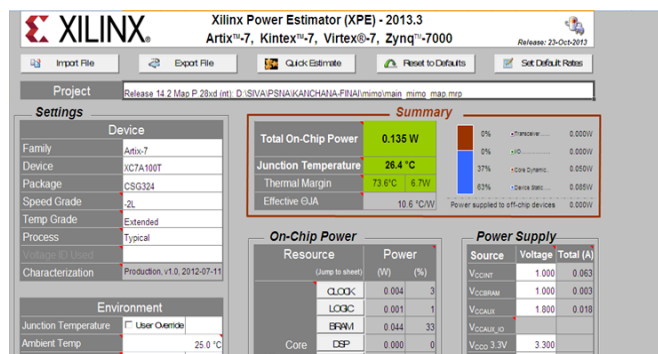


Fig. 9(b)

Fig. 9(a),(b) Simulation Output of Power Calculator in MIMO Accelerator

## POWER CALCULATION

$$\begin{aligned} \text{POWER} &= (\text{TOTAL ON CHIP POWER}) - (\text{STATIC POWER}) \\ &= (0.135) - (0.091) \\ &= (0.044) \text{ W} \end{aligned}$$

TABLE 1. COMPARISON OF EXISTING AND PROPOSED MODULE OF MIMO ACCELERATOR

	EXISTING SYSTEM	PROPOSED SYSTEM
DELAY(NS)	6	1.149
SPEED(MHz)	166	870.95
POWER(mW)	300.9	44.0

## V. CONCLUSION

In this paper, an energy-efficiency model is proposed for MIMO-OFDM mobile multimedia communication systems with statistical Scheduled random rotation unit. An energy-efficiency optimization scheme is presented based on process core which consists the process of adder/subtractor, multiplier and Rotation unit. From the existing Rotation unit we have modified that into scheduling mechanism by the functional input conditions to the rotator algorithm. Our proposed work prepares better result while comparing with the previous works held based on conventional process unit. We have simulated the design using Xilinx ism simulator and verified the designs. The trade off of power, delay and speed are calculated for proposed model. The obtained result is compared with existing paper and good trade off are obtained.

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