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Implementation of Reduce the Area- Power Efficient Fixed-Point LMS Adaptive Filter with Low Adaptation-Delay

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ABSTRACT : In the existing system the high amount of delay, area and power can be used . so we use a novel partial product generator and propose a strategy for optimized balanced pipelining across the time-consuming combinational blocks of the structure. To achieving lower adaptation-delay and area-delay-power efficient implementation. In proposed method we use large processing elements (PEs) for achieving a lower adaptation delay with the critical path of one MAC operation. They have proposed a fine-grained pipelined design to limit the critical path to the maximum of one addition time, which supports high sampling frequency, but involves a lot of area overhead for pipelining and higher power consumption due to large number of pipeline latches. A an efficient adder tree for pipelined inner-product computation to minimize the critical path and silicon area without increasing the number of adaptation delays. so we use a carry select adder in the proposed method to reduce the area and power. The carry select adder is efficient adder and easy to design compare to other design.

KEYWORDS : Adaptive Filter, Least Mean Square Algorithm, Weight Update Block, Adder

I. INTRODUCTION

The Least Mean Square (LMS) adaptive filter is the most popular and most widely used adaptive filter because of its satisfactory convergence performance. The direct-form LMS adaptive filter involves a long critical path due to an inner-product computation to obtain the filter output. The critical path is reduced by pipelined implementation .the conventional LMS algorithm does not support pipelined implementation because of its recursive behavior, It is modified then it called by delayed LMS (DLMS) algorithm which allows pipelined implementation of the filter. A lot of work has been done to implement the DLMS algorithm in systolic architectures to increase the maximum usable frequency but, they involve an adaptation delay of $\sim N$ cycles for filter length N , which is quite high for large order filters. Since the convergence performance degrades considerably for a large adaptation delay has proposed a modified systolic architecture to reduce the adaptation delay.

II.EXISTING METHOD

An efficient architecture for the implementation of a delayed least mean square adaptive filter. We use novel partial product generator to optimized balanced pipelining across the time-consuming combinational blocks of the structure. We also find that the proposed design offers less area, less energy than the best of the existing systolic structures, on average, for filter lengths $N = 8$. The final outputs of MA units calculated and the desired updated weights to be used as inputs of the error-computation block as well as the weight-update block for the next iteration. The weight-update block generates w_{n-1-n2} , and the weights are delayed by each of $n2+1$ cycles. However, it should be noted that the delay by 1 cycle is due to the latch , which is included in the delay of the error-computation block, i.e., $n1$. Therefore, the delay generated in the weight-update block becomes $n2$. If the locations of pipeline latches are decided $n1$ becomes 5,

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where three latches are in the error-computation block, one latch is after the subtraction and the other latch is before PPG Also, n_2 is set to 1 from a latch in the shift-add tree in the weight-update block.

III. PROPOSED METHOD

CARRY SELECT ADDER

A carry-select adder is a way to implement an adder, it is easy to design. In logic element that computes the n -bit sum of two n -bit numbers. The carry-select adder is simple but fast. The carry-select adder consists of two ripple carry adders and a multiplexer. Adding two n -bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, The each of the function each of carry being zero and the other assuming one.

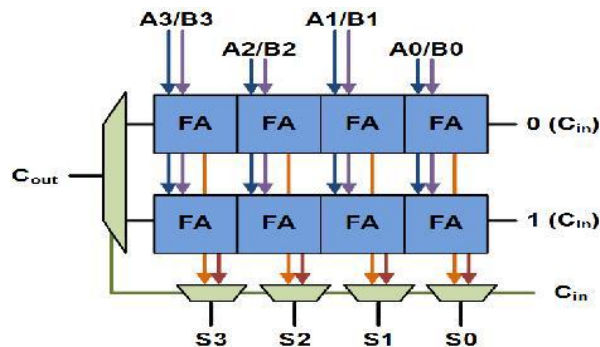


Fig 1. Basic building block of carry select adder

BLOCK DIAGRAM OF LMS ADAPTIVE FILTER

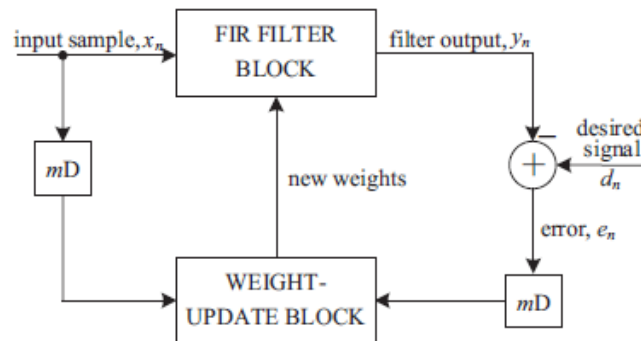


Fig 2 :Structure of conventional delayed LMS Adaptive filter

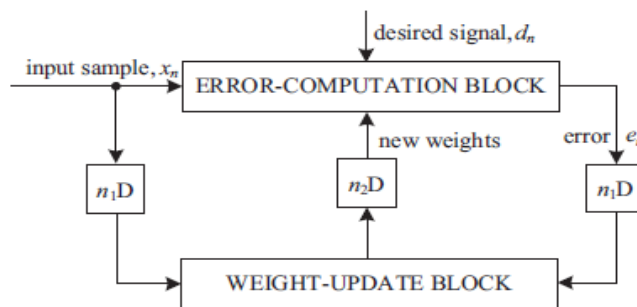


Fig 3:Structure of modified delayed LMS Adaptive filter

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ERROR COMPUTATION BLOCK

In the error computation block the each of the input are given to the D and the 2-BIT PPG and each of the condition to check the co efficient of each sample of inputs . N number of 2-b partial product generators (PPG) with respect to N num of multipliers and a cluster of L/2 binary adder trees. It should be based on adder tree and shift adder tree.

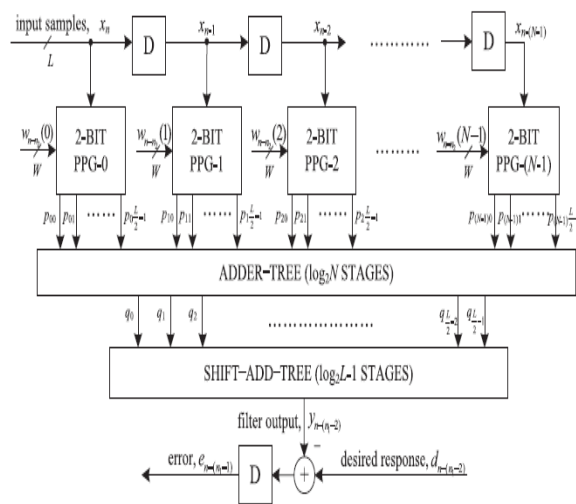


Fig 4. Structure of error-computation block

STRUCTURE OF PPG

In the PPG L/2 number of 2-to-3 decoders and also the same number of AND/OR cells (AOC).the 2 to 3 decoders to produce the three outputs are b0, b1 and b2.the co efficient value of each w ,2W,3W are fed to the AOC.

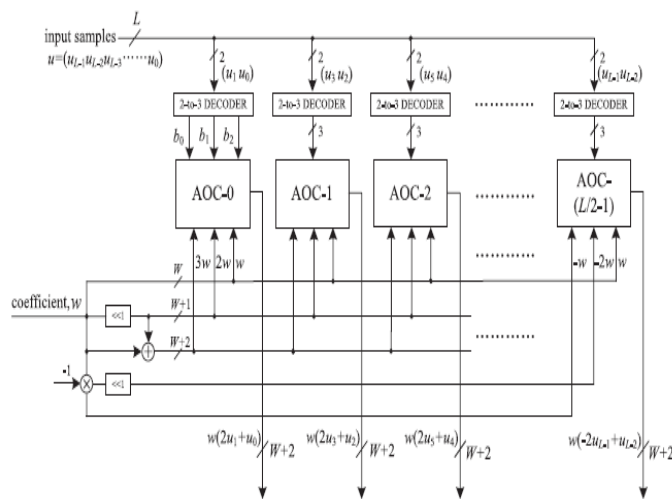


Fig 5. Structure of PPG (AOC stands for OR/AND cell)

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WEIGHT-UPDATE BLOCK

The proposed structure for the weight-update block is shown in below. It performs N multiply-accumulate operations of the form $(\mu \times e) \times x_i + w_i$ to update N filter weights for each condition. Every the MAC units performs the multiplication of the shifted value of error with the delayed input samples x_i followed by the additions with the corresponding old weights. All the N multiplications for the MAC operations are performed by N PPGs, followed by N shift-add trees. The PPGs generates $L/2$ partial products corresponding to the each product of the recently shifted error value $\mu \times e$ with $L/2$, the number of 2-b digits of the input word x_i .

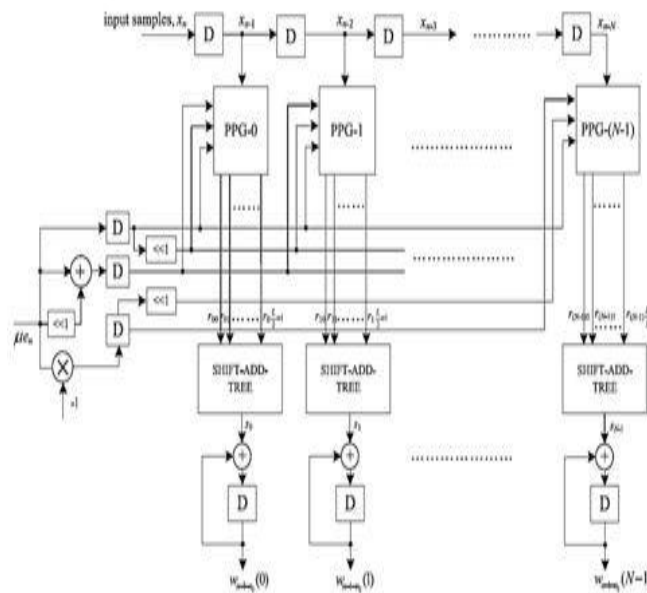


Fig 6. Structure of weight-update block.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

OUTPUT OF GATE COUNT:

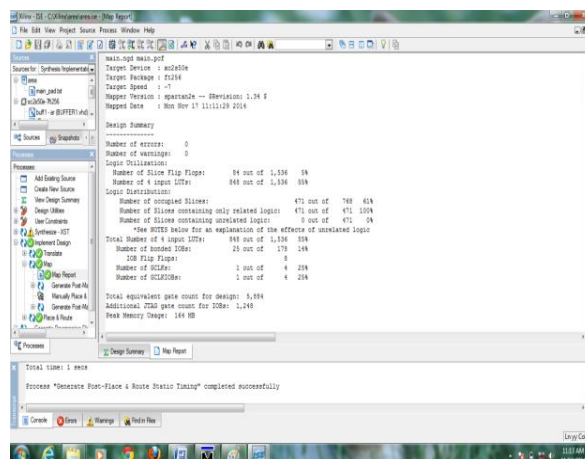


Fig 7. Output of gate count

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OUTPUT OF POWER ANALYSIS:

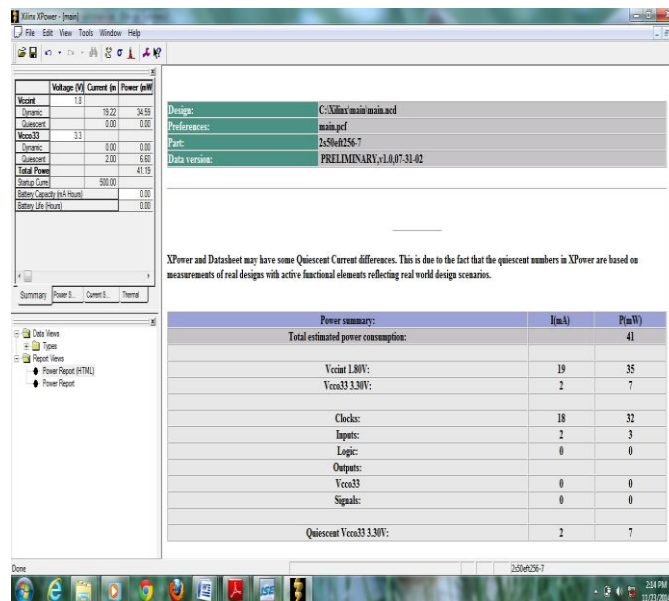


Fig 8. Output of Power Analysis

OUTPUT FOR LMS ADAPTIVE FILTER WITH DELAY

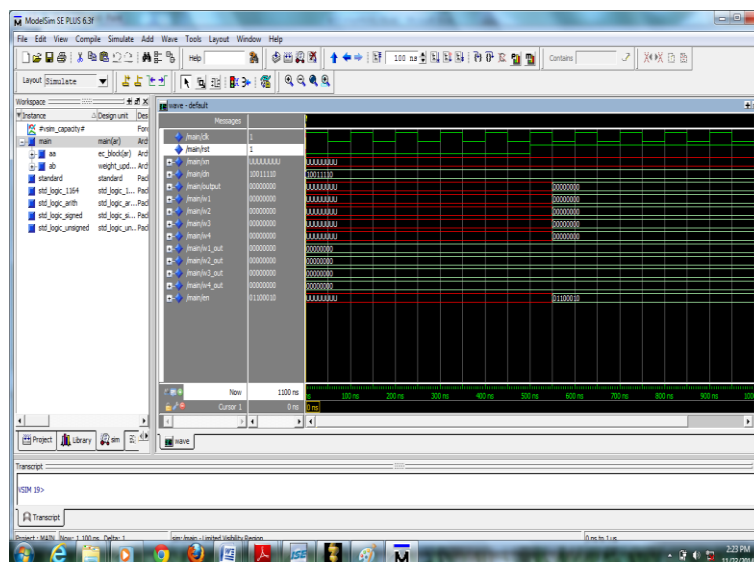


Fig 9. Output With Delay

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OUPUT OF LMS ADAPITIVE FILTER WITHOUT DELAY

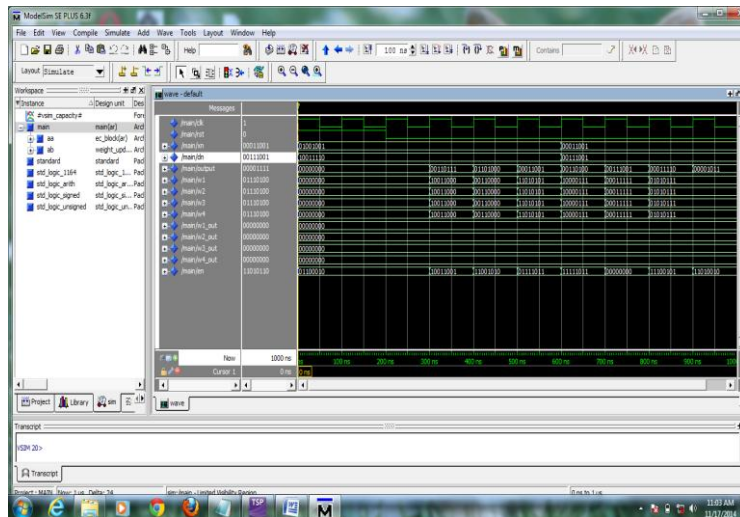


Fig 10.output without delay

TABLE

MODULE	AREA (By gate counts)	POWER (mW)
Fixed-Point LMS Adaptive Filter With Ripple Carry adder	5995	50
Fixed-Point LMS Adaptive Filter With Carry Select adder	5884	41

Table 1

V. CONCLUSION

We proposed an area–delay–power efficient low adaptation delay architecture for fixed-point implementation of LMS adaptive filter. So We used a novel PPG for efficient implementation of general multiplications and inner-product computation by common sub expression sharing. We have proposed an efficient addition scheme for inner-product computation to reduce the adaptation delay significantly in order to achieve faster convergence performance and to reduce the critical path. We proposed a strategy for optimized balanced pipelining across the time-consuming blocks of the structure to reduce the adaptation delay and power consumption.

The proposed structure involved significantly less adaptation delay and provided significant saving of ADP and EDP compared to the existing structures. We proposed a fixed-point implementation of the proposed architecture, and derived the expression for steady-state error. We also discussed a pruning scheme that provides nearly 25% saving in the ADP and 10% saving in EDP over the proposed structure before pruning, without a noticeable degradation of steady-state error performance. The highest sampling rate that could be supported by the ASIC implementation of the proposed design ranged from about 875 to 1015 MHz for filter orders 9 to 35. When the adaptive filter is required to be operated at a lower sampling rate, with a clock slower than the maximum usable frequency and a lower operating voltage to reduce the power consumption .

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