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# **Design of Low Power Non Volatile Magnetic Flip-Flop or Memories Based On Lector Technique**

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**ABSTRACT:** Power has becoming a burning issue in modern VLSI design. Non volatile memories like MRAM, FeRAM , ReRAM etc can save power by allowing the system power off in standby state. MRAM can be built up by using Magnetic Flip-flop like portable computer, Floppy disk, CD's etc. Comparing to the conventional Flip-flop STT-MRAM can save the power and retain the data by using 22 nm technology .Advanced computing systems suffer from high static power due to rapidly rising leakage currents in deep sub-micron MOS technologies. In this paper performed electrical simulations to validate its functional behaviors and evaluate its performance by using spice model of STT-MRAM. Some mechanisms like checkpointing/power gating has been undergone in this NVM(non-volatile memories). There are numerous methods proposed to control leakage power dissipation. LECTOR is one of the techniques used for leakage reduction without affecting the dynamic power. The proposed design requires less design effort and offers greater power reduction and smaller area cost than the previous method. in leakage power reduction when compared to all other existing leakage reduction techniques. Using this LECTOR technique, power efficiency becomes better.This paper presents the analysis for leakage current in Static RAM implementing LECTOR technique

**KEYWORDS:** Checkpointing, flip-flop, STT-MRAM, non-volatile, LECTOR

## **1. INTRODUCTION**

Non-volatile memories (NVM) are to be integrated in Flip-Flops or memories to allow system power-off in standby state and save power. STT-MRAM has high speed, low power, and infinite endurance. Power consumption consists of dynamic and static power, the main function of dynamic power is to charging and discharging of load capacitance at an average frequency over any given interval time.. There are various techniques to reduce the static power dissipation. Spin transfer torque-Magnetic random access memory (STT-MRAM) can be used to reduce the power but it has high write energy. Recently microprocessors are composed of a large number of registers or flip-flops, which are based on CMOS volatile memory for high speed. To retain data in standby mode, volatile memories need power all the time, it leads to high static power. A number of solutions are under intense investigation by both industries and academia. To overcome that some non volatile memories has been introduced such as ReRAM, MRAM, phase change memory.

By using this NVM flip-flops, computing systems can be completely powered off in standby mode and the secured data can be also retrieved instantly. This new computing function allows zero standby power and particularly for normally-off electronics. Here STT-MRAM has been used to achieve ultra low power microprocessor. In NV, Normally off processor can replaces the CMOS FF by magnetic flip-flop and SRAM by STT-MRAM. Data can be kept up without power supply and the system consumes zero leakage power. The reliability of the system has been improved and the data can be retrieved when the system is on. The architecture cannot operate as fast as CFF and the switching speed cannot be led to some GHz, energy for storing the STT-MRAM is high. STT-MRAM can be built by using MTJ structure has fixed FM layer has fixed magnetic orientation, oxide layer and Variable magnetic orientation. In this

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paper new proposed magnetic flip-flop design consumes ultra low power compared to conventional flip flop architectures.

Magnetic Flip-Flop (MFF) stores the intermediate computing data in non-volatile mode. It was firstly proposed in 2006 and the idea is to replace one of the master or slave parts by the circuit similar to a non-volatile configuration point. The first prototype was presented in 2008 by NEC based on hybrid process and its high performance up to 3.5 GHz .MFF is expected to make low standby power for electrical appliances like LCD TV, PC and portable devices in the next few years. MFF is the key element to build non-volatile logic circuits and allows true instant on/off and zero standby power. As the switching of MRAM cell consumes always much more than a SRAM, two special techniques have been developed to relax the switching power of MFF, which should be operating with a very high frequency  $f_{switch}(>MHz)$ . One is checking point: MFF stores the intermediate data in MTJs with a manageable slow frequency (e.g. 1 KHz) and the other is “write before sleep”: MFF stores the intermediate data in MTJs, as there is a request by user or in case of power failure.

Future trends in MRAM are error detection mechanisms and MRAM enhances FPGA density and energy consumption, core processor and hierarchy memory.

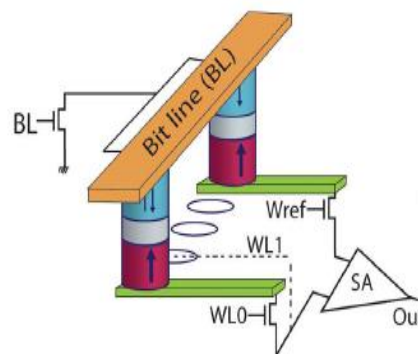


Fig 1.1 structure view of a STT-MRAM cell

## II. SPIN TRANSFER TORQUE MRAM

As the basic storage element in STT-MRAM, perpendicular anisotropy Magnetic Tunnel Junctions (p-MTJ) can store data by configuring its magnetization orientation of the free layer. Due to the tunnel magneto-resistance (TMR) effect [26], the resistance of p-MTJ depends on the relative orientation of magnetization in the free and pinned ferromagnetic layer. As shown in Fig. 1.1, for the parallel configuration ( $R_p$ ) the resistance is low (logic ‘0’ is stored), while for the anti-parallel configuration ( $R_{ap}$ ) the resistance is high (logic ‘1’ is stored). For switching between these configurations, the magnetization orientation of the free layer follows the direction of the applied switching current.

A pair of MTJs connected to the storage nodes of a standard SRAM cell with CIMS architecture enables fully electrical store and restore operations for nonvolatile logic information. Low power consumption is a major issue in nowadays electronics systems. This trend is pushed by the development of data center related to cloud services and soon to the Internet of Things (IoT) deployment. Memories are one of the major contributors to power consumption. . Another advantage of this new MFF is its easy extension for multi-bit registers (e.g. 64-bit), which allows low area overhead by sharing peripheral control circuits. Besides, multi NV storage can improve the reliability of the computing system against power failures and soft errors.

### 2.1 checkpointing

The checkpointing mechanism operates periodically a snapshot of the system state, and stored into non-volatile storage. Upon detection of power supply failure or error event, the check point works. In checkpointing scheme, the current state is stored in the hard drive disk (HDD), Storing a global checkpoint using this technique is

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expensive and can stop the execution for a long time. The total checkpoint overhead goes beyond 10% of the total execution time. Checkpointing is a good solution to keep both data reliability and achieve ultra low power by reducing the switching frequency. When power failures occur, the system can be instantly off/on and the starting point can be arbitrarily chosen. The main objective of checkpoint is activating the checkpoint when the system enters into standby state. By using power-gating technique supply voltage is cut off. When the power on the data can be restored instantly and save the power.

## 2.2 power-gating technique

Power gating technique saves the static power. PG has demonstrated in how to effectively use micro-architectural information to detect when to enable power gating mechanism in a microprocessor's unit. They propose an idle-Count algorithm to predict when to assert the PG signal. Due to this algorithm, the PG can be activated even for short standby time leads to energy savings. In order to simplify the mechanism and conserve area, the writing circuit of all the transistors are sized to reduce the write supply voltage to  $V_{dd}$  logic. Therefore, all blocks are powered by the same logic  $V_{dd}$  (1.1 V), and share the same sleep transistor. MFF can be fully shut down and the leakage power can be completely suppressed in standby mode. As different logic blocks will not switch simultaneously, the peak current will not occur at the same time, the sleep transistor can be trimmed to save area. Different energies consumed in a system with power gating operation. Normally during the standby mode, the energy required for PG is higher than the static energy consumed.

## 2.3 Self enable control circuit

“Self-Enable” circuit is to replace the fixed writing pulse by a sequence of self-enabled write/read operations whose number is determined. The detailed schematic of the self-enabled switching circuit is shown below. Self-enable switching allows the programming pulse to be shortened and obtains the best power efficiency.

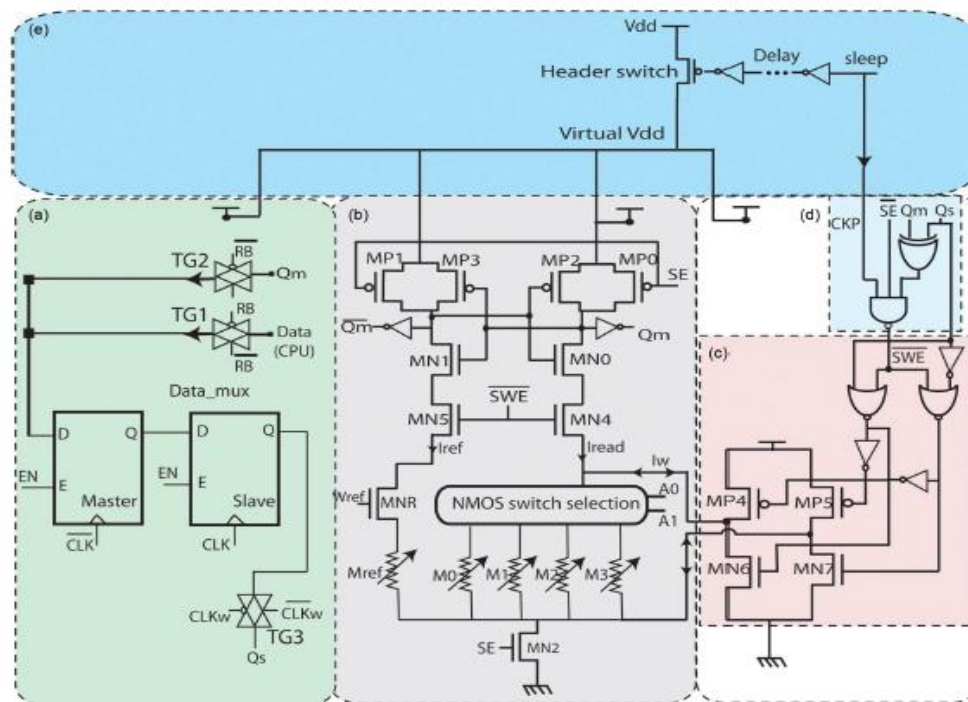


Fig 2.1 (a) CMOS Volatile D-latch, (b) 4-bits STT-MRAM including Sense Amplifier circuit (c) STT writing circuit, (d) Self-Enable control circuit, (e) Power gating cell using sleep p-MOS transistor (header switch).

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## III. OPERATION OF MAGNETIC FF

### 3.1.1 CMOS FLIP-FLOP (CFF)

The above fig 2.1(a) shows the CMOS Volatile D-latch, with three additional transmitter gates (TG1, TG2, TG3) for transferring data between CFF and STT-MRAM. When rollback signal "RB=0", "Data\_mux" is connected to "Data" and the CFF can receive data from the computing unit driven by the clock signal "CLK". When "RB=1", "Data\_mux" is connected to "Q<sub>m</sub>" and the CFF can load one of the four contexts. The transmitter gate TG3 is used for data sampling between CFF and STT-MRAM is shown in fig 2.1(a).

### 3.1.2 STT-MRAM CIRCUIT

In STT-MRAM circuit, during the sensing mode SE=1 and SWE\_bar=0, the write current source is disabled and the transistors MN4 and MN5 are turned on to connect the SA (MN0-MN1, MP0-MP3) to the NMOS switch selection. Once the NMOS switches on through address "A0/A1" to connect the SA to drive the read current, I<sub>read</sub>. By activating W<sub>ref</sub>=1, the transistor MNR is turned on. As "SE" is set to '1', MN2 is turned on both I<sub>read</sub> and I<sub>ref</sub> flow to the ground is shown in fig 2.1(b). As a result, the difference between these two currents will charge or discharge the output "Q<sub>m</sub>" to get logic data read out.

### 3.1.3 CONVENTIONAL BIDIRECTIONAL STT-MRAM WRITING CIRCUIT

In conventional writing circuit for STT-MRAM write operation SWE\_bar=0, the transistors MN4 and MN5 are turned off to isolate between the read and the write operations so that the read current will not be disturbed by the write current. To write logic '0' the transistors MP4 and MN7 are turned on and the transistors MP5 and MN6 are turned off, the write current generated flows. To write logic '1', the reversed current is generated by turning on the MP5 and MN6 and turning off the MP4 and MN7. The switching may happen at any moment inside the large fixed write pulse, in addition the write current is applied to all p-MTJs even when the current p-MTJ state "Q<sub>m</sub>" is equal to the expected data "Q<sub>s</sub>". Therefore, unnecessary energy is lost. The energy to store "0101" is 4.5pJ from this simulation. In order to save this wasted energy while keeping high data reliability, add a small combinatory logic block to build up a self-enabling write circuit is shown in fig 2.1(c).

### 3.1.4 SELF-ENABLE CONTROL CIRCUIT

The "Self-Enable" circuit is to replace the fixed writing pulse by a sequence of self-enabled write/read operations. The schematic of the self-enabled switching circuit is shown in fig 2.1(d). By activating CKP=1, the self enabled SWE\_bar=0, the current p-MTJ state "Q<sub>m</sub>" and the expected state "Q<sub>s</sub>" are different, and no sensing operation is ongoing SE=0. The switching pulse is applied when "Q<sub>m</sub>" is equivalent to "Q<sub>s</sub>". If there is a read back, the switching current is applied only for N<sub>m</sub> bits where "Q<sub>s</sub>" is different to "Q<sub>m</sub>". The switching energy reduction E<sub>s</sub> can be calculated using self enable technique. In our simulation the four p-MTJs are initialized at logic '1111' and the expected data "Q<sub>s</sub>" is '0101'. In fact, only two out of four bits are written. The energy reduction is estimated and the write energy of the four p-MTJs is reduced.

### 3.1.5 POWER-GATING CIRCUIT

To simplify the PG mechanism and conserve area, the writing circuit of all the transistors are sized to reduce the write supply voltage to V<sub>dd</sub> logic. Therefore, all blocks are powered by the same logic V<sub>dd</sub> (1.1 V), and share the same sleep transistor. During the standby mode the MFF can be fully shut down and the leakage power can be completely suppressed. As different logic blocks will not switch simultaneously, at the same time the peak current will not occur, the sleep transistor can be trimmed to save area. Once the standby mode is detected, the "sleep" signal is activated and the checkpoint "CKP" is forced. The delay will depend only on the writing latency of STT-MRAM (e.g.4 ns/bit). Power gating shows the simulated waveform for MFF power gating and different operations before and after the cutting-off power is shown in the Fig.2.1(e).

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### IV. PROPOSED LECTOR TECHNIQUE

LECTOR is used for reducing the leakage power based on the effective stacking of transistors in the path from supply voltage to ground. The LECTOR technique is based on the concept that “a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path.” In this process, two leakage control transistors (LCTs) were introduced in each CMOS gate, a PMOS (LCT1) added to the pull-up network and a NMOS (LCT2) added to the pull-down network and the gate terminal of one LCT is controlled by the source terminal of the other, such that one of the LCTs is always near its cutoff region of operation for any input(s) given to the CMOS gate, thus providing additional resistance in the path from supply to ground, decreasing the sub-threshold leakage current, thereby the reducing the static power.

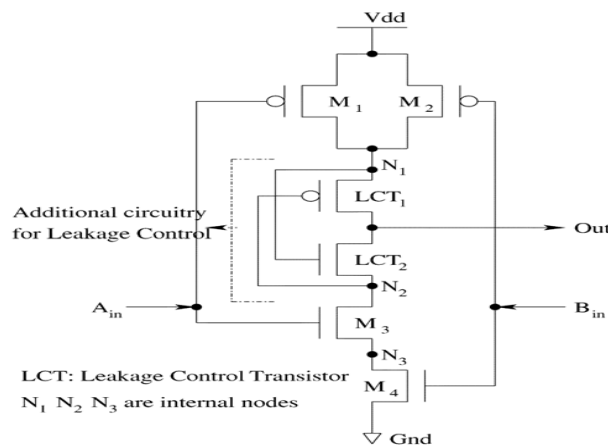


Fig.4.1 Lector technique

### V. WORKING PRINCIPLE OF LECTOR

A CMOS NAND gate with the addition of two leakage control transistors is known as LECTOR NAND. Two leakage control transistors LCT1 (PMOS) and LCT2 (NMOS) are introduced between the nodes N1 and N2 of the NAND gate. The drain nodes of the transistors LCT1 and LCT2 are connected together to form the output node of the NAND gate. The source nodes of the transistors are connected to nodes N1 and N2 of pull-up and pull-down logic, respectively. The switching of transistors LCT1 and LCT2 are controlled by the voltage potentials at nodes N2 and N1 respectively. This ensures that one of the LCTs is always near its cutoff region, irrespective of the input vector applied to the NAND gate. It can be observed that the output voltage variation is similar in both the cases. Consider the dc characteristics of the LCT NAND gate. When  $A_{in} = 1V$  and  $B_{in} = 0V$ , the voltage at the node N2 is 800 mV. To turn LCT1 completely to OFF state the voltage is not sufficient. Hence, the resistance of LCT1 will be lesser than its OFF resistance, allowing conduction. Even though the resistance of LCT1 is not as high as its OFF state resistance, it increases the resistance of  $V_{dd}$  to ground path, controlling the flow of leakage currents, then the leakage power has been suppressed and saves the static power.



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## VI. RESULTS AND DISCUSSION

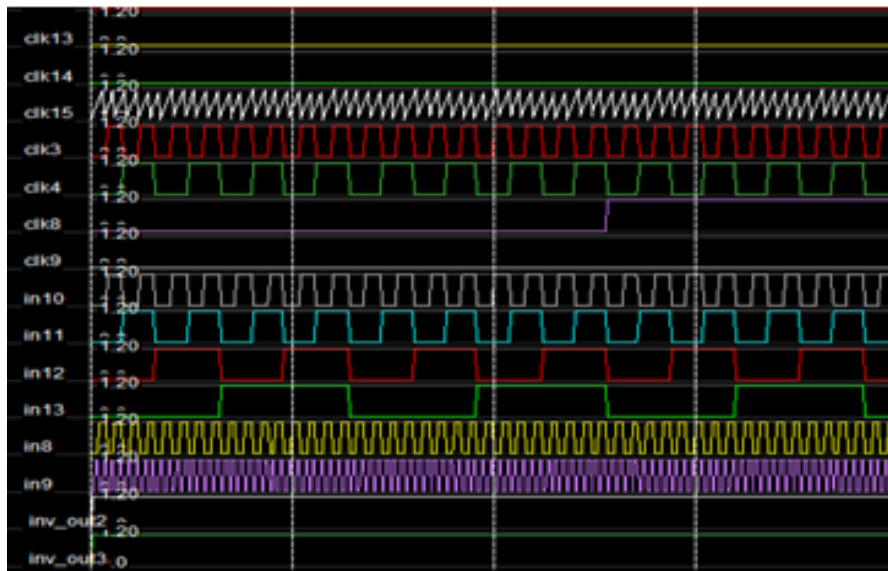


Fig 6.1 Existing Simulation result of MFF

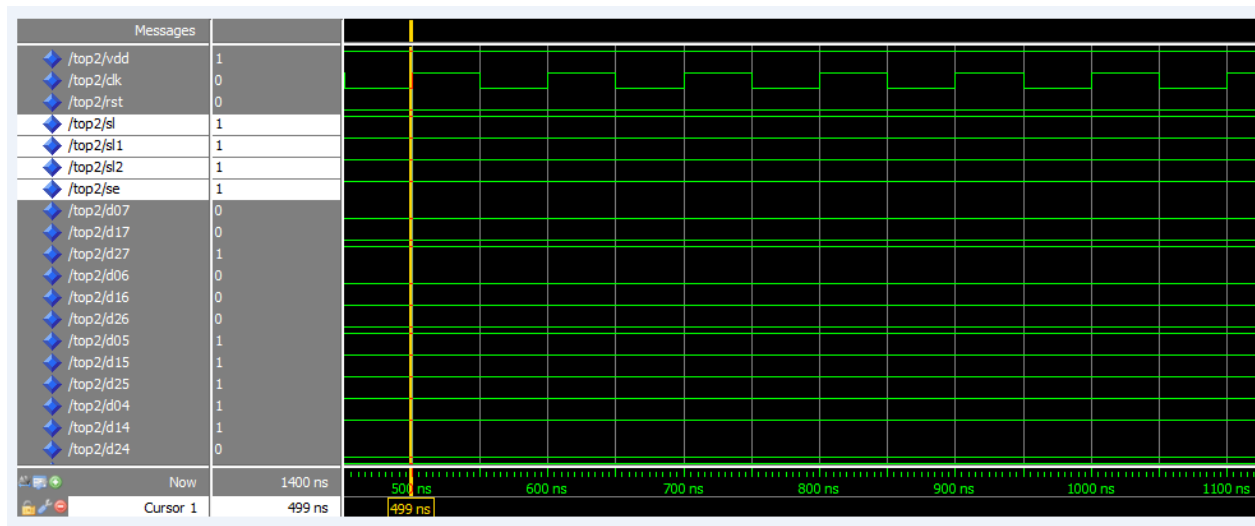


Fig 6.2 simulation result of LECTOR technique

## VII. CONCLUSION

The scaling down of device dimensions, supply voltage, and threshold voltage for achieving high performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. we proposed a new magnetic flip-flop (MFF) integrating four contexts with little area overhead. It can be used as a key element in the future memory hierarchy architectures to achieve a “normally off” computing system. To achieve ultra low power two mechanisms has been used. The first one is the checkpointing/power-gating operation used to suppress the standby static leakage power by cutting off the power supply voltage. The 3D structure of STT-MRAM allows the

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checkpointing operation to achieve tradeoff between speed and energy. The second one is the Self-Enable switching, is to reduce significantly the large margin of the switching current to avoid errors. This paper presents "LECTOR" to tackle the leakage problem. LECTOR uses two additional self controlled transistors. Like other leakage reduction techniques, such as sleepy stack, sleepy keeper, etc, LECTOR also achieves leakage power reduction but with the advantage of not affecting the dynamic power as this technique does not require any additional control and monitoring circuitry like in and also maintains exact logic state. Comparing to CFF and STT-MRAM power has been consumed but has high static power. Using LECTOR technique leakage current suppressed and saves the static power is shown in fig 6.2.

By using an accurate spice model and a commercial 20 nm CMOS design kit, functionality and performance of the new MFF was validated and evaluated. A prototype of this circuit is under development to demonstrate experimentally its performances in our group. We are simulating the MFF shown in Fig.6.1 to address some specific applications and evaluate the system-level performance of this new MFF.

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