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Design of Low Power Dual Edge Triggered Flip Flop Based On Signal Feed through Scheme

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ABSTRACT: A low power dual edge triggered flip flop based on a signal feed through scheme is presented. The power consumption is the major problem in circuit design. The proposed design reduces power and delay compared to explicit pulse triggered flip flop. Reducing the number of transistor in the stack and increasing the number of charge path leads to higher operational speed compared to others flip-flops. Using CMOS 90nm technology dual edge triggered flip flop consumes low power.

KEYWORDS: flip flop, low power, delay, dual edge, area

I. INTRODUCTION

The dynamic power consumption in the clock tree depends on the frequency, and the load of clock tree. If the sampling of the input is performed in both rising and falling edge of clock (double-edge triggered), then for same applications and operational speeds, the frequency of the clock can be half of the clock frequency of the single edge triggered FF. Low-Swing clock Double-edge triggered Flip-Flop (LSDFF). Double-edge triggered Feedback Flip-Flop (DFFF) has less dynamic power consumption, static power, and delay compared to the previous flip-flops.

Several researchers have worked on low power flip-flop design, but they are mostly focused on one or a few types of flip-flops or applications. The need for comparing different designs and approaches is the main motivation for this paper. The main trade-offs of any flip-flop are very important for a design engineer when designing a circuit or for a tool that automates the process of design. This design introduces our new flip-flop design and presents the comparative evaluation for the new flip-flop against the previous discussed flip-flop designs with the least peak power obtained. The proposed design adopts two measures to overcome the problems associated with existing pulse triggered flip flop. First one is reducing number of nmos transistors stacked in the discharging path. Second one is supporting the mechanism to enhance the pull down strength when the input data is 1. Dual edge triggered flip flop shortens the delay by passing the data at both rise and fall edge. Positive edge triggered passes the data when the clock is from 0 to 1. Negative edge triggered passes the data when the clock is from 1 to 0. Hence this gives better performance for power and delay. Thus the switching power can also be minimized.

II. EXISTING DESIGN

The pulse generation can be classified into implicit and explicit type. Implicit type does not occupy much space and is inbuilt within the circuit, no external signals are needed. Power consumption is less in implicit type but it suffers from longer discharging path. In explicit type pulse generator and latch are separate. Hence the power consumption is more. Thus to reduce the power consumption and circuit complexity a single pulse generator can be shared by a group of FFs. Here explicit type designs are discussed. Some existing flip flops are compared here.

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A.CONVENTIONAL EXPLICIT TYPE P-FF DESIGNS

1.Fig a. shows a classic explicit type data close to output.It contains a NAND-logic-based pulse generator and a semidynamic true-single-phase-clock (TSPC) . In this P-FF design, inverters I3 and I4 are used to store data, and inverters I1 and I2 holds the internal node X.The delay of three inverters determine their pulse width.A drawback here is even if their static input is 1 the internal node X is discharged on every rising edge of the clock. some techniques are used to overcome this problem.They are conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme.

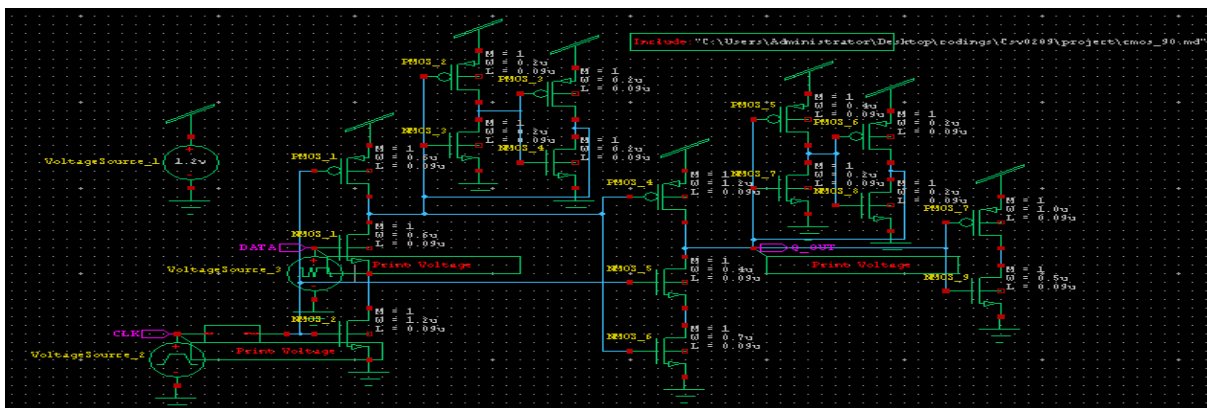
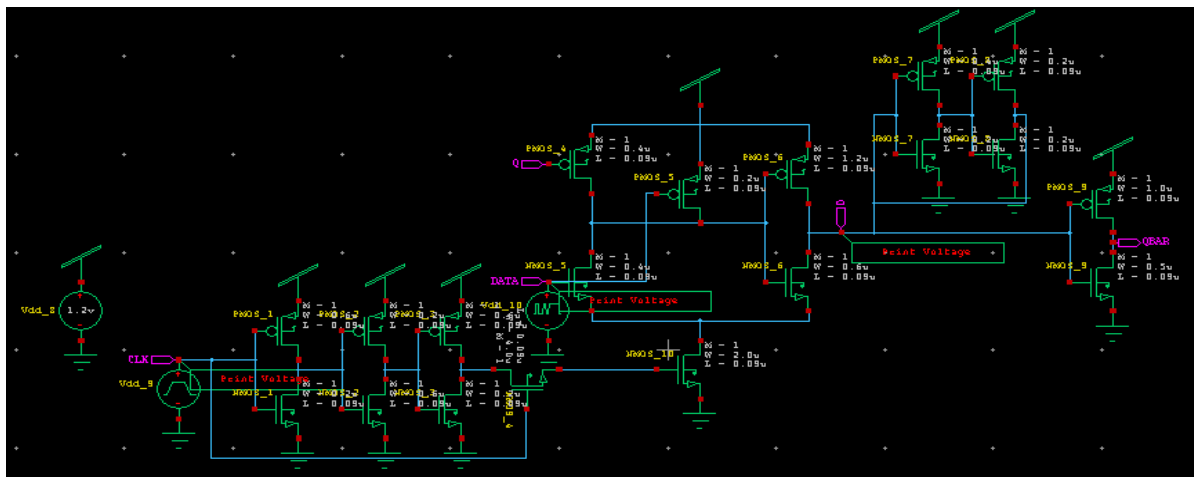


Fig. 1. Conventional P-FF designs. (a) ep-DCO

. Fig. 1(b) static conditional discharge technique.It has longer data to Q delay compared to CDFP.since three stacked transistor is used it faces worst case delay.To overcome this delay a pull down circuitry is used but the disadvantage is that extra layout area and power consumption



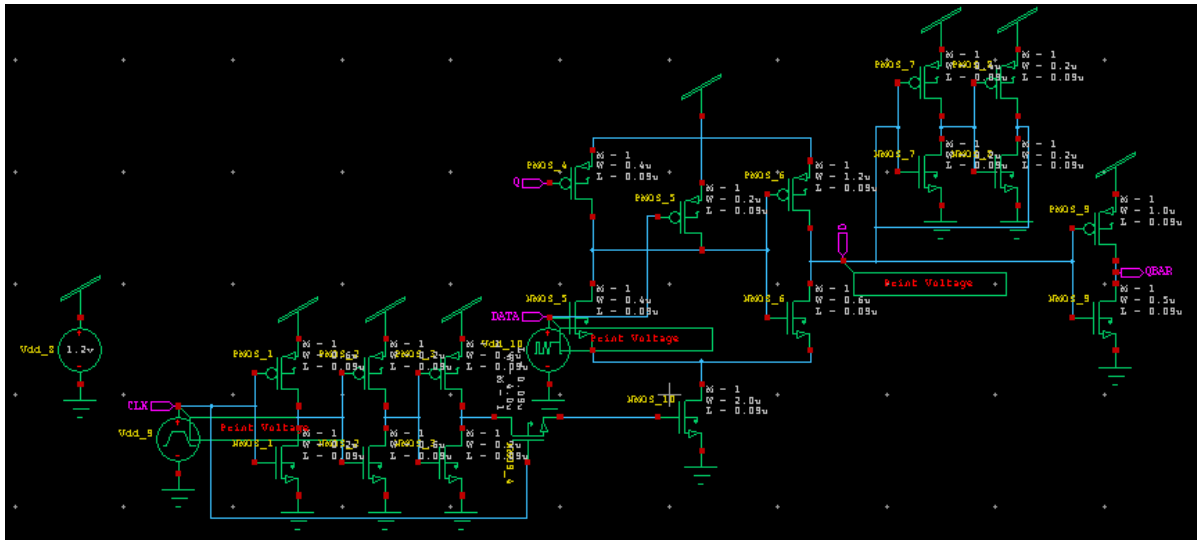
(b) Static-CDFP

The modified hybrid latch flipflop (MHLFF) shown in Fig. 1(c). The keeper logic at node X is removed.This is satisfied by having a weak pull-up transistor MP1 controlled by the output signal.Thus Q maintains the level of node X when Q equals 0. There are two drawbacks in the MHLFF design. First, a prolonged 0 to 1 delay is expected. Second, node X becomes floating sometimes and its value may drift causing extra dc power.

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(c) MHLFF

B.PULSE TRIGGERED FLIPFLOP

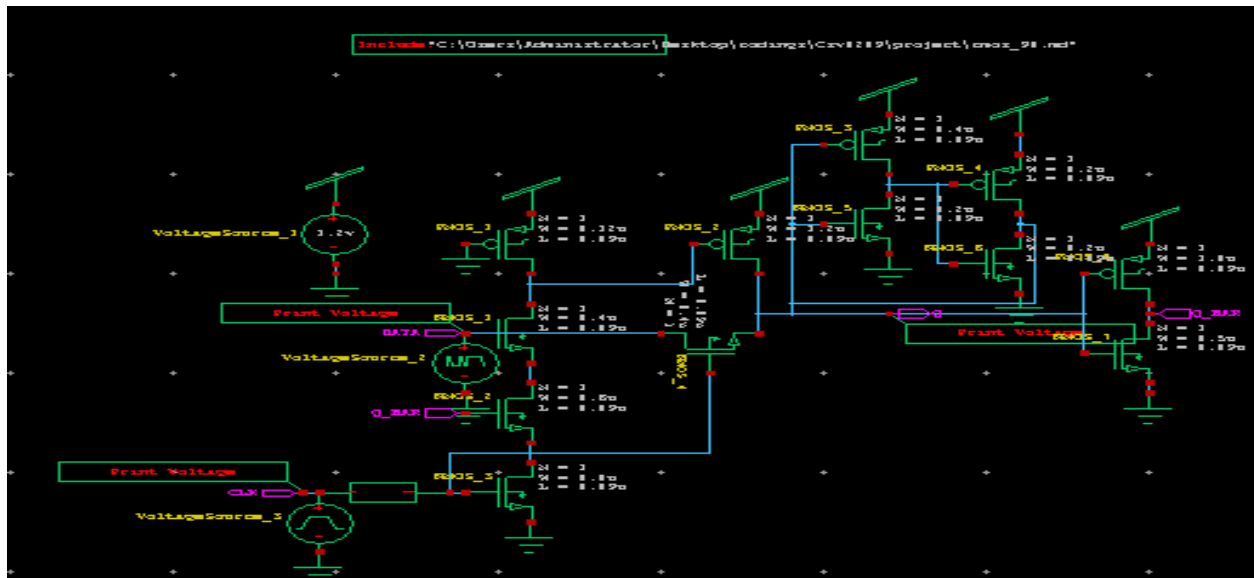


Fig.2 pulse triggered flip flop

All the above circuits have delay from 0 to 1 data transition. To overcome this delay we use signal feedthrough scheme. This design has three major differences compared to other circuits. First, the weak pull-up PMOS transistor is grounded. Here, pseudo NMOS logic style is followed, thus the internal node X is saved. Second, a pass transistor is used to feed the input directly. The pass transistor is controlled by clock and thus reduces delay during transition of data.

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III. PROPOSED DESIGN

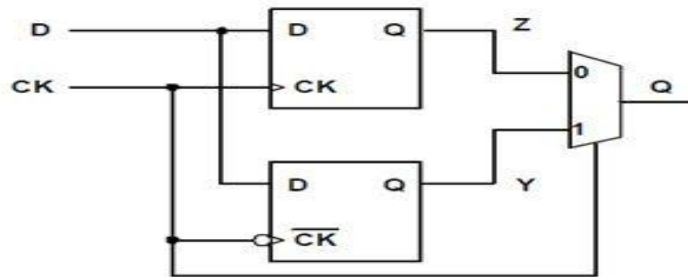


Fig.3.double edge triggered flip flop

The input of the flip-flop is transferred to the output at the rising and falling edges of the clock. since pass transistor is used the power consumption is minimized. The data is triggered at both the edges simultaneously hence the clock power is reduced. The clock power distribution is major problem hence the above technique is preferred. This design gives high throughput compared to single edge triggering. The frequency needed for dual edge triggering is half the frequency compared to single edge triggering.

The dual edge triggered flip flop thus leads to higher operating speed by reducing delay. It also reduces area by triggering both positive and negative edges simultaneously. It also reduces sensitivity to noise pulses.

IV. COMPARISON TABLE

DESIGNS	Explicit pulse data close output	Conditional discharge flip flop	Static conditional discharge flip flop	Modified hybrid latch flip flop	Pulse triggered flip flop	Dual edge triggered flip flop
POWER (μW)	34	27	34	26	24	21

Table. Comparison of various designs

V. RESULTS AND DISCUSSION

The results obtained by using tanner 14.0 version. This compares the power for various design of flip flops and thus shows the improvement in power and delay. Thus the simulation results are obtained for dual edge triggered flip flop along with signal feed through scheme.

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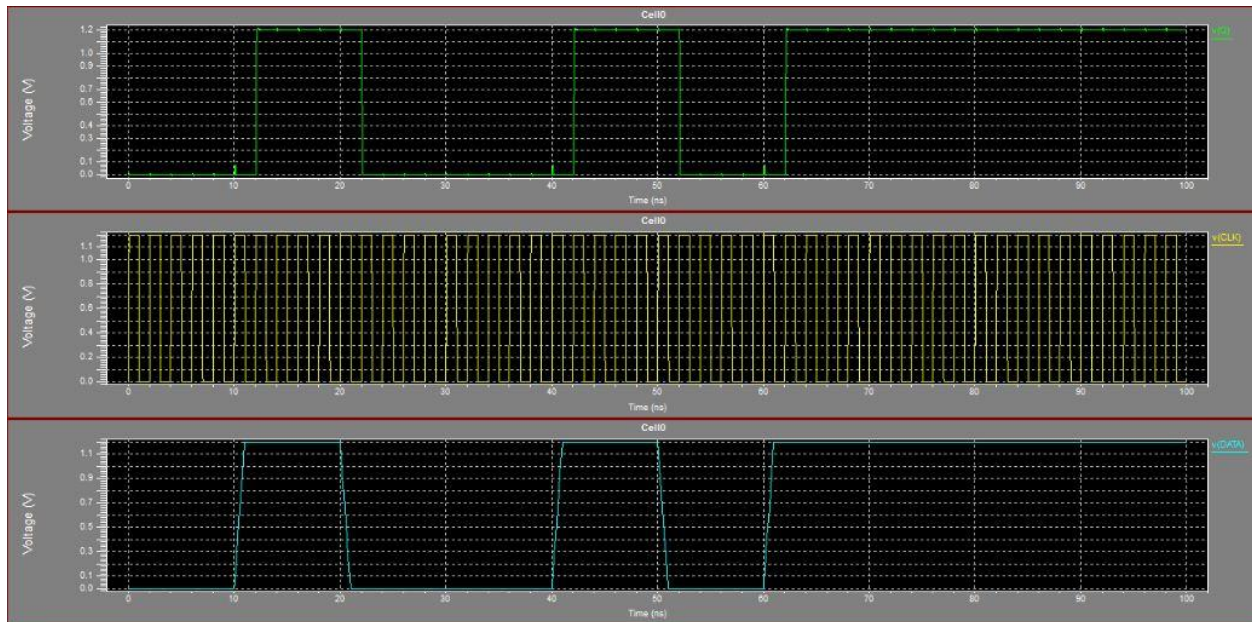


Fig.5.a.voltage v_s time

In Fig 5.a.The delay is reduced by comparing voltage and time since the pass transistor is used here.This shows the signal characteristics

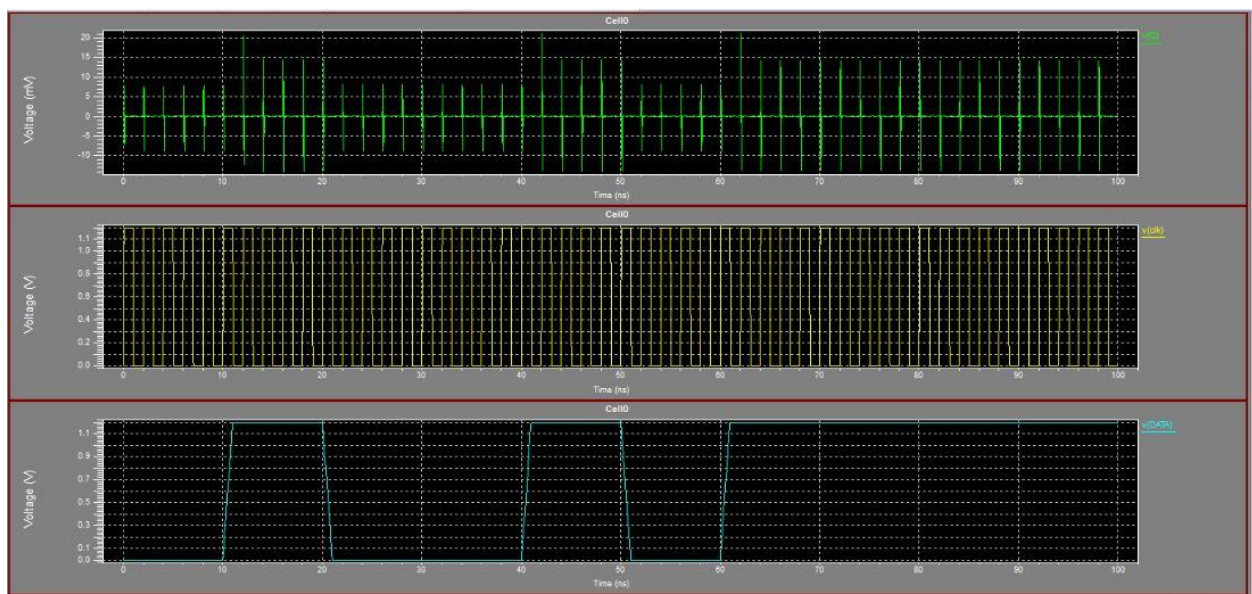


Fig.5.b.voltage v_s time

In Fig 5.b.The dual edge triggered flip flop further reduces the power and delay by comparing voltage and time.The signal feed through scheme and dual edge triggered flip flop also enhances speed.

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V.CONCLUSION

Dual-edge-triggered flip-flops (DET-FF's) offer potential advantages with respect to speed and power supply requirements. since data can be transmitted at both rise edge and fall edge dual edge triggered flipflop consumes lowpower. It also reduces delay when the input is given. Nearly 40 percent the power consumption can be made. Already the pass transistor is used to enhance the signal feed through directly in order to reduce power. In addition to that dual edge triggered flip flop is used in the design.

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