

# **Design of Low Power Double Tail Comparator by Adding Switching Transistors**

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**ABSTRACT:** The low power double tail comparator is designed by adding switching transistor. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on comparison. The overall performance of the comparator is based on power consumption and speed. In the proposed comparator by adding more number of switching transistor below the input transistors, static power dissipation going to reduce. The positive feedback during the regeneration is strengthened, which results in low power. Compared with existing comparator, in the proposed comparator, both the power consumption and delay time are significantly reduced. Post-layout simulation results in a 0.18- $\mu$ m CMOS technology confirm the analysis results.

**KEYWORDS:** Switching transistor, Low Power, Delay

## **I. INTRODUCTION**

Comparator plays an important role in high speed analog to digital converters. A comparator is a device, which compares two currents or voltages and produces the digital output based on the comparison. Comparators are known as 1-bit analog to digital converter and for that reason they are mostly used in large quantity in A/D converter. Dynamic comparators are widely used in the design of high speed ADCs due to speed, low power consumption, high input impedance and full- swing output, dynamic latched comparators are very attractive for many applications such as high-speed analog- to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers.

In the double tail comparator signal is given to input transistors, produce the output based on the input values and it has two outputs. The output going to discharges at different rate based on the input voltage given to the comparator. A clocked comparator generally consists of two stages. The first stage is to interface the input signals. The second stage consists of two cross coupled inverters, where each input is connected to the output of the other. The static power dissipation in double tail comparator reduced by adding switching transistors. The power ground path is switched off either by a NMOS or PMOS transistor.

In many low power applications comparator speed, power dissipation, power efficiency and number of transistors are more important. Fast speed and low power consumption are the two most important parameter of the comparator which is to be used in high speed ADCs. By using more number of switching transistor the power and delay reduced in proposed double tail comparator.

## **II. EXISTING DESIGN**

### *1. Conventional Dynamic Comparator:*

This comparator widely used in A/D converters, relaxation oscillator, and null detector with high input impedance, rail-to-rail output swing and no static power consumption. These comparators are clocked and they produce output after the transition of the clock. The value of the input to a clocked comparator is only of concern in a short time interval around the clock transition.

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The modes of operation depend on the clock input given. CLK = 0 is called reset phase and CLK = Vdd is called as evaluation phase. When CLK = 0, nMOS transistor is off and pMOS transistor is on. When CLK = Vdd, nMOS is on and pMOS transistor is off. The speed of this comparators is very high and the power dissipation of this comparators can be very low. The comparators using clock signals are called dynamic Comparators. Regenerative feedback is often used in dynamic comparators and also in non-clocked comparators.

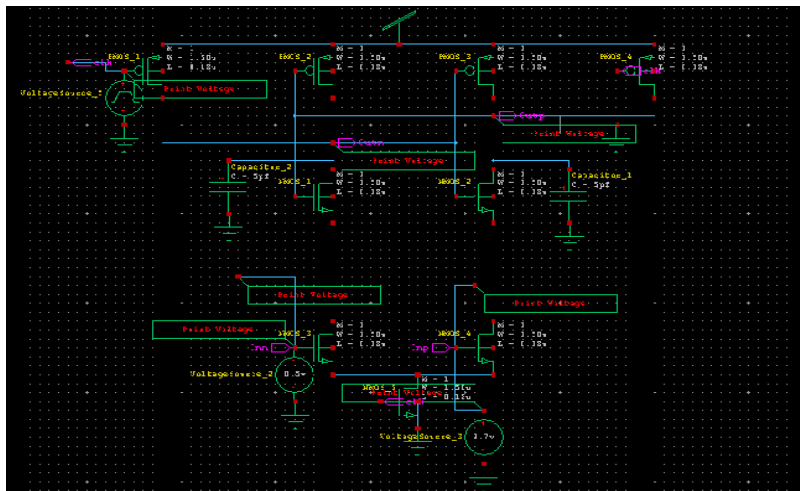


Fig.1 Conventional Dynamic Comparator

The operation of the comparator is explained below. During the reset phase when CLK = 0 the Mtail is in off, reset transistors (M7– M8) pull both output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset.

After when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), are pre-charged to VDD, then started to discharge with different discharging rates depending on the input voltage (INN/INP) given to the comparator.

Now consider this case where VINP > VINN, then the Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding PMOS transistor (M5) will turn on in the latch regeneration caused by back-to-back inverters and M4, M6). Thus Outn goes to VDD and Outp discharges to ground. If VINP < VINN, the circuits operate inversely.

## 2. Conventional Double Tail Comparator:

Double tail comparator is used in low power applications. In this method, increase the voltage difference between the output nodes in order to increase the latch regeneration speed. For this purpose, two control transistors has been added to the first stage in parallel to M3 and M4 transistors in a cross-coupled manner.

Double tail comparator has two operation modes, the reset phase and another one is decision making phase. The double tail enables both a large current in the latching stage and in Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset.

During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which makes transistors MR1 and MR2 to discharge the output(outn,outp) nodes to ground.

When CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), are pre-charged to VDD, then started to discharge with different discharging rates depending on the input voltage (INN/INP) given to the comparator.

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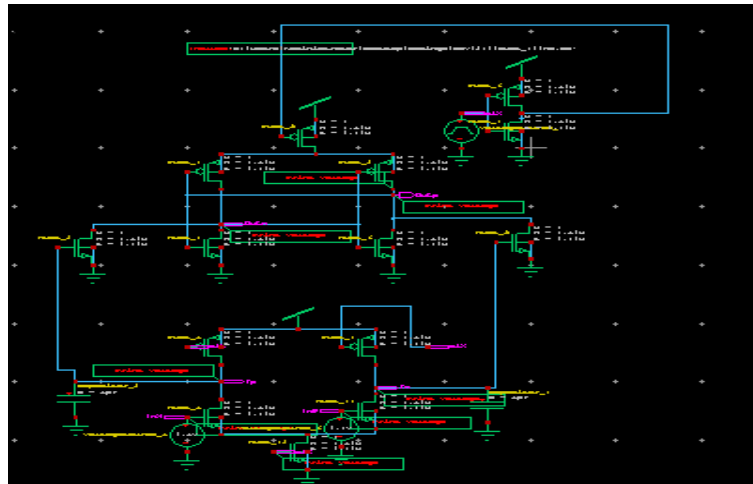


Fig.2 Conventional Double Tail Comparator

### 3. Double tail dynamic comparator :

In this type of comparator without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in reduced delay time. During reset phase (CLK=0 Mtail1 and Mtail2 are off avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD hence Mc1 and Mc2 are in cut off. Intermediate stage transistor MR1 and MR2 reset both latch outputs to ground. During decision making phase (CLK=VDD Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose  $V_{INP} > V_{INN}$ , thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding PMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely. One of the points which should be considered in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1) resulting in static power consumption. To overcome this problem, two NMOS switches are used below the input transistor.

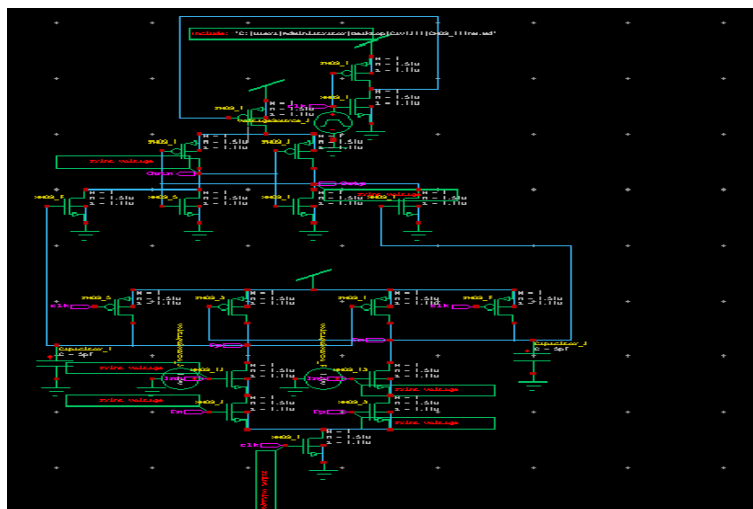


Fig.3 Double tail dynamic comparator

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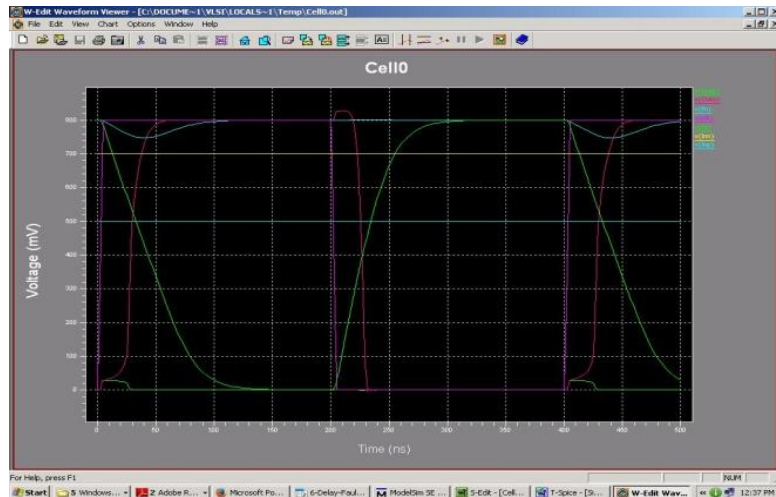


Fig.4 Simulated output for double tail comparator

Thus the average power consumption of the double tail dynamic comparator is  $12\mu\text{W}$  and the delay is  $7.4\text{ns}$ . Compared with the conventional double tail dynamic comparator it has less power and delay.

### III. PROPOSED DESIGN

#### ADDING SWITCHING TRANSISTORS

Here connecting four switching transistor in parallel manner below the INN and INP transistor to reduce the power consumption. By using more number of switching transistor  $\Delta V_{fn}/f_p$  is going to increased so the latch regeneration speed also increased. The power consumption and delay going to reduce.

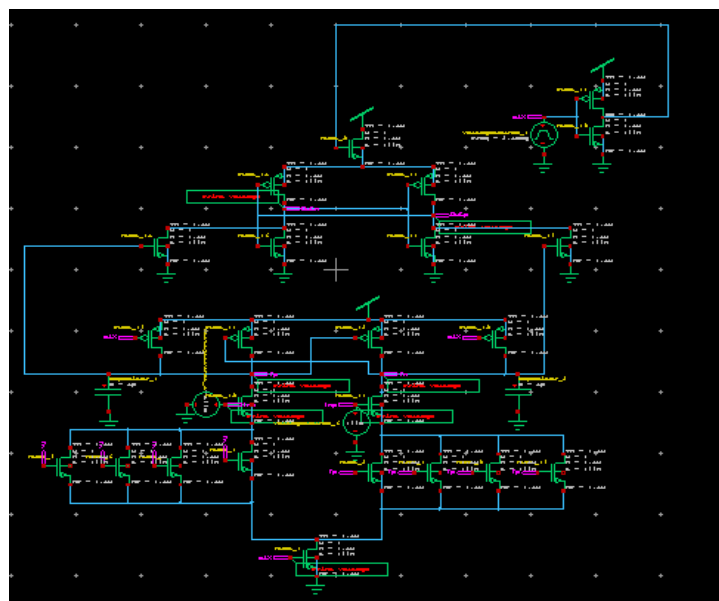


Fig.5 DCVS logic based comparator

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Depending up on the state of differential inputs, the two nodes connecting pullup and pull down network get pull down by one of the Nmos logic tree. The regenerative action of PMOS maintain the outputs outn and outp to be static and obtains full voltage swing Vdd or ground of its outputs.

During the reset phase when CLK = 0 and Mtail is off, reset transistors (M7– M8) pull both output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset.

During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the different rate dependent differential voltage.  $V_{INP} > V_{INN}$ , thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding PMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged. In this design by adding more number of switching transistors the delay time can be reduced. Based on the input voltage, output started to drop at different rates.

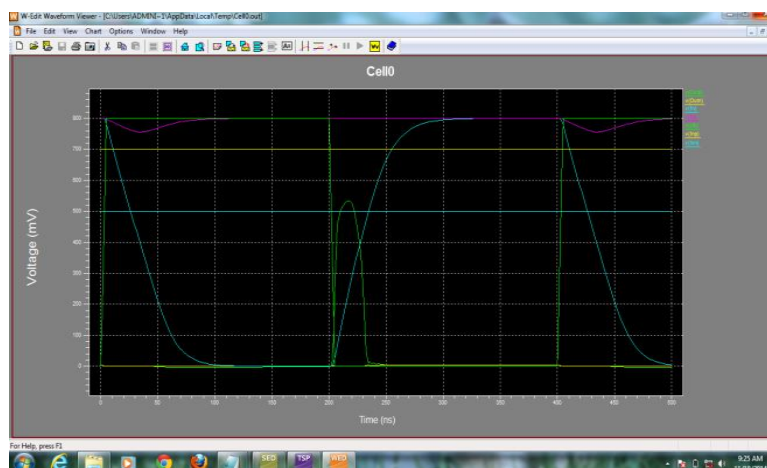


Fig.6 Simulation output of DCVS logic based comparator

If the input voltage given to the comparators are INN is 0.7v and INP is 0.5v, so that outn discharge faster than outp. Thus the simulated output shown in fig.6. The power consumption of this comparator is  $9.3\mu\text{w}$  is calculated by using T-SPICE tool.

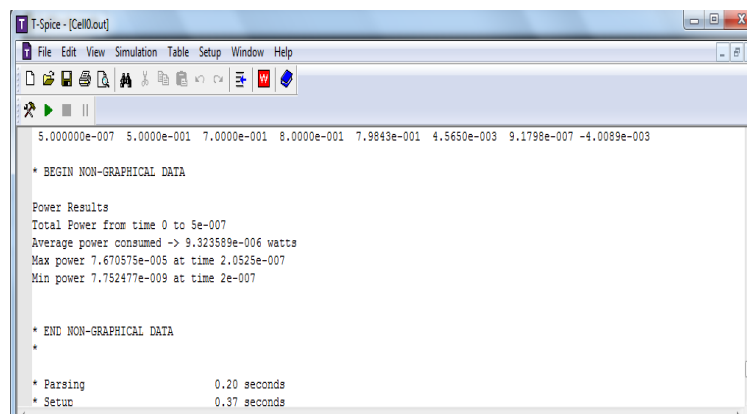


Fig.7 Power and delay analysis output

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TYPES	POWER	DELAY
Single tail comparator	$7.04 \times 10^{-7} = 7\mu\text{w}$	$6.61 \times 10^{-8} = 66\text{ns}$
Conventional double tail	$1.50 \times 10^{-5} = 15\mu\text{w}$	$7.50 \times 10^{-9} = 7.5\text{ns}$
Double tail comparator	$1.29 \times 10^{-5} = 12\mu\text{w}$	$7.40 \times 10^{-9} = 7.4\text{ns}$
Modified double tail comparator	$9.3\mu\text{w}$	Not found

Table.1 Comparison of Power and Delay of Various Comparators

## IV. CONCLUSION

Power and delay estimation is calculated by using post layout simulation with the help of Tanner EDA tools. In order to compare the modified double tail based comparator with the single tail comparator, the conventional double tail comparators and double tail comparator, all circuits have been simulated in 180 nm CMOS technology, VDD = 0.8v. Thus the power consumption modified double tail comparator is less than double tail comparator and delay also reduced.

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