

FPGA Implementation of Nano-Ram Circuit Using Reversible Gates in Reversible Mac Unit

Aathilakshmi S¹

P.G. Student, Department of VLSI DESIGN, Kalaignar Karunanidhi Institute of Technology, Coimbatore, India¹

ABSTRACT: The multiplication and accumulation are the vital operations involved in almost all the Digital Signal Processing applications. Consequently, there is a demand for high speed processors having dedicated hardware to enhance the speed with which these multiplications and accumulations are performed. In the present conventional circuits, the multiply accumulate unit multiplies the two operands, adds the product to the previously accumulated result and stores back the new result in the accumulator in a single clock. Using reversible logic the implementation of digital circuits is gaining popularity with the arrival of quantum computing and reversible logic. In this paper, a novel reversible multiply accumulate unit is proposed. The comparison of various possible implementations of the reversible multiply accumulate unit in terms of gate count, quantum cost, constant inputs and number of garbage outputs is carried out. In this thesis, a novel reversible MAC unit is proposed. The reversible multiplier is implemented by the combination of reversible half adders, full adders and Peres gates. The reversible adder is used as the adder and the reversible accumulator is designed using the reversible shift register. A reversible MAC unit is also built and compared with other possible implementations unit in terms of gate count, quantum cost, constant input and garbage output of the circuit.

KEYWORDS: Reversible Multiply Accumulate Unit, Digital Signal Processors, Reversible Shift Register, Reversible Adder, Reversible Multiplier, Quantum Cost.

I. INTRODUCTION

In irreversible logic, according to Landauer's [1] research, heat dissipation of $kT \ln 2$ joules takes place on erasing a bit (k is the Boltzmann's constant and T is the absolute temperature of environment). A one to one mapping exists between the input and output vectors in reversible logic and according to Bennett [2], the operations performed in reversible logic will not dissipate $kT \ln 2$ joules of heat energy. Reversible logic gates constitute reversible logic circuits and their major application can be seen in quantum computing. Each quantum logic gate performs an elementary unitary operation on one, two or more two-state quantum system called qubits. In the design of reversible circuits, fan-out and loops are not permitted. From the point of view of reversible circuit design, there are three parameters for determining the complexity and performance of circuits: Quantum cost (QC): The number of 1×1 or 2×2 reversible gates which are used in circuit. Constant inputs (CIs): the inputs which are used as control inputs and are connected to logical zero or one. Garbage outputs (GOs): The number of dummy (unused) outputs which are made to appear in order to make the circuit reversible. Gate count: The number of 1×1 or 2×2 reversible gates which are used in the design. A reversible circuit designer always looks to optimize on these four parameters. All Digital Signal Processing (DSP) algorithms extensively use Multiply-Accumulate (MAC) operation for high performance digital processing system. This operation eases the computation of convolution which is needed in filters, Fourier Transforms, etc. A MAC unit comprises of a multiplier, an adder and an accumulator. The multiplier multiplies the inputs and gives the result to the adder, which adds the multiplier result to the previously accumulated result.

Contribution: In this paper, a novel reversible MAC unit is proposed. The reversible multiplier is implemented by the combination of reversible half adders, full adders and Peres gates. The reversible adder is used as the adder and the reversible accumulator is designed using the reversible shift register. A reversible MAC unit is also built and compared with other possible implementations unit in terms of gate count, quantum cost, constant input and garbage output of the circuit.

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Organization: The rest of the paper is organized as follows: Section 2 explains the basics of reversible gates. The proposed design of reversible MAC unit is discussed in section 3. Section 4 shows the performance analysis of the proposed MAC unit and section 5 provides the conclusions.

II. BASIC REVERSIBLE GATES

The simplest reversible gate is NOT gate and is a 1*1 gate. Controlled NOT (CNOT) gate is an example for a 2*2 gate. There are many 3*3 reversible gates such as Fredkin (F), Toffoli (TG), Peres (PG) and TR gate. The quantum cost of 1*1 reversible gates is zero, and quantum cost of 2*2 reversible gates is one. Any reversible gate can be realized by using 1*1 NOT and 2*2 CNOT reversible gates, such as V, V+ (V is square root of NOT gate and V+ is its hermitian) and Feynman gate which is also known as CNOT gate. The V and V+ quantum gates have the property given in the Equations 1, 2 and 3.

$$V * V = \text{NOT} \dots\dots\dots (1)$$

$$V * V+ = V+ * V = I \dots\dots\dots (2)$$

$$V+ * V+ = \text{NOT} \dots\dots\dots (3)$$

The quantum cost of a design using reversible logic is calculated by counting the number of V, V+ and CNOT gates.

A. Fredkin Gate

Reversible 3*3 gate maps inputs (A, B, C) to outputs (P = A, Q = A1B + AC, R = AB + A1C) having quantum cost of five and it requires two dotted rectangles, is equivalent to a 2*2 Feynman gate with quantum cost of each dotted rectangle is one, one V and two CNOT gates.

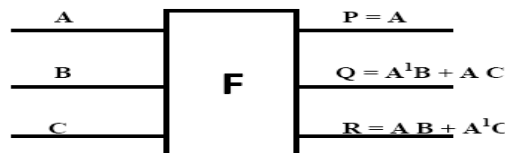


Fig.1. Fredkin gate

Fredkin gate and its quantum implementations are shown in fig 1 respectively.

B. Peres Gate

The three inputs and three outputs i.e., 3*3 Reversible gate having inputs (A, B, C) mapping to outputs (P = A, Q = AB, R = (A.B)C). Since it requires two V+, one V and one CNOT gate, it has the quantum cost of four. The Peres gate and its quantum implementation are as shown in the figure 2 respectively.

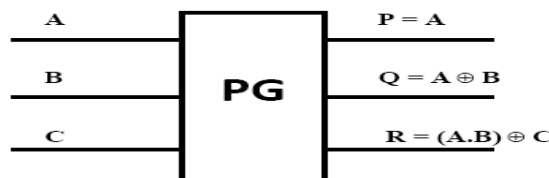


Fig. 2. Peres gate

C. Double Peres Gate

The 4x4 reversible gate with four inputs and four outputs. The inputs (A, B, C, D) mapped to (P = A, Q = A.B, R = A&B D, S = (A.B) D.AB.C) is as shown in fig 3. The DPG has a quantum cost of six as it requires three V, one V+ and two CNOT gates and its implementation is as shown in figure 3.

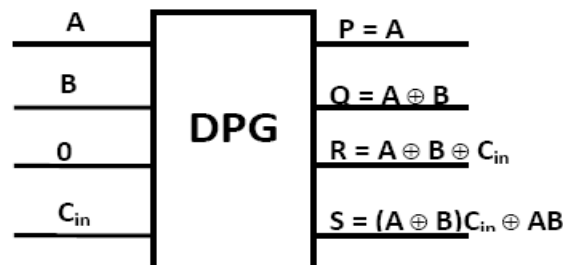


Fig. 3. DPG as full adder

III. PROPOSED MAC DESIGN

A. Multiplier

A reversible 4x4 multiplier circuit has two parts: Partial Product Generation (PPG) circuit and Multi-Operand Addition (MOA) circuit. The details of these two parts are discussed in the following sections.

B. Partial Product Generation

The basic operation of 4x4 parallel multiplier circuit is depicted in figure 4. It consists of sixteen partial products of the form $X_i.Y_i$, where i vary between 0 and 3.

The PPG circuit using Peres and RAM gates is as shown in figure 4. Here sixteen PG gates are used to generate sixteen partial products as shown in figure 4. The RAM gate is used as a copying gate, for each X_i input four copies are generated and totally sixteen input signals are copied using four RAM gates as shown in figure 4.

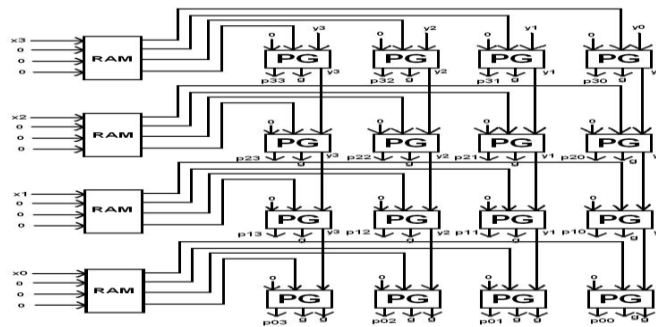


Fig. 4. Proposed reversible partial products generation circuit using Peres and RAM gates

C. Multi-Operand Addition

The addition of the partial products using DPG and PG gates is as shown in figure 5. The basic cells for such a multiplier is full adder using DPG with three inputs and one constant input, two garbage outputs and half adder using PG with two inputs and one constant input, one garbage output.

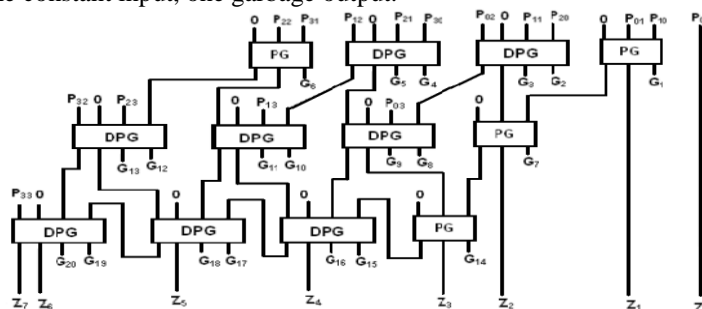


Fig. 5. Reversible multi-operand addition circuit

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The proposed reversible multiplier circuit uses eight DPG gates, four PG gates, sixteen PG gates for partial product generation and four RAM gates for fan-out creation. It is possible use FG gate as copying circuit, but it requires twelve FGs instead of four RAM gates and by using RAM gate the hardware complexity and garbage outputs are reduced.

D. Adder

i) Half Adder/Subtractor

Reversible half Adder/Subtractor–Design III is implemented with three Reversible gates of which two are FG gates each having Quantum cost of one and a PG gate with Quantum cost four is as shown in the figure 6. The numbers of Garbage outputs is two i.e., g1 and g2, Garbage inputs are one denoted by logical zero and Quantum Cost is six.

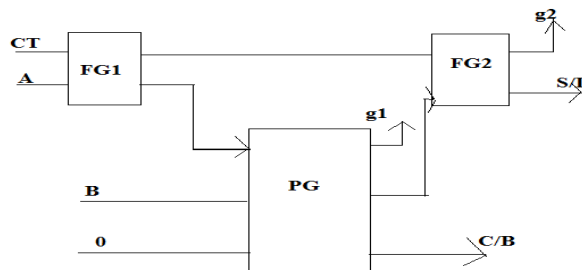


Fig. 6. Reversible half adder/subtractor–Design III

ii) Full Adder/Subtractor

The Reversible Full Adder/Subtractor Design III consists of two FG, two PG gates, and their interconnections are shown in the figure 7. The three inputs are A, B, and Cin, The outputs are S/D and C/B. For Ctrl value zero the circuit performs addition and Subtraction for Ctrl value one. The numbers of Garbage inputs are 1 represented by logical zero. The Garbage outputs are 3 represented by g1 to g3.

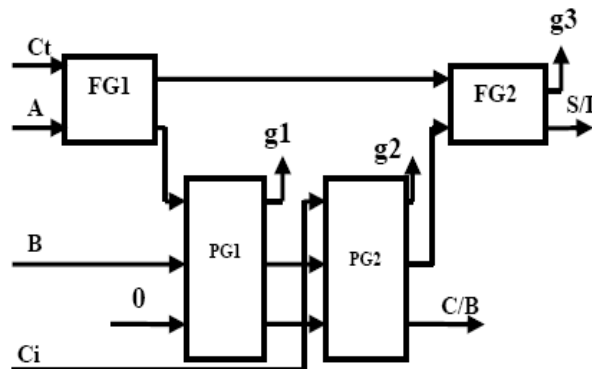


Fig. 7. Reversible full adder/subtractor–Design III

The Quantum Cost for the design is 10. A Quantum Cost advantage of 11 is obtained when compared to Adder/Subtractor Design I and of 4 when compared to Adder/Subtractor Design II. Quantum Cost advantage is due to the realization of Arithmetic blocks using two PG gates as against two F and one TR gate for Design I and two TR gates for Design II.

E.Eight-bit Parallel Binary Adder/Subtractor

The Half and Full Adder/Subtractor Design I, Design II and Design III are used to construct Reversible eight-bit Parallel Binary Adder/Subtractor is shown in the figure 8. The ctrl input is used to differentiate eight-bit addition and subtraction functions. The two eight-bit binary numbers are A0 to A7 and B0 to B7. Carry/Borrow is obtained after

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Addition/Subtraction is represented by C_B1 to C_B7. The outputs Sum/Difference and Carry are shown as S_D0 to S_D7 and C_B8 respectively. The implementation requires seven Full Adder/Subtractor units and one half Adder/Subtractor units in which first stage is half Adder/Subtractor.

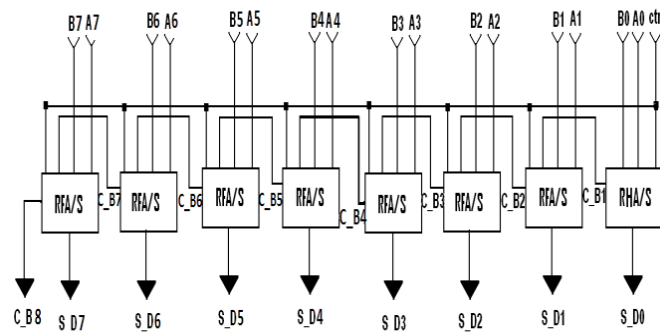


Fig .8. Reversible Eight-bit parallel Binary Full Adder/Subtractor

F. Accumulator

Accumulator is one of the most extensively used functional devices in digital systems. A register consists of a group of flip-flops connected together so that the information bits can be stored within a digital system so that they can be used later during computing process. Shift register is a register in which information can be shifted bit wise depending on the clock signal. This section proposes Parallel-In-Parallel-Out (PIPO) shift register. The designs are proposed using the basic reversible gates considering the previous designs, we are aiming on reducing the quantum cost of each designs.

G. Reversible D-Latch

The D-latch can be realized using Fredkin gate as shown in figure 9. The quantum cost of the design shown is five; number of garbage outputs is one. The propagation delay of the design is 5Δ .

H. Reversible D Flip-Flop

A flip-flop is a bi-stable electronic circuit that has two stable states and one-bit memory device. The characteristic equation of D flip-flop is $Q^+ = D \cdot Clk + \bar{Q} \cdot Clk1$ which can be mapped onto the Fredkin gates as shown in figure 9.

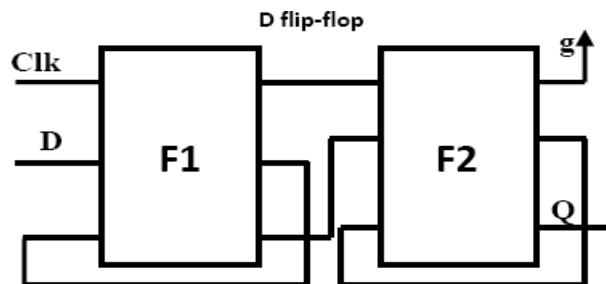


Fig. 9. Reversible D Flip-Flop

The Feynman gate produces the toggled output of the input and the second Feynman again toggles the output of the first Feynman, thus we obtain the input at the output with a delay. The constant input '1' helps the second Feynman gate to toggle the input. The output 'g' represents the garbage output and Q is the actual output.

I. Reversible eight-bit PIPO Shift Register

In this shift register, the inputs are fed simultaneously into the flip-flops and we get the output when we apply clock pulse. Here eight D flip-flops are used for the design. The PIPO shift register combines the functions of the Parallel-In-Serial-Out (PISO) and Serial-In-Parallel-Out (SIPO) shift registers. When there is a clock signal, the inputs D0, D1...D7 are loaded parallel into the register coincident. The outputs Q0, Q1...Q7 are available in parallel at the Q

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output of the flip-flops. The quantum cost of D flip-flop is ten, therefore the quantum cost of eight-bit shift register if eighty without fan-out creation and is eighty seven with fan-out creation.

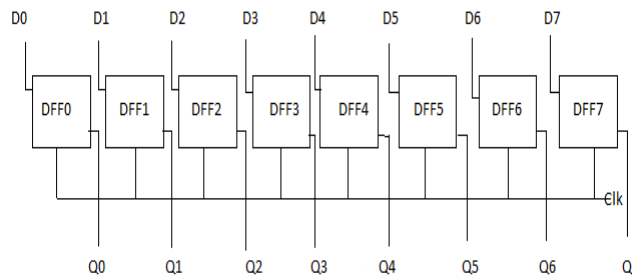


Fig. 10. Reversible 8-bit PIPO Shift Register

J. Multiply Accumulate (MAC) Unit

This section describes four-bit reversible Multiply Accumulate Unit shown in figure 11. A MAC unit is used to perform the multiplication and accumulator operations together to avoid unnecessary overhead on the processor in terms of processing time and the on-chip memory requirements. This is extensively used in Digital Signal Processing algorithms for high performance digital processing system. The proposed reversible MAC unit comprises of a four-bit reversible Multiplier, eight-bit reversible Adder and eight-bit reversible Accumulator register. The Multiplier multiplies the inputs and gives the result to the adder, which adds the multiplier result to the previously accumulated result. The reversible Accumulator is designed using the reversible eight-bit register.

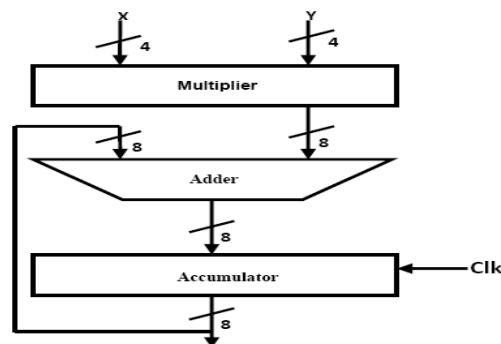


Fig. 11. Reversible 4-bit multiply-accumulate unit

The four-bit inputs X and Y are applied to the multiplier unit which results in eight-bit product. The product is applied to eight-bit adder unit which adds the previous result stored in accumulator as well as the present out of the multiplier. Again the result of the adder is stored back into the accumulator and this process will repeat till the last bits. In digital signal processing, Discrete Fourier Transform (DFT) computation is most widely used where number of multiplications and additions should be performed. Most of the power consumption occurs during data manipulation. Therefore to minimize the power consumption DFT computation can be implemented by reversible MAC unit. The conventional multiply accumulate unit consists of multiplier and an accumulator register that contains the sum of the previous consecutive products. The function of the multiply accumulate unit is given by the following expression.

IV. SIMULATION RESULTS

A. Reversible Multiplier

Reversible multiplier is coded in Verilog and simulated using Modelsim simulator. Reversible gates such as PG, DPG and RAM gates are coded in Data flow style of modeling. The PPG generation circuit is coded in structural style of modeling and multi-operand addition circuit is constructed by using the reversible gates as the components for the structural model and the functionality is verified. The simulation result is given in figure 12. Here, a and b are four-bit inputs and z is the eight-bit multiplier output.

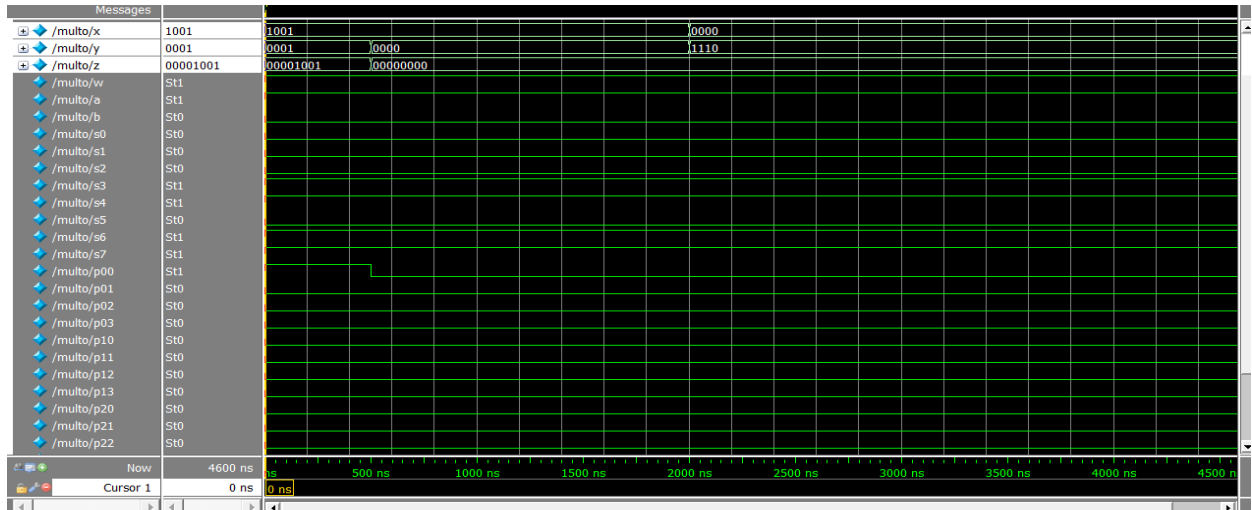


Fig. 12. Reversible PPG with Multi Operand Addition

The wave form shown in figure 12 is an example for reversible multiplier. In this, a and b are four-bit inputs and z is eight-bit product output. For a = “1001” and b = “0011” inputs the circuit performs multiplication function results in z = “00011011” output.

b.Reversible Adder

Reversible adder/subtractor designs types are coded in verilog and simulated using Modelsim simulator. Reversible gates such as FG and PG gates are coded in Dataflow style of modeling. Half and full adder/subtractors are coded in structural style of modeling. Half and full adder/subtractors are constructed by using the reversible gates as the components for the structural model and the functionality is verified. Results of simulation are given in figure 13 to 15 . In this design the control bit set to logic one indicates subtraction function and control bit set to logic zero indicates addition function. The output bits s_d and c_b shows the corresponding logic levels for the input bits a, b and c logic levels. The implementation uses seven full adder/subtractor units and one half adder/subtractor unit in which first stage is half adder/subtractor.

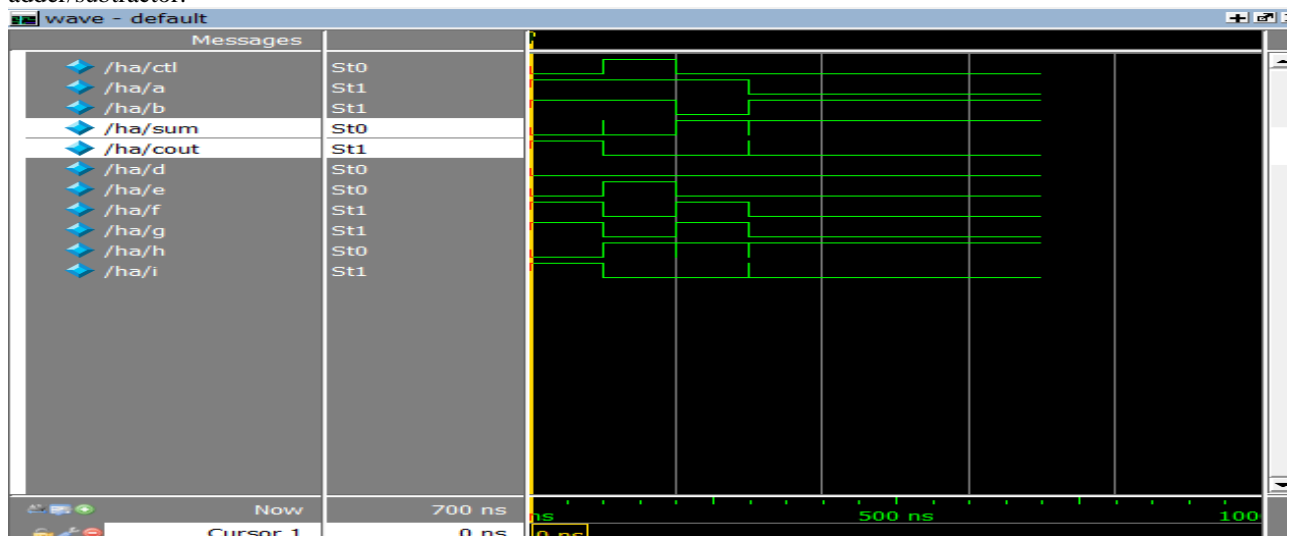


Fig. 13. Simulation Result of Reversible Half Adder/Subtractor

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The wave form shown in figure 13 is an example for half adder/subtractor and is same for all the three design types. In this a, b and Ctrl are input bits and s_d and c_b are sum/difference and carry/borrow outputs respectively. For a = '0', b = '1' and Ctrl = '1' inputs the circuit performs addition function results in s_d = '1' and c_b = '0' outputs.

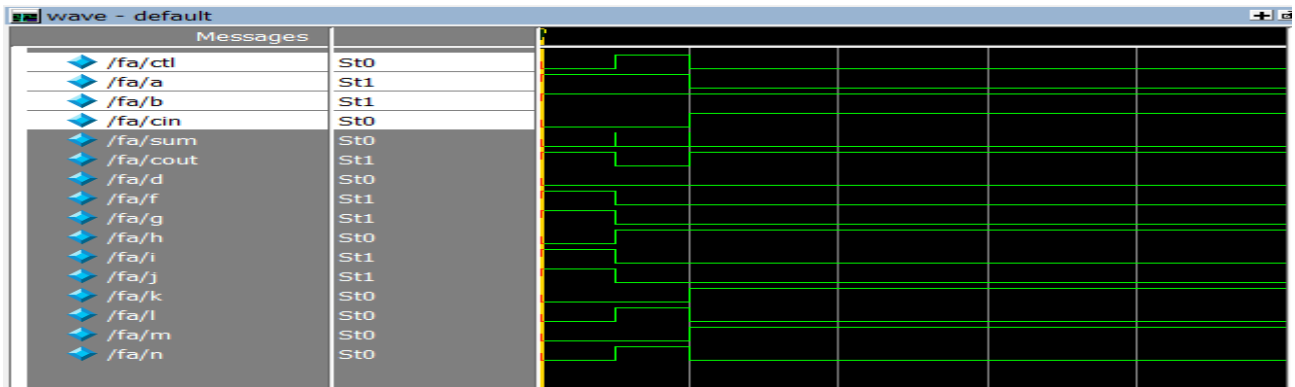


Fig. 14. Reversible Full Adder/Subtractor

The wave form shown in figure 14 is an example for full adder/subtractor and is same for all the three design types. In this a, b, c and Ctrl are input bits and s_d and c_b are sum/difference and carry/borrow outputs respectively. For a = '0', b = '1', c = '1' and Ctrl = '0' inputs the circuit performs subtraction function results in s_d = '0' and c_b = '1' outputs.

The wave form shown in figure 14 is an example for eight-bit parallel adder/subtractor and is same for all the three design types. In this a and b are eight-bit and Ctrl one-bit inputs and s_d and c_b8 are eight-bit sum/difference and one-bit carry/borrow outputs respectively. For a = "10101110", b = "01010111", c = '1' and Ctrl = '1' inputs the circuit performs addition function results in s_d = "00000101" and c_b8 = '1' outputs.

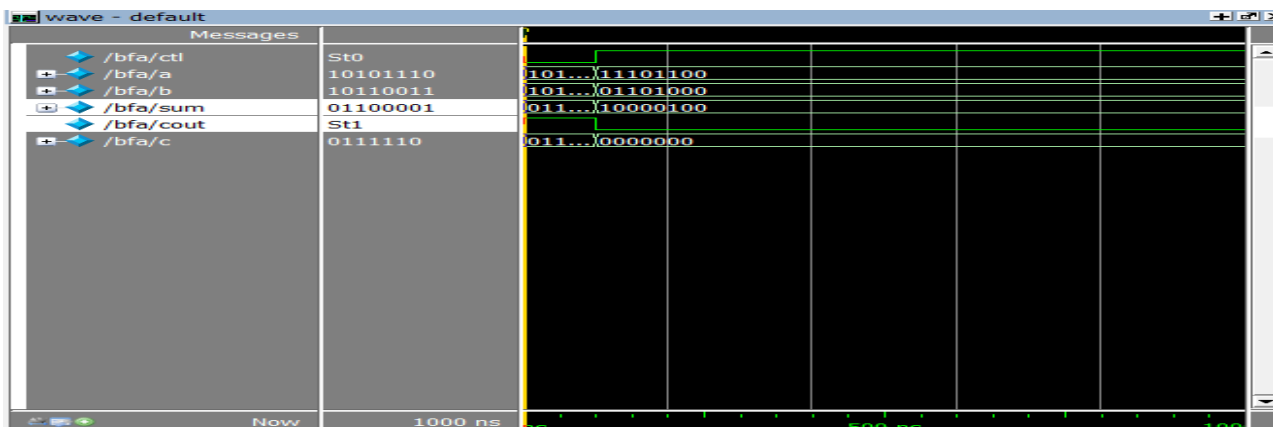


Fig. 15. Reversible 8-Bit Parallel Binary Full Adder/Subtractor

C. Reversible Accumulator

Reversible D flip-flop and shift register designs types are coded in Verilog and simulated using Modelsim simulator. Reversible gates such as FG and F gates are coded in dataflow style of modeling. The simulation results of D flip-flop and Accumulator are shown in the following figures. In the D flip-flop, whenever Clk signal is high the input D appears at the output Q and is shown in figure 16.

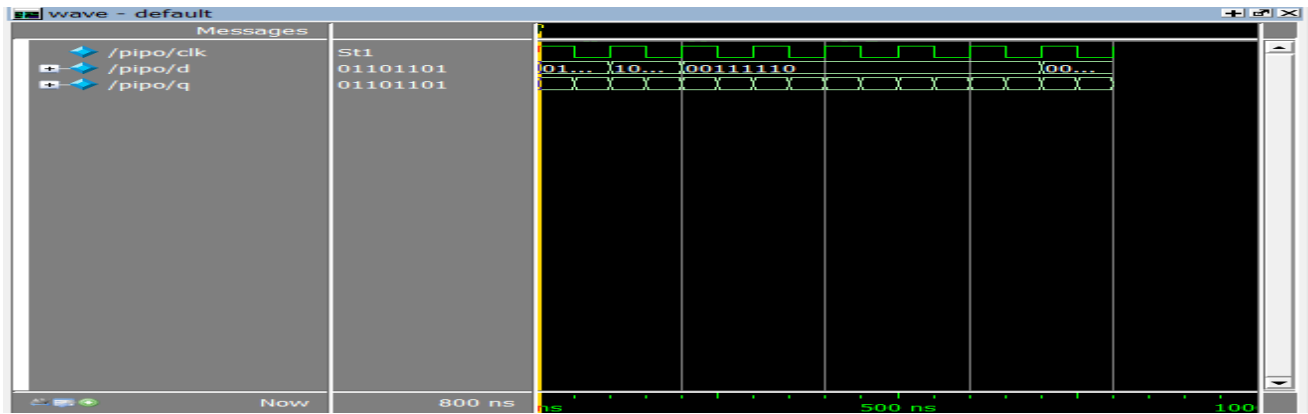


Fig. 16. Reversible 8-Bit PIPO Shift Register

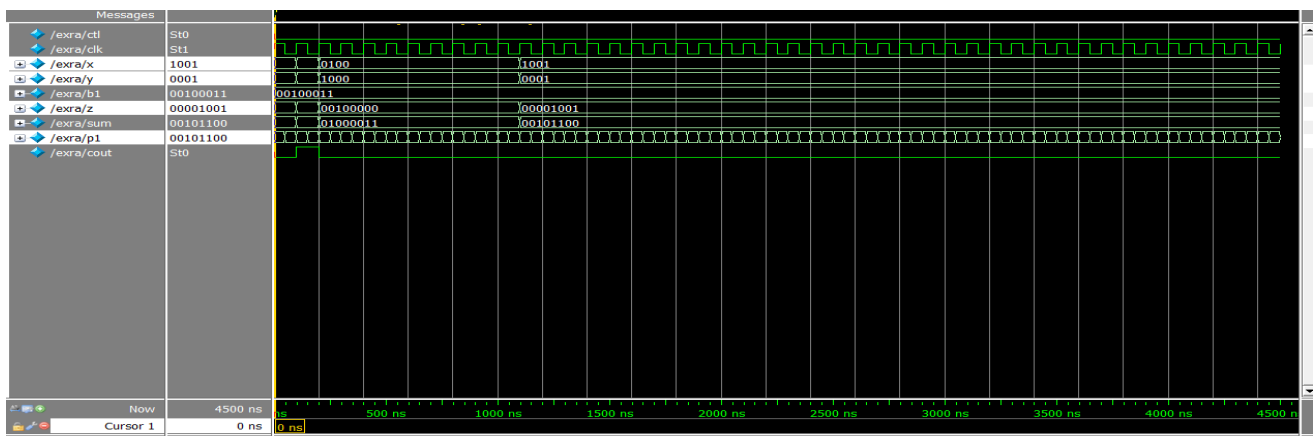


Fig. 17. Simulation Result of Reversible MAC UNIT

V. CONCLUSIONS

Nowadays reversible gates based NANO-RAM technique is used for Low Power applications, Quantum dot Cellular Automata, Computing Techniques. The proposed reversible design is utilized for efficiently designing Double Edge Triggered flip flop. Flip flops are most important memory elements used in several circuits like RAM, Logic blocks of FPGA. The proposed technique is compared with existing designs, minimized the garbage outputs and number of gates. The proposed design is highly optimized. Thus, the resulting sequential circuit is most efficient. Reversible gates are major building block of NANO-RAM. In proposed work sequential NANO-RAM circuits are designed by using reversible gates. The gate count is reduced from 60 to 30, garbage output is reduced from 17 to 9, and the power is reduced from 0.124mw to 47.135µw using Xilinx 8.1 and micro wind 3.1, DSCH 2 tool. In this paper design of reversible shift register and multiply-accumulate units are presented. The design is based on the useful properties of standard reversible gates suitable for multiplication, addition and accumulation. The 4-bit reversible multiply-accumulate unit is designed using 4-bit reversible multiplier circuit, 8-bit reversible adder/subtractor and 8-bit accumulator register. The key performance parameters like garbage outputs, number of reversible gates used, quantum cost and constant inputs are computed and analyzed for 4-bit multiply accumulate unit. It is observed that the performance parameter values are less in the proposed design compared to the existing approaches. Reversible circuits are an emerging technology with a promising application.

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