

VHDL in Low Power FSK Modulation and Demodulation

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ABSTRACT: In telecommunications and signal processing, frequency modulation (FM) is encoding of information on a carrier wave by varying the instantaneous frequency of the wave. Digital data can be encoded and transmitted via carrier wave by shifting the carrier's frequency among a predefined set of frequencies-a technique known as frequency-shift keying (FSK). The task of the PLL is to maintain coherence between the input (modulated) signal frequency, ω_i and the respective output frequency, ω_o via phase comparison. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. Frequency modulated input signal is assumed as a series of numerical values (digital signal) via 8-bit of analog to digital conversion (ADC) circuit. The FM Receiver gets the 8 bit signal every clock cycle and outputs the demodulated signal. The All Digital FM Receiver circuit is designed using VHDL, then simulated and synthesized using Modelsim SE 6 simulator and Xilinx ISE 6.3i, respectively.

KEYWORDS: Frequency modulation(FM), Frequency shift keying(FSK), Phase locked loop(PLL), VHDL.

I.INTRODUCTION

Frequency shift keying (FSK) is the most common form of digital modulation in the high-frequency radio spectrum, and has important applications in telephone circuits. Binary FSK (usually referred to simply as FSK) is a modulation scheme typically used to digital information between digital equipment such as tele printers and computers. The data are transmitted by shifting the frequency of a continuous carrier in a binary manner to one or the other of two discrete frequencies. One frequency is designated as the "mark" frequency and the other as the "space" frequency. The mark and space correspond to binary one and zero, respectively. By convention, mark corresponds to the higher radio frequency. Figure 1 shows the relationship between the data and the transmitted signal.

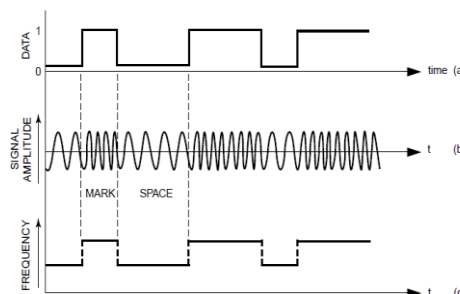


Fig 1. Fsk modulation. (a) Binary data (b) frequency modulates the carrier to produce the fsk signal (c) which has the frequency characteristic

The most commonly used signal parameters for describing an FSK signal are shown in Figure 2. The minimum duration of a mark or space condition is called the element length. Typical values for element length are between 5 and 22 milliseconds, but element lengths of less than 1 microsecond and greater than 1 second have been used. Bandwidth constraints in telephone channels and signal propagation considerations in HF channels generally require the element

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length to be greater than 0.5 millisecond. An alternate way of specifying element length is in terms of the keying speed. The keying speed in “bauds” is equal to the inverse of the element length in seconds. For example, an element length of 20 milliseconds (.02 seconds) is equivalent to a 50-baud keying speed. Frequency measurements of the FSK signal are usually stated in terms of “shift” and center frequency. The shift is the frequency difference between the mark and space frequencies. Shifts are usually in the range of 50 to 1000 Hertz. The nominal center frequency is halfway between the mark and space frequencies. Occasionally the FM term “deviation” is used. The deviation is equal to the absolute value of the difference between the center frequency and the mark or space frequencies. The deviation is also equal, numerically, to one-half of the shift. FSK can be transmitted coherently or non coherently. Coherency implies that the phase of each mark or space tone has a fixed phase relationship with respect to a reference. This is similar to generating an FSK signal by switching between two fixed-frequency oscillators to produce the mark and space frequencies. While this method is sometimes used, the constraint that transitions from mark to space and vice versa must be phase continuous (“glitch” free) requires that the shift and keying rate be interrelated. A synchronous FSK signal which has a shift in Hertz equal to an exact integral multiple ($n = 1, 2, \dots$) of the keying rate in bauds, is the most common form of coherent FSK. Coherent FSK is capable of superior error performance but non coherent FSK is simpler to generate and is used for the majority of FSK transmissions. Noncoherent FSK has no special phase relationship between consecutive elements, and, in general, the phase varies randomly.

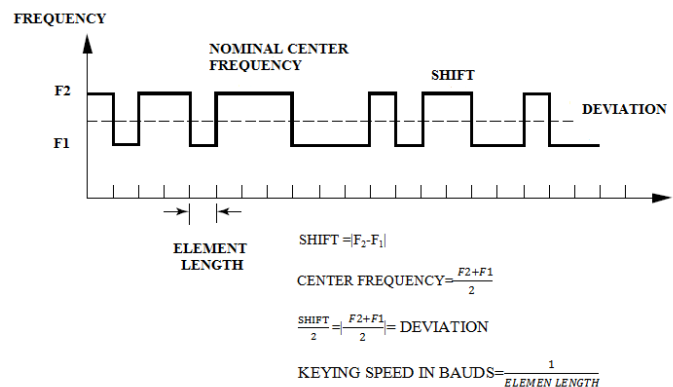


Fig 2. FSK parameters

Frequency modulation has been in ubiquitous use for communication media such as radio broadcast FM, TV audio, VHS Hi Fi, laser disc, and even digital wireless in the form of frequency shift keying FSK. Many efforts have been made to integrate an FM receiver on a single chip using various architectures, but the performance has been limited by the analog signal-processing accuracy. The main issue of integrating an FM demodulator on a chip is how to accurately discriminate a small frequency deviation of the FM signal from its center frequency. Most FM demodulators use either the Foster-Seeley method or phase-locked loops (PLL) [1]. The PLL behaves as a narrow-band tracking filter, with its loop-filter output exhibiting a frequency discriminating characteristic. It is readily implementable in integrated forms, but the linearity of the voltage-controlled oscillator VCO affects the overall linearity. Hence, Digital PLL's can overcome some of the weaknesses of analog PLL's. Also, the digital tangent method can compute frequency from the ratio of in-phase and quadrature (I-Q) signals. These digital methods for wide dynamic range IF processing and accurate frequency discrimination require either extensive numerical processing or large read-only memory (ROM) lookup tables. Frequency-shift keying (FSK) is a frequency modulation scheme in which digital information is transmitted through discrete frequency changes of a carrier wave. This application report discusses logic level implementation of binary FSK (BFSK) modulator and demodulator using a phase-locked loop PLL. A phase-locked loop or phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. It is widely used in modern wireless communication system owing to high frequency resolution and fast settling time. On the other hand, it also encounters some challenges. PLL frequency synthesizer is a complex mixed-signal system, and there is no stable periodic solution. Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications [1],[2]. They can be used to demodulate a signal,

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recover a signal from a noisy communication channel & generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Phase locked loop can be implemented in synchronous condition where after a definite time interval the PLL is locked .

Phase locked loop normally consists of voltage controlled oscillator, phase detector or comparator, low pass filter. The oscillator generates a periodic signal. The phase detector compares the phase of that signal with the phase of the input periodic signal and adjusts the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison is called a feedback loop as the output is 'fed back' toward the input forming a loop .

Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. Consequently, in addition to synchronizing signals, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. These properties are used for computer clock synchronization, demodulation, and frequency synthesis, respectively.

II.CIRCUIT DESIGN

The design of the All Digital FM Receiver circuit in this project uses Phase Locked Loop (PLL) as the main core. The task of the PLL is to maintain coherence between the input (modulated) signal frequency, ω_1 and the respective output frequency, ω_0 via phase comparison. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked.

Frequency modulated input signal is assumed as a series of numerical values (digital signal) via 8-bit of analog to digital conversion (ADC) circuit. The FM Receiver gets the 8 bit signal every clock cycle and outputs the demodulated signal. The block diagram of FSK modulation is shown below.

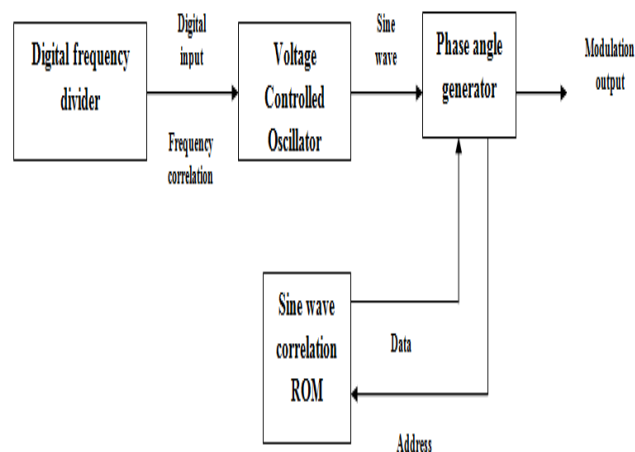


Fig 3. FSK modulation

Signal generator generates required input signal. The signal is given to numerical controlled oscillator which is nothing but the voltage controlled oscillator.

A. Numerical Controlled Oscillator (Nco)

NCO is a digital signal generator which creates a synchronous (i.e. clocked), discrete-time, discrete-valued representation of a waveform, usually sinusoidal.^[1] NCOs are often used in conjunction with a digital-to-analog

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converter(DAC) at the output to create a direct digital synthesizer (DDS).^[3] Numerically controlled oscillators offer several advantages over other types of oscillators in terms of agility, accuracy, stability and reliability.^[2] NCOs are used in many communications systems including digital up/down converters used in 3G wireless and software radio systems, digital PLLs, radar systems, drivers for optical or acoustic transmissions, and multilevel FSK/PSK modulators/demodulators [7]. An NCO generally consists of two parts:

- A phase accumulator (PA), which adds to the value held at its output a frequency control value at each clock sample.
- A phase-to-amplitude converter (PAC), which uses the phase accumulator output word (phase word) usually as an index into a waveform look-up table (LUT) to provide a corresponding amplitude sample. Sometimes interpolation is used with the look-up table to provide better accuracy and reduce phase error noise. Other methods of converting phase to amplitude, including mathematical algorithms such as power series can be used, particularly in a software NCO.

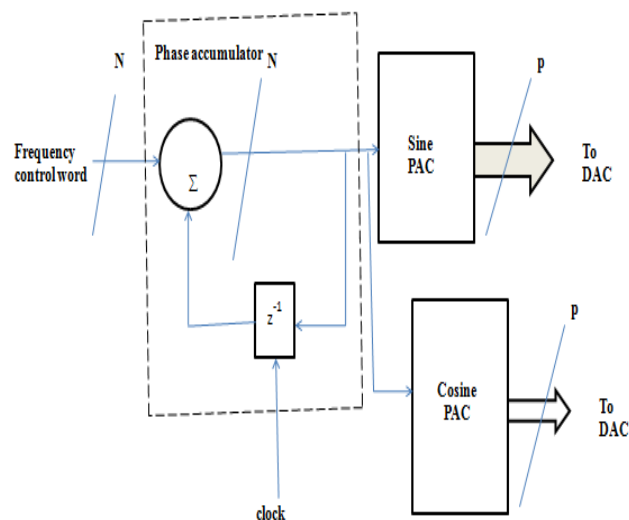


Fig 4. Numerically controlled oscillator with quadrature output

When clocked, the phase accumulator (PA) creates a modulo- 2^N sawtooth waveform which is then converted by the phase-to-amplitude converter (PAC) to a sampled sinusoid, where N is the number of bits carried in the phase accumulator. N sets the NCO frequency resolution and is normally much larger than the number of bits defining the memory space of the PAC look-up table. If the PAC capacity is 2^M , the PA output word must be truncated to M bits as shown in Figure 1. However, the truncated bits can be used for interpolation. The truncation of the phase output word does not affect the frequency accuracy but produces a time-varying periodic phase error which is a primary source of spurious products. Another spurious product generation mechanism is finite word length effects of the PAC output (amplitude) word.

The frequency accuracy relative to the clock frequency is limited only by the precision of the arithmetic used to compute the phase. NCOs are phase- and frequency-agile, and can be trivially modified to produce a phase-modulated or frequency-modulated output by summation at the appropriate node, or provide quadrature outputs. Sine correlation is a method to generate sine wave based on sine table.

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B. Phase Detector

The Phase Detector (PD) detects phase error between input signal and output signal from NCO. This operation employs a multiplier module and a register as shown in the figure

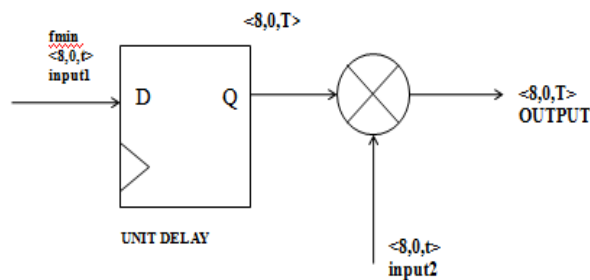


Fig 5. Phase detector

III. SIMULATION RESULTS

The system clock frequency and sampling frequency can be taken up to 100MHz. FM modulation is $\pm 10\text{KHz}$ at a 1MHz center frequency. In this simulation the system clock frequency is 100MHz. The modulation is just $\pm 1.0\%$ of the 1MHz carrier frequency. The simulation results are shown below. Internal architectures of NCO module, phase angle generators are given. FM modulation output waveform is obtained. In the modulated waveform positive and negative deviations are shown for 10KHz.

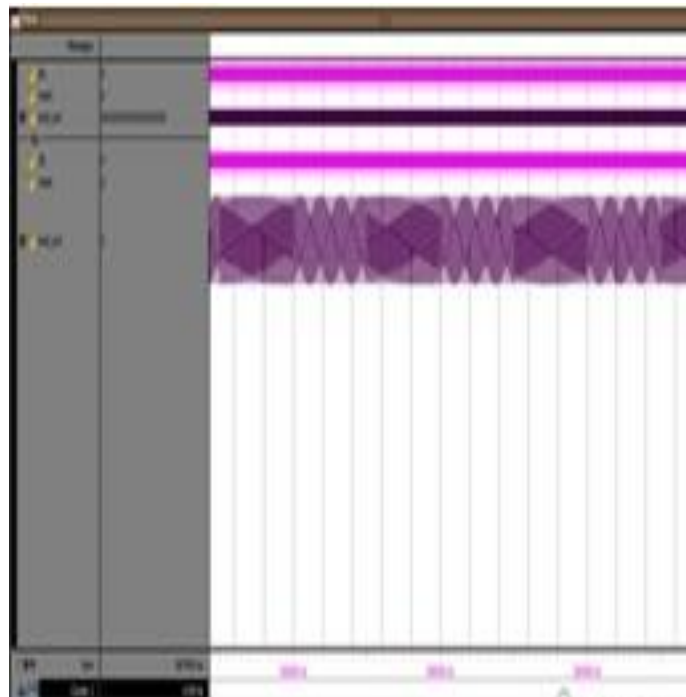


Fig 6. FSK modulation

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IV. CONCLUSION

FSK modulated waveform is obtained with frequency modulation techniques. Phase locked loop and voltage controlled oscillators are the important parameters. The above modulation technique can be implemented in field programmable gate array(FPGA) and can be synthesized using Xilinx. Positive and negative deviations of FSK can be achieved.

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