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High Speed and Pre-Charging Sense Amplifier for CMOS Logic Circuits on Resistive Switching Memories

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ABSTRACT: The RS-NVL architecture consists of the complementary RS-NVMs. The design of RS-NVL architecture using compact models of STT-MRAM and OxRRAM. It allows the logic-in-memory architecture. They can be easily extended to different RS-NVM or memristor technologies. This integration allows the elimination of dynamic power dedicated for data transfer between logic units and memory array. Special design techniques and strategies are proposed to optimize the structure according to different resistive characteristics of NVMs. To validate a non-volatile full-adder (NVFA) with two types of NVMs: STT-MRAM and OxRRAM. The RS-NVL architecture consists of the complementary RS-NVMs. the design of RS-NVL architecture using compact models of STT-MRAM and OxRRAM. It allows the logic-in-memory architecture. They can be easily extended to different RS-NVM. This integration allows the elimination of dynamic power dedicated for data transfer between logic units and memory array.

KEYWORDS: Complementary cells, low-power design, non-volatile memory, resistive switching, synchronous logic gate.

I.INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC makers add all of these into one chip. Modern computing systems suffer from rising power dissipation including both static and dynamic parts [1], [2]. The static power is driven by the high leakage currents, which increase exponentially with the minimization of fabrication node. The dynamic power is induced mainly by the data transfer between memory chip and logic units, which requires more power (i.e., 1 pJ/mm/bit) than the transistor switching (e.g., 1 fJ/bit), and then imposes the speed bottleneck to adapt the current cooling systems [2].

Resistive switching refers to the physical phenomena where a dielectric suddenly changes resistance under the action of a strong electric field or current. The change of resistance is non-volatile and reversible. Typical resistive switching systems are capacitor like devices, where the electrode is an ordinary metal and the dielectric a transition metal oxide. An interesting application of resistive switching is the fabrication of novel non-volatile resistive random-access memories (RRAM). This effect is also at the base of the behavior of the so called memristor devices and xeromorphic memories. Resistive switching is the physical phenomenon that consists on the sudden and non-volatile change of the resistance due to the application of electric stress, typically voltage or current pulsing.

Even though these emerging RS-NVMs are derived from different physics, they hold many common features. For instance, they are two-terminal nanoscale devices and their resistances vary to present '0' and '1' NV states. Benefiting from these features, a number of innovative hybrid RS-NVM/CMOS circuit have been designed in the last few years

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such as NV look-up-table (NV-LUT) [12], NV Flip-Flop (NVFF) [13]–[15] and NV Full Adder (NVFA) [16]–[19]. They show interesting performance in terms of power, area and speed. However there is no general design rule so far for these hybrid circuits and it is difficult to extend them for all types of RS-NVMs. Moreover, most of these circuits suffer from critical limits. For instance, [16]–[18] use magnetic fields or capacitance, which cannot be used in deep submicron ICs. The dynamic power is induced mainly by the data transfer between memory chip and logic units, which requires more power than the transistor switching, and then imposes the speed bottleneck to adapt the current cooling systems. MRAM cells integrate a magnetic tunnel junction (MTJ) consisting of a thin insulating barrier separating two ferromagnetic (FM) layers. OxRRAM modeling approach, deriving from a unipolar model relies on electric field-induced migration of oxygen vacancies within the switching layer.

II. GENERAL SYNCHRONOUS RS-NVL STRUCTURE

This general structure or algorithm of synchronous logic gate based on STT-MRAM was initialized and named “logic-in-memory” architecture. It allows a novel combination between logic unit and memory cell beyond Von-Neumann architecture. The data movement distance becomes much shorter, and this promises lower power and faster speed. In this paper, we extend this structure from STT-MRAM to universal RS-NVMs. According to their different resistance characteristics, a detailed theoretical analysis will be introduced for structure optimization. The general structure is mainly composed of three parts: a fast speed dynamical-mode sense amplifier (SA), volatile or fragile *logic* data and non-volatile or secure *analog* data as shown in Fig. 4. In order to perform the logic function, a SA is firstly required as the RS-NVM cell with analog data is integrated directly with the logic circuit. This SA should be fast, robust and consume low power to ensure the computing purpose of this structure.

Different from the SA for memory chip, it is impossible to embed error correction circuits (ECC) and to share the circuit for multi-cells. Thereby we use here the pre-charge sense amplifier (PCSA), which showed high performance in terms of reliability, power and speed. There is no capacitance in this structure, which allows better minimization in advanced fabrication node.

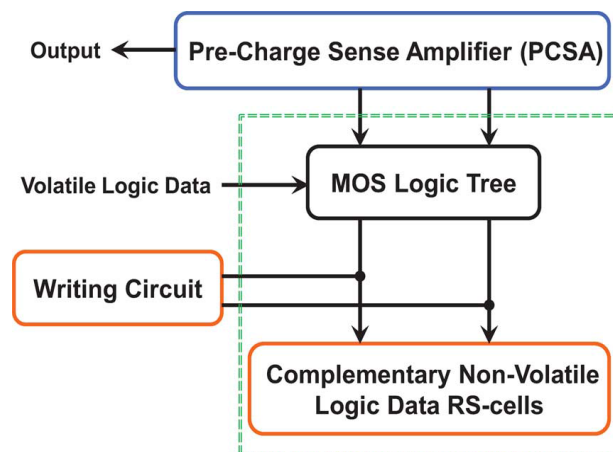


Fig.1 Logic gates composed of PCSA, MOS logic tree and RS-NVMs

PCSA consists of a pre-charge sub circuit ($MP2-3$), a discharge sub-circuit ($MN2$) and a pair of inverters ($MN0-1$ and $MP0-1$), which act as an amplifier. It operates in 2 phases. During the first phase, “CLK” is ‘0’ and the outputs (“ Qm ” and “ $\bar{Q}m$ ”) are pulled-up to “CLK” or logic ‘1’ through $MP2-3$ while $MN2$ remains off. During the second phase, “CLK” becomes ‘1’, $MP2-3$ are turned off and $MN2$ on. As RS-NVM0 and RS-NVM1 are in complementary states (one is set to and the other to discharge currents are different in the two branches).

The lower resistance branch will be pulled-down to reach the threshold voltage of transistor ($MP1$ or $MP2$) more quickly, at the same time, the other branch will be pulled up to or logic ‘1’ and this low-resistance branch will continue

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to drop to G_{nd} or logic '0'. The volatile input data is injected in the structure through MOS tree (i.e., series connection of NMOS transistors). The *logic* data control the gate of the NMOS transistor setting their states to or . Resistance value of NMOS transistors contributes then like that of the RS-NVMs to the overall branch resistance. The non-volatile input data are stored in a pair of RS-NVM cells always in opposite state to ensure the necessary sensing speed and reliability (e.g., 100 ps) .

Thanks to the proximate position of the complementary RS-NVMs, this structure suffers from low mismatch variation, which is one of the most important limitations for large capacity RS-NVM chips in advanced technology node The RS-NVM cells are serially connected with a common central point. To program them, bi-directional write circuit is required. It is composed of pass transistors, which are connected respectively to the bottom electrode (BE) and the top electrode (TE) of RS-NVM cells and to the common point.

This structure allows the same storage state cases for the RS-NVM cells to be avoided, and then provides hardness against programming errors. It is important to note that the control signals should not be activated at the same time. The control of these signals can be optimized further to improve the power efficiency and reliability of RS-NVL. For instance, "self-enable" write circuits for RS-NVMs were presented recently, which detect the state difference between input data and stored data before the writing enable operation. Different from many emerging logic solutions based on RS-NVMs, RS-NVL can implement all basic logic functions. This advantage allows a relatively complex function such as full-adder to be built up easily. The following subsection introduces the design rules for different resistive characteristics of RS-NVMs, which allow the designers to find the optimal solution regarding RS-NVM features Which is so tremendous that it is adapted to nearly all the RS-NVM cells .

III. DESIGN CONSIDERATION AND THEORETICAL ANALYSIS

As mentioned above, outputs " Q_m " and detect the logic result through the discharging currents of PCSA. These currents depend on the volatile data in the MOS logic tree and on the NV data stored in the complementary RS-NVMs. The resistance configuration of both types of data plays then a significant role to ensure the correct operation of RS-NVLs. In the following, we will give two examples, a 2-input "AND" and a 2-input "XOR" logic gates, to analyze the impact of the resistance configuration on logic operations.

The left branch (LB) represents the output through a series connection of one NMOS transistor and one RS-NVM cell. The right branch of PCSA represents the output " Q_m " through three parallel sub branches (RB0-RB2) or "OR" logic. This design strategy of RS-NVL is similar to that of CMOS logic. For this structure, any resistive level of RS-NVMs allows correct "AND" function. However the numerous NMOS transistors and RS-NVMs lead to large die area. In particular, it needs at least two writing circuits for complementary data storage. In order to optimize the design, we can benefit from the resistance configuration of MOS and RS-NVM. For the advanced MOS technology, k and G . Thereby the is much larger than of RS-NVMs and it determines directly the whole resistance of series connection

We keep RB1 to make RS-NVM cells of the right branch complementary to that of the left branch. The structure can be further optimized to one RS-NVM for the right branch with the condition that is much larger than, and it meets the "logic-in-memory" architecture. Whatever the logic value of only one RS-NVM is useful to change " Q_m ". We call this structure "optimizedstructure-1". exhibits the truth table of optimized structure and the resistance configuration to allow correct "AND" logic function. and present data '0' for NMOS transistor and RS-NVM, on the contrary, and present data '1'. and are respectively the resistance of the left and right branches of PCSA. When the output on the contrary, We can find that there are two uncertain cases.

Depending on the values of and the relationship between and is different, driving the result to get correct values or not. Resistance conditions to identify the uncertain cases for the structure. It demonstrates that the difference between and should be in the range to ensure "AND" logic function. This range is approximately, 10 G for advanced MOS nodes, Transient simulations have been performed to confirm this conclusion by using compact models of RS-NVM and CMOS 40 nm design-kit STT-MRAM (in the k range). The circuit performs correctly the "AND" logic whatever the input data of Additionally, the parallel NMOS transistors driven by respectively data can be deleted considering the

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logic design strategy. From analog point of view, whatever the value of the resistance of the right branch will always be the same. We can then obtain an ultra-compact structure where there is only one transistor for the MOS tree.

We call this structure “optimized structure-2”. However the resistance of the right branch changes after this ultimate optimization, we need to re-check the resistance configuration. We can find that there are also two uncertain cases. It is important to note that the resistance condition is very different between the two optimized structures 1 and 2. should vary in the range to ensure the “AND” logic for the structure-2, which is much more rigorous than the first one. This makes it unsuitable for all the RS-NVMs. As mentioned above, we performed transient simulations to validate the optimized structure-2 by using two RS-NVMs. We find that there is error for STT-MRAM as the data is respectively ‘1’ and ‘1’. This is caused by the low value of STT-MRAM, which is out of the acceptable range for the structure-2. However, similar simulations with 40 nm CMOS and OxRRAM compact model.

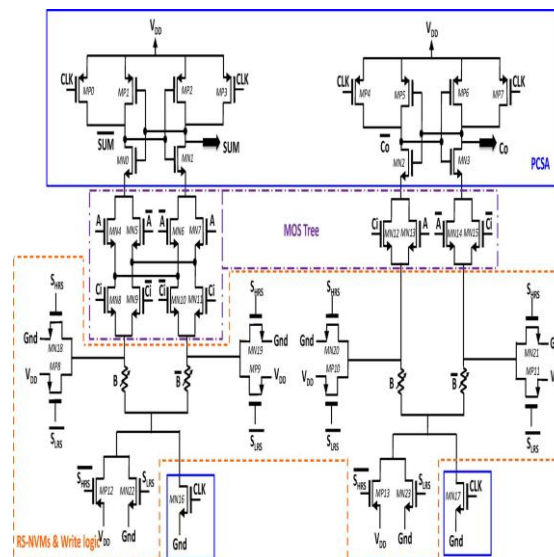


Fig.2 NVF architecture based on RS-NVMS

IV. FULL ADDER ARCHITECTURE

Based on the design of fundamental “AND” and “XOR” logic gates with RS-NVMs, one more complex logic gate, 1 bit non-volatile full-adder (RS-NVFA), has been investigated. The logic functions are Noted that active value is also set here to ‘0’:The architecture inputs are the outputs are “SUM” is volatile and can be changed with the high frequency of computation; on the contrary, is non-volatile and could change with are latively low frequency. “CLK” synchronizes the results of this computing unit.

As it equals to ‘0’, “SUM” and “Co” are recharged to “Vdd” or logic ‘1’, then the evaluation will occur when it is set to ‘1’.It is an optimized design based on the strategies For instance, according to the right branch of the general structure to perform logic includes three parallel sub-branches: AB, and . In the other side, there are also three parallel sub-branches exhibits the truth table and the resistance configurations. We can find Fig.2 whatever the value sub-branches and have no impact on the output. If the resistance of the two sub-branches is exactly the same. If they are the same, This allows the two sub-branches to be deleted from the structure without any impact.

The two sub-branches AB and can be combined to B, which is its optimized structure for logic gate. It is important to note that there is neither capacitance for the data sensing and nonmagnetic field for data programming in this ultimate RS-NVFA structure. This is advantageous compared to the previous structures allowing this design suitable for advanced technological nodes below 65 nm and efficient area minimization. Electrical simulations with the STT-

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MRAM and OxRRAM technologies confirm that behaviours of “SUM” and “Co” agree with the addition logic function for the whole truth table. They have been performed respectively with Specter and Eldon simulators. For instance, as , the result will be ‘1’ and no carry yields; in another case, will be ‘0’ and the carry “Co” becomes ‘1’.

V. PERFORMANCE COMPARISON

The delay time and dynamic power of RS-NVFA are comparable to synchronous CMOS FA powered also by 1.2 V supply. Different resistance characteristics of RS-NVMs can slightly affection the speed and power performance, however the power-delay product (PDP) keeps the same value. The delay time is slightly higher for NVFA; this is due to the additional resistance in the discharge (DC) current path from to Gnd. This can explain also the decreasing of dynamic power@500MHz even though the PDP exceeds that of a CMOS full-adder by %. It is advantageous in the terms of *standby power*, with an appropriate system designed based on this circuit, they can be powered off completely during “idle” state. The similar comparison which concludes limited dynamic power gain of RS-NVFA over CMOS-only FA due to the switching power of in-plane shape anisotropy MTJ. However the current research focus of STT-MRAM is PMAMTJ, which provides much lower power and faster speed than in-plane MTJ.

It allows the RS-NVFA to provide advantageous whole power performance. Thanks to the 3-D integration technology, the die area of our design is slightly more compact than the conventional CMOS Full-adder, % as the RS-NVMs are on top of CMOS circuits. We used the CMOS Full-adder in the commercial library of STMicroelectronics this integration allows also the elimination of dynamic power dedicated for data transfer between logic units and memory array. The data transfer distance becomes some m instead of some mm in conventional CMOS computing systems.

VI. SIMULATION RESULTS

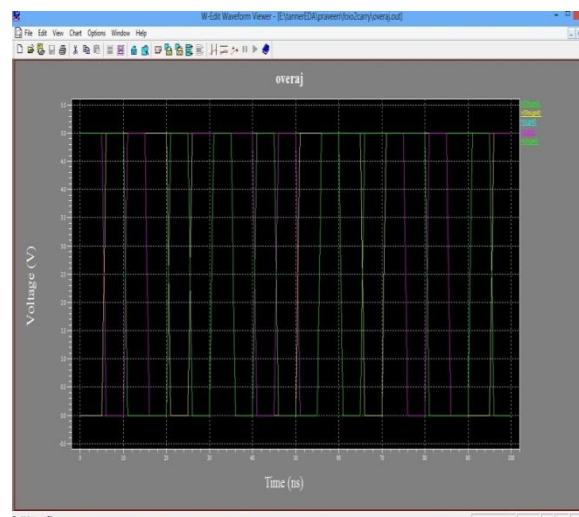


Fig.3 Full Adder Carry Output

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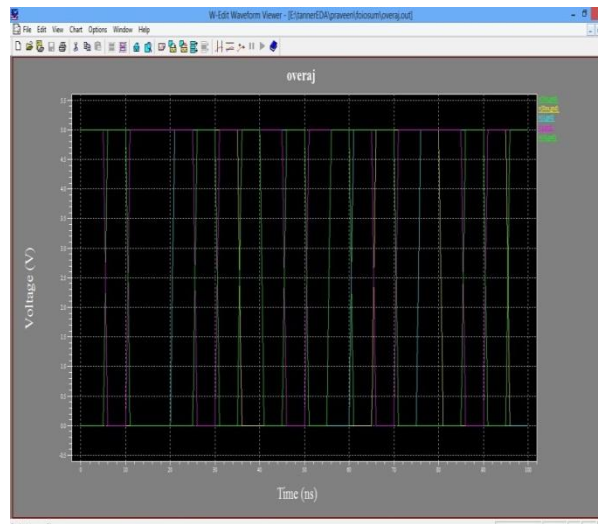


Fig.4 Full Adder Sum Output

VII.CONCLUSION

This paper described the generic concept of RS-NVL architecture based on complementary RS-NVMs. Based on the design strategies and theoretical analysis for optimization, compact structures can be obtained. They can be easily extended to different RS-NVM technologies and allow the designers to better understand the “logic-in-memory” architecture. By using compact models of STT-MRAM and OxRRAM, RS-NVL circuits have been simulated successfully to validate their functionality.

We also run Monte-Carlo simulations to test the NVFA design robustness and we show that the failure rate can be low even if and values distribution is large until .We finally simulated two RS-NVFAs and compared their performance with CMOSFA. The results confirm that RS-NVL is an efficient solution to reduce the whole power and improve logic density benefiting from the 3-D integration of RS-NVM. Demonstrator of these RS-NVL gates is under development by our groups with STMicroelectronics.

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