

Signal Integrity Issues in 3D IC Design- A Theoretical Study

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ABSTRACT: In this paper, we have considered the signal integrity issues of through-silicon-via (TSV)-based 3D Integrated Circuits. Advanced system integration technology, either via Through Silicon Stack (TSS) and/or Through Silicon Interposer (TSI), involves tighter evaluation of the coupling effects in the system-wide Power Distribution Network (PDN) impedance and Signal Integrity (SI) characteristics. If these communications are not properly accounted early in the design cycle, undesired design loop iterations, affecting design efficiency is possible. Therefore, new tools and flows incorporating abstracted physical information of the Power Distribution Network and Clock Distribution Network (CDN) are needed for early design exploration. This paper elaborates on the problems, tool flows and methods necessary to deal with these challenges for 3D systems.

KEYWORDS: Signal Integrity, Power Integrity, Power Distribution and Clock Distribution Networks, Through Silicon via (TSV).

I. INTRODUCTION

In the realm of high – speed digital design, Signal Integrity has become a critical issue, and is posing increasing challenges to the design engineers. Many signal integrity problems are electromagnetic phenomena in nature and hence related to the EMI/EMC issues. The term Signal Integrity (SI) addresses two concerns in the electrical design aspects – the clock signal timing and the quality of the signal. Does the signal reach its destination when it is supposed to? And also, when it gets there, is it in good condition? The goal of signal integrity analysis is to ensure high – speed data transmission [1]. High speed reduces the margin of error for clock timing signals. Accurately distributing the system clock to multiple circuits on a large p.c. board requires an unprecedented level of precision. At high speeds, timing errors are magnified, both in timing pulse alignment and in rise/fall times that can cause overlapping signals or violations of digital circuit setup and propagation delay times.

The Core Issues of Signal Integrity

The various causes of signal integrity problems are grouped into related areas. These are listed according to the approximate degree of difficulty:

1. Transmission line effects-losses and reflections in interconnecting traces, including package leads, vias and connectors, as well as impedance matching to the active devices.
2. Coupling effects-crosstalk between signal lines, or between signal and clock lines.
3. Ground currents-Signal return currents (the “other side” of transmission lines); propagated signal, clock and noise; plus DC “ground bounce.”
4. Power integrity-DC supply distribution and decoupling; plus unwanted signal or clock propagation through power distribution circuits.
5. Electromagnetic Interference (EMI) - External noise ingress, self –interference, control of radiated emissions.
6. Circuit design issues-Clock distribution, timing errors, logic process sequencing.

This last item on the list is certainly not the least important, but was put in that position because it should be a

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familiar issue for a digital designer. And there are several other factors that might have been included on this list, such as manufacturing tolerances and temperature, humidity and aging effects [2].

The study carried out in this paper is divided into two phases. 1) Power Distribution Network Design 2) Clock Distribution Network Design. Ideally, the AC impedance, between power and ground, should be zero, up to the maximum operating frequency for reliable performance. To achieve this the power distribution network (PDN) of a multilayer PCB should be designed in such a way to distribute low noise and stable power to ICs over the entire board area. For the synchronization issue of 3-D ICs, we focus on the analysis of the variability and the performance of 3-D clock distribution networks.

Paper is organized as follows. Section II describes about the PDN planning tool which is very essential to effectively analyse the PDN requirements and to ensure confidence in the performance and reliability of the product. In section III, we explore more aggressive 3D CDN circuits and structure that improve both energy efficiency and latency by 3D stacking, as well as the additional reduction of CDN power supply. Finally, Section IV presents conclusion.

II. POWER DISTRIBUTION NETWORK PLANNING AND DESIGN

Today's high-performance processors, with sub nanosecond switching times, use low DC voltages with high transient currents and high clock frequencies in order to minimize the power consumption and hence, heat dissipated. Fast rise times, low output-buffer impedance and the simultaneous switching of busses create the high transient currents in the power and ground planes, degrading performance and reliability of the product. Adequate power delivery can exhibit intermittent signal integrity issues. Also, many failures to pass electromagnetic compliancy (EMC) are due to excessive noise on the PDN coupling into external cables and radiating emissions.

A typical high-speed design, incorporating DDR3 memory, contains five or six individual power supplies. The PDN must accommodate these variances of current drawn with as little change in power supply voltages as possible (5% voltage ripple is a typical requirement). So the goal of PDN planning is to design a stable power source, taking the above into account, for all the required power supplies. Ideally, the effective impedance of the PDN should be kept as low as possible, up to the maximum operating frequency. PDN planning is a trade-off of cost/performance and results in the following:

- Gives higher confidence and reliability in the performance of the product
- Meets the performance target at the lowest cost of production
- Finds and eliminates issues early in the design cycle

As with stack up planning, the PDN design is required before a single IC is placed on the board. Figure 1 shows the topology of the PDN which includes the VRM, bulk bypass and decoupling capacitors, the plane, the die capacitance, plus BGA via and via spreading inductance.

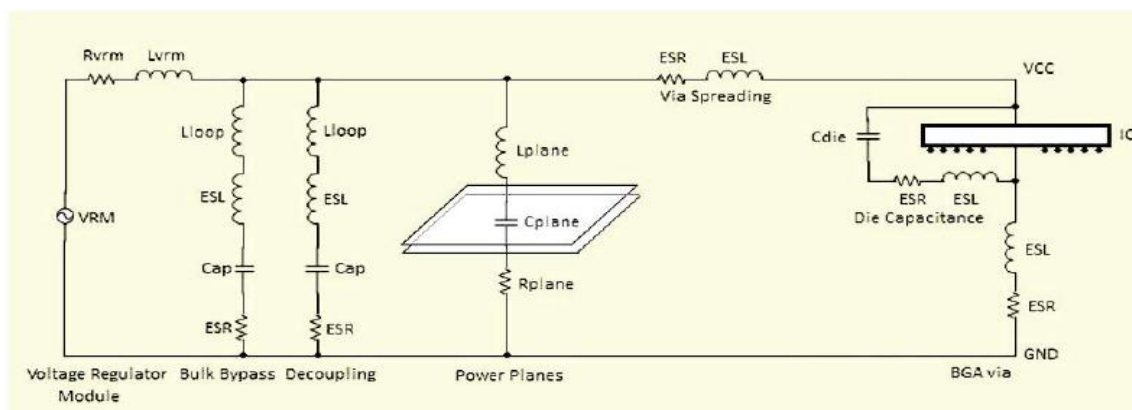


Figure 1: Topology of Power Distribution Network

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Figure 2 illustrates the resonant frequency of the PDN components. Each component added to the PCB lowers the impedance of the PDN at a particular frequency. The PDN impedance for a computer-based product must be kept low and flat over a large frequency range for improved product performance.

Each capacitor's resonant frequency can be calculated by:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad \text{--- (1)}$$

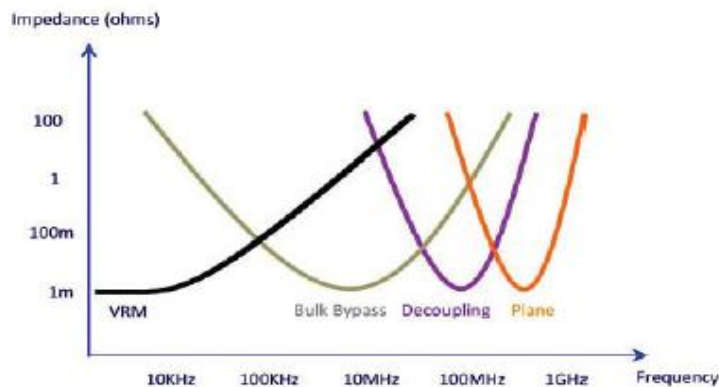


Figure 2: Impedance Characteristics of PDN

The first major component of the PDN is the voltage regulator module (VRM). The VRM is typically a switching regulator that adjusts the amount of current being supplied (via feedback) to keep the voltage constant at frequencies from DC to a few hundred KHz (depending on the regulator). For all transient events that occur at frequencies above this range, there is a time lag before the VRM can respond to the new level of demand.

The second major component of the PDN is the bulk bypass (tantalum) and decoupling capacitors (ceramic). These capacitors supply instantaneous current (at different frequencies) to the drivers until the VRM can respond. In other words, it takes a finite amount of time for current to flow from the power supply circuit (whether on-board or remote) due to the inductance of the trace and/or leads to the drivers. Every decoupling capacitor has an equivalent series inductance (ESL) which causes its impedance to increase at high frequencies. The bulk bypass capacitance provides low impedance, up to 10 MHz. High-frequency decoupling is provided by ceramic capacitors up to several hundred MHz, but above that only the third major component of the PDN—the plane capacitance itself—can reduce the PDN impedance. The power-to-ground plane capacitance of the PCB provides an ideal capacitor in that it has no series lead inductance and little equivalent series resistance (ESR), which helps to reduce noise at extremely high frequencies.

Capacitors reach their minimum impedance at their resonant frequency, which is determined by the capacitance and the ESL. To meet the target impedance at a particular frequency, a capacitance value is chosen so that when mounted on the PCB, it will resonate at the desired frequency, and have impedance that is equal to its ESR. Then, a sufficient number of those capacitors are placed in parallel so that the parallel ESRs approach the desired target impedance.

From Figure 2, it is clear that each different value capacitor has a different resonant frequency. So one would assume that by placing many different values of capacitors on the board, the entire frequency range would be covered or have minimal impedance from DC to maximum frequency. Unfortunately, it is not as simple as that. Lower inductance is achieved by placing the capacitors as close as possible to the power pins. Thus a PDN planning tool is very essential to effectively analyse the PDN requirements and to ensure confidence in the performance and reliability of the product [3].

III. DESIGN OF CLOCK DISTRIBUTION NETWORKS FOR TSV BASED 3D ICs

For 3D synchronous digital systems, the Clock Distribution/Generation Network (CDN) circuit and architecture is one of the most important and challenging issue for design considerations. Therefore, 3D integration enables stacking several tiers directly on the top of a microprocessor which improves significantly both power efficiency and latency between the stacked devices. However, one of the key issues in 3D CDN is to minimize clock skew at the 3D clock tree leaves of different tiers. Another key issue is to improve the power efficiency of 3D CDN [4] – [5].

Recent CDN topologies for 3D ICs including H-trees, rings, and meshes or the combination of these structures are widely used to generate the symmetrical structure of CDN and improved synchronous clock in 3D ICs [6]. However, these approaches are considering only 2D CDN organizations such as basic CDN flip-flops placement algorithms and the size reduction of the clock trees buffers. Lastly, recent 3D CDN studies are based on only lumped R-L-C models for such a 3D TSV model and 2D clock tree channel [7],[8]. The 3D TSV and on-chip CDN channels are based on the highly accurate 3D electromagnetic (EM) solver (HFSS) and 2D EM Momentum models, respectively. In this section, we analyze and design novel 3D CDN circuits and organizations that improve both power efficiency and latency by using highly accurate 3D EM TSV and 2D Momentum on-chip transmission line models. Our analysis of the latency and power consumption provides comparative understanding of the advantages and disadvantages of each 3D CDN topology.

Figure 3 shows 2D and 3D clock tree structures. A clock source must be located in the third tier in order to keep the symmetry of the structures.

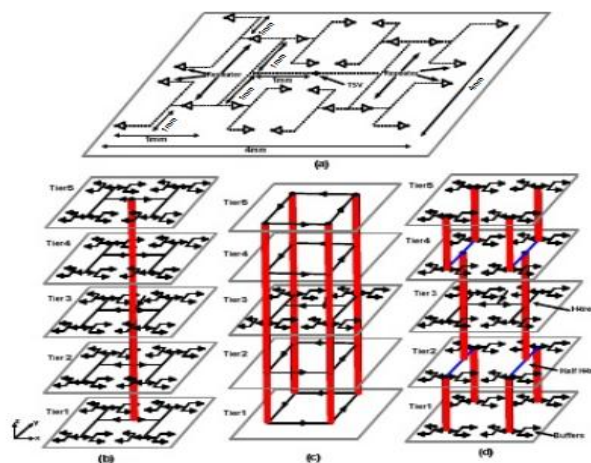


Figure 3: (a) 2D H-tree CDN structure. (b) 3D CDN structure using H-trees in all tiers (c) 3D CDN using H-tree and global rings [10] (d) Energy efficient 3D Symmetrical Centroid Tree (SCT) CDN structure.

Figure 3(a) shows the H-tree structure used for 3D H-tree CDN (Figure 3(b)). This H-tree is a 4-level clock tree which is going to distribute the clock signal all over a 4mm X 4mm die. Figure 3(c) uses the global rings structure to reduce overall 3D CDN power [10]. The third tier in a global rings structure has an H-tree clock network and the other tiers use ring type clock networks.

Figure 3(d) shows our proposed 3D symmetrical centroid tree (SCT) structure to improve power efficiency and reduce clock skew of 3D CDN. The SCT CDN structure has an H-tree clock network in the center (or middle) tier that distributes the clock signal all over the third tier. The clock signal is transferred to the other tiers (second and fourth tiers) using 4 symmetrical and centroid shape of 3D TSV. The CDN in 2 and 4 tier are two half H-tree structures. Finally the 2 and 4 tier is connected to 1 and 5 tier using 8 TSVs. The clock signal is distributed using buffers all over these tiers. Our proposed SCT CDN structure has less TSVs compared to global rings clock tree [6] which further leads to the reduction of the overall R-L-C parasitics. Moreover, 1, 2, 4 and 5 tier's clock trees are changed by removing the first clock buffer of 3 tier clock source to save more power. Therefore, the proposed 3D SCT CDN can

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improve overall power efficiency and minimize unwanted clock skews due to much simpler structures (i.e., less buffers are used). In a general case, number of the TSVs used in a 3D structure using SCT CDN is limited by the power consumption requirements of the system.

The circuit diagram of the transmitter and receiver blocks are shown in Figure 4(a) and 4(b), respectively. The clock transmitter circuit has a clock generation circuit which works at 1.6GHz for DDR3 applications. The generated clock is fed into a clock driver circuit to drive the off-chip transmission line in the 2D structure. The transmission line is a 30cm PCB line. This transmission line is connected to the clock receiver which includes the receiver circuit and the clock trees. The transmission line is replaced with a TSV model to simulate the 3D structure. However multiple TSV models should be used to model multi connections between tiers [9].

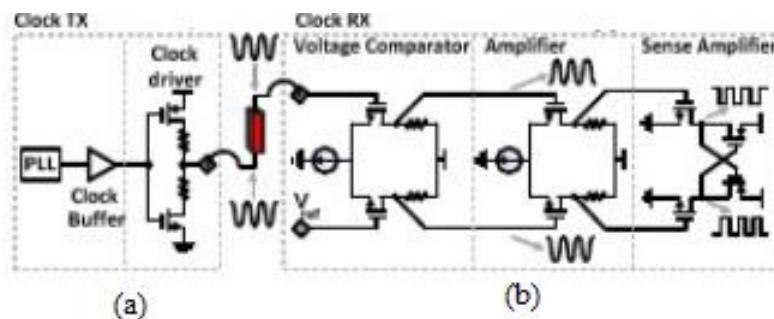


Figure 4: Low swing SCT Clock Transmitter and Receiver

IV. CONCLUSION

In this paper, we suggested the PDN planning tool which is very essential to effectively analyse the PDN requirements and to ensure high performance and reliability of the product. Also we explore more powerful 3D SCT CDN circuits and structure that improve both energy efficiency and latency by 3D stacking, as well as the additional reduction of CDN power supply.

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