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# Analysis of VSI fed IM Drives using SVPWM and RFPWM Techniques

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**ABSTRACT:** This paper mainly focus on harmonics analysis of three phase AC supply available from three phase voltage source inverter which is fed to induction motor drives using various PWM techniques based on Field programmable Gate Array. Ideally the output of inverter should be sinusoidal but due to harmonics the output having distorted waveforms. A number of Pulse width modulation (PWM) schemes are used to obtain variable voltage and frequency supply. The most widely used PWM schemes for three-phase voltage source inverters are carrier-based sinusoidal PWM, Space vector PWM (SVPWM) and Random frequency PWM (RFPWM). There is an increasing trend of using SVPWM because of their easier digital realization and better DC bus utilization. The SVPWM pulses thus generated through FPGA is given as switching pulses to VSI circuit to trigger the motor. The gating signals to the inverter are produced by means of RFPWM to significantly reduce harmonics in comparison to currently used PWMs. FPGA is used to produce gating signals to the switches in a three phase bridge inverter since a faster speed of operation is needed. This paper discuss the harmonic analysis of VSI fed IM drives using SVPWM and RFPWM techniques based on implementation of FPGA. The Simulation is carried on VHSIC Hardware Description language (VHDL) using modelsim.

**KEYWORDS:** VHDL, Space vector PWM (SVPWM), Random frequency PWM (RFPWM), Voltage Source Inverter (VSI) Drive, Total Harmonic Distortion (THD).

#### 1. INTRODUCTION

AC drives are more predominant than dc drives. Ac drives requires high power variable voltage variable frequency supply. The research in Pulse width modulation schemes has been intensive in the last couple of decades. PWM techniques have been used to achieve variable voltage and variable frequency in ac-dc and dc-ac converters. PWM techniques are widely used in different applications such as variable speed drives (VSD), static frequency changers (SFC), and un-interruptible power supplies (UPS) etc. The main problems faced by the power electronic design engineers are about the reduction of harmonic content in inverter circuits. The classical square wave inverter used in low or medium power applications suffers from a serious disadvantage such as lower order harmonics in the output voltage. One of the solutions to enhance the harmonic free environment in high power converters is to use PWM control techniques. The objective of PWM techniques was to fabricate a sinusoidal AC output whose magnitude and frequency could both be restricted.

The main aim of pulse width modulation (PWM) technique in an inverter is to shape the output voltage/output current spectra in a way to eliminate lower order harmonics. If the controller part is analog based then the implementation needs complete substitution [2], [3]. Hence the need for fast prototyping and reprogrammable configuration is now growing up in control of power converters. FPGA incorporates the architecture of gate arrays and the programmability of programmable logic devices (PLD's). The fundamental component and total harmonic distortion (THD) can be controlled by Random Frequency carrier PWM. Each of the above methods possesses different patterns of pulse width modulation, and harmonic components [4], [5]. Though sinusoidal pulse width modulation renders many advantages, its foremost disadvantage is the fundamental magnitude restriction which can be overcome through over modulation by increasing duty cycle [6]. But when this method is operated beyond a particular modulator voltage it introduces lower order harmonics. In order to minimize unwanted harmonic content, i.e., a THD, a number of PWM techniques have been developed to reduce THD and switching losses [7]. Since a three-phase bridge inverter



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provides adjustable frequency power than any other type of inverters it is preferred for industrial applications. In power electronics, various pulse width modulation (PWM) techniques are widely employed to control the output of inverters. The gating signals to the inverter are produced by means of Random Frequency carrier PWM technique. The Field Programmable Gate Array is used to produce the gating signals. As to modulation is concerned the space vector modulation (SVM) has attracted great interest in recent years. Because the harmonic better than those of the other modulation method. The advantage of lower THD is without increasing the switching losses. The emergence of multilevel inverters has been in increase since the last decade. These new types of converters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum. Thus this paper demonstrates that a more efficient and faster solution is the use of Field Programmable Gate Array (FPGA's), it investigates how to generate a variable PWM waveform based on Xilinx FPGA and the proposed design is tested by functional/timing simulation and experiments.

#### II. SPACE VECTOR PULSE WIDTH MODULATION (SVPWM)

Space Vector Modulation (SVM) was originally developed as vector approach to Pulse Width Modulation (PWM) for three phase inverters. It is a more sophisticated technique for generating sine wave that provides a higher voltage to the motor with lower total harmonic distortion. The main aim of any modulation technique is to obtain variable output having a maximum fundamental component with minimum harmonics. Space Vector PWM (SVPWM) method is an advanced; computation intensive PWM method and possibly the best techniques for variable frequency drive application. The circuit model of a typical three-phase voltage source PWM inverter is shown in Figure-1. S<sub>1</sub> to S<sub>2</sub>

are the six power switches that shape the output, which are controlled by the switching variables a, a', b, b', c and c'. When an upper switch is switched on, i.e., when a, b or c is 1, the corresponding lower transistor is switched off, i.e., the corresponding a', b' or c' is 0. Therefore, the on and off states of the upper switch  $S_1$ ,  $S_2$  and  $S_5$  can be used to

determine the output voltage. SVPWM is a different approach from PWM modulation, based on space vector representation of the voltages in the  $\alpha$ - $\beta$  plane. The  $\alpha$ - $\beta$  components are found by Clark's transformation. Space Vector PWM (SVPWM) refers to a special switching sequence of the upper three power transistors of a three-phase power inverter. It has been shown to generate less harmonic distortion in the output voltages and/or currents applied to the phases of an AC motor and to provide more efficient use of dc input voltage. Because of its superior performance characteristics, it has been finding widespread application in recent years.



Figure-1. Three phase voltage source inverter



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#### **III. SPACE VECTOR CONCEPT**

The space vector concept, which is derived from the rotating field of induction motor, is used for modulating the inverter output voltage. In this modulation technique the three phase quantities can be transformed to their equivalent two-phase quantity either in synchronously rotating frame (or) stationary frame. From these two-phase components, the reference vector magnitude can be found and used for modulating the inverter output. The process of obtaining the rotating space vector is explained in the following section, considering the stationary reference frame. Considering the stationary reference frame let the three-phase sinusoidal voltage component be,

$V_a = V_m Sin(\omega t)$	(1)
$V_b = V_m \sin(\omega t - 2\pi/3)$	(2)
$V_c = V_m Sin (\omega t - 4\pi/3)$	(3)

When this three-phase voltage is applied to the AC machine it produces a rotating flux in the air gap of the AC machine. This rotating resultant flux can be represented as single rotating voltage vector. The magnitude and angle of the rotating vector can be found by means of Clark's Transformation as explained below in the stationary reference frame. To implement the space vector PWM, the voltage equations in the abc reference frame can be transformed into the stationary dq reference frame that consists of the horizontal (d) and vertical (q) axes as depicted in Figure-2. From Figure-2, the relation between these two reference frames is below



Figure-2. The relationship of abc reference frame and stationary dq reference frame.

$$\mathbf{K}_{s} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}, \ \mathbf{f}_{dq0} = \begin{bmatrix} f_{d}f_{q}f_{0} \end{bmatrix}^{\mathrm{T}}, \ \mathbf{f}_{abc} = \begin{bmatrix} f_{a}f_{b}f_{c} \end{bmatrix}^{\mathrm{T}},$$
(5)

and f denotes either a voltage or a current variable.

As described in Figure-2. This transformation is equivalent to an orthogonal projection of [a b c] onto the twodimensional perpendicular to the vector  $\begin{bmatrix} 1 & 1 \end{bmatrix}^{t}$  (the equivalent d-q plane) in a three-dimensional coordinate system. As a result, six non-zero vectors and two zero vectors are possible. Six non-zero vectors  $(V_1 - V_6)$  shape the axes of a hexagonal as depicted in Figure-3, and supplies power to the load. The angle between any adjacent two non-zero vectors is 60 degrees. Meanwhile, two zero vectors  $(V_0 \text{ and } V_7)$  and are at the origin and apply zero voltage to the load. The eight vectors are called the basic space vectors and are denoted by  $(V_0, V_1, V_2, V_3, V_4, V_5, V_6, V_7)$ . The same



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transformation can be applied to the desired output voltage to get the desired reference voltage vector,  $V_{ref}$  in the d-q plane. The objective of SVPWM technique is to approximate the reference voltage vector  $V_{ref}$  using the eight switching patterns. One simple method of approximation is to generate the average output of the inverter in a small period T to be the same as that of  $V_{ref}$  in the same period



### IV. SWITCHING STATES

Voltage	Switching vectors		Line to neutral voltage		Line to line voltage				
vectors	A	В	С	V <sub>an</sub>	V <sub>bn</sub>	V <sub>cn</sub>	V <sub>ab</sub>	V <sub>bc</sub>	V <sub>0</sub>
V <sub>0</sub>	0	0	0	0	0	0	0	0	0
V <sub>1</sub>	1	0	0	2/3	-1/3	-1/3	1	0	-1
V <sub>2</sub>	1	1	0	1/3	1/3	-2/3	0	1	-1
V <sub>3</sub>	0	1	0	-1/3	2/3	-1/3	-1	1	0
V <sub>4</sub>	0	1	1	-2/3	1/3	1/3	-1	0	1
V <sub>5</sub>	0	0	1	-1/3	1/3	2/3	0	-1	1
V <sub>6</sub>	1	0	1	1/3	-2/3	1/3	1	-1	0
V <sub>7</sub>	1	1	1	0	0	0	0	0	0

Table-1. Switching patterns and output vectors.



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For 180° mode of operation, there exist six switching states and additionally two more states, which make all three switches of either upper arms or lower arms ON. To code these eight states in binary (one-zero representation), it is required to have three bits  $(2^3 = 8)$ . And also, as always upper and lower switches are commutated in complementary fashion, it is enough to represent the status of either upper or lower arm switches. In the following discussion, status of the upper bridge switches will be represented and the lower switches will it's complementary. Let "1" denote the switch is ON and "0" denote the switch in OFF. Table-1 gives the details of different phase and line voltages for the eight states.

#### V. SOFTWARE IMPLEMENTATION OF SVPWM

Space vector PWM can be implemented by the following steps:

**Step-1:** Determine Vd, Vq, Vref and angle ( $\alpha$ ).

**Step-2:** Determine the time duration T1,T2 and T0.

Step-3: Determine the switching time of each transistor (S1 to S6)

Step-1: Determine Vd, Vq, Vref and angle (α)

From Figure 4 Vd, Vq, Vref and angle ( $\alpha$ ) can be calculated as follows:

$$V_{d} = V_{an} - V_{bn} \cdot \cos 60^{\circ} - V_{cn} \cdot \cos 60^{\circ}$$
$$= V_{an} - \frac{1}{2} \cdot V_{bn} - \frac{1}{2} \cdot V_{cn}$$
(6)

$$V_{q} = 0 + V_{bn} \cdot \cos 30^{\circ} - V_{cn} \cdot \cos 30^{\circ}$$

$$= V_{an} + \frac{\sqrt{3}}{2} \cdot \cos 30^{\circ} - \frac{\sqrt{3}}{2} \cdot \cos 30^{\circ}$$
(7)

$$\therefore \begin{bmatrix} \mathbf{V}_{d} \\ \mathbf{V}_{q} \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \mathbf{V}_{an} \\ \mathbf{V}_{bn} \\ \mathbf{V}_{cn} \end{bmatrix}$$
(8)

$$\therefore \left| \overline{\mathbf{V}}_{\mathrm{ref}} \right| = \sqrt{\mathbf{V}_{\mathrm{d}}^{2} + \mathbf{V}_{\mathrm{q}}^{2}} \tag{9}$$

$$\alpha = \tan^{-1} \left( \frac{V_d}{V_q} \right) = wt = 2\pi ft$$
, where  $f = fundamental$  frequency.





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#### Step-2: Determine the time duration T1, T2 and T0

From Figure-5 the switching time duration can be calculated as follows:

Switching time at sector -1



Figure-5. Reference vector as a combination of adjacent vectors at sector-1.

$$\int_{0}^{T_{z}} \overline{\nabla}_{ref} = \int_{0}^{T_{1}} \overline{\nabla}_{1} dt + \int_{T_{1}}^{T_{1}+T_{2}} \overline{\nabla}_{2} dt + \int_{T_{1}+T_{2}}^{T_{z}} \overline{\nabla}_{0}$$
(10)

$$\int_{0}^{T_{e}} \overline{\nabla}_{ref} = \int_{0}^{T_{1}} \overline{\nabla}_{1} dt + \int_{T_{1}}^{T_{1}+T_{2}} \overline{\nabla}_{2} dt + \int_{T_{1}+T_{2}}^{T_{2}} \overline{\nabla}_{0}$$
(11)

$$\Rightarrow T_{Z} \cdot \nabla_{ref} = (I_{1} \cdot V_{1} + I_{2} \cdot V_{2})_{(12)}$$

$$\Rightarrow T_{Z} \cdot \left[ \overline{\nabla_{ref}} \right] \cdot \left[ \frac{\cos(\alpha)}{\sin(\alpha)} \right] = T_{1} \cdot \frac{2}{3} \cdot V_{dc} \cdot \left[ \begin{matrix} 1 \\ 0 \end{matrix} \right] + T_{2} \cdot \frac{2}{3} \cdot V_{dc} \cdot \left[ \begin{matrix} \cos(\frac{\pi}{3}) \\ \sin(\frac{\pi}{3}) \end{matrix} \right]$$

$$(13)$$

$$\therefore T_1 = T_Z \cdot a \cdot \frac{\sin(\frac{\pi}{3} - \alpha)}{\sin(\frac{\pi}{3})} \quad (\text{Where, } 0 \le \alpha \le 60^\circ \text{ )} \quad (14)$$

$$\therefore T_2 = T_Z \cdot a \cdot \frac{\sin(\alpha)}{\sin(\frac{\pi}{3})}$$
(15)

$$\therefore T_0 = T_Z - (T_1 + T_2) \left( \text{where, } T_Z = \frac{1}{f_z} \text{ and } a = \frac{\left| \overline{\nabla}_{ref} \right|}{\frac{2}{3} \cdot \nabla_{dc}} \right) \quad (16)$$

Switching time during any sector

$$=\frac{\sqrt{3} \cdot T_{Z} \cdot \left|\overline{V}_{ref}\right|}{V_{dc}} \cdot \sin\left(\frac{n}{3}\pi - \alpha\right)$$
(17)

$$=\frac{\sqrt{3}\cdot T_{Z}\cdot |\overline{\nabla}_{ref}|}{V_{dc}}\cdot \left(\sin\frac{n}{3}\pi\cdot\cos\alpha-\cos\frac{n}{3}\pi\cdot\sin\alpha\right)$$
(18)

$$\therefore T_2 = \frac{\sqrt{3} \cdot T_Z \cdot \left| \overline{V}_{ref} \right|}{V_{dc}} \cdot \left( \sin\left(\alpha - \frac{n-1}{3}\pi\right) \right)$$
(19)

$$= \frac{\sqrt{3} \cdot T_Z \cdot \left| \overline{\nabla}_{ref} \right|}{V_{dc}} \cdot \left( -\cos\alpha \cdot \sin\frac{n-1}{3}\pi + \sin\alpha \cdot \cos\frac{n-1}{3}\pi \right)$$
(20)  
$$\therefore T_0 = T_Z - T_1 - T_2 \left( \begin{array}{c} \text{where, } n=1 \text{ through } 6(\text{that is, Sector 1 to } 6) \\ 0 \le \alpha \le 60^{\circ} \end{array} \right)$$

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#### Step 3: Determine the switching time of each transistor (S1 to S6)

Simulation Steps:

- (1) Initialize system parameters in MATLAB/SIMULINK.
- (2) Perform M-File coding to
  - (i) Determine sector
  - (ii) Determine time duration T1, T2, T0
  - (iii) Determine the switching time (Ta, Tb, and Tc) of each transistor (S1 to S6)

(iv) Generate the inverter output voltages (VAB, VBC, VCA,)

(v) Generate VHDL Codings through software conversion tool

- (vi) Burn the program in the FPGA kit
- (vii) View the SVPWM waveforms through Xilinx.

#### VI. FIELD PROGRAMMABLE GATE ARRAY

A Field-Programmable Gate Array or FPGA is a silicon chip containing an array of configurable logic blocks (CLBs). Unlike an Application Specific Integrated Circuit (ASIC) which can perform a single specific function for the lifetime of the chip an FPGA can be reprogrammed to perform different function in a matter of microseconds. The design used Xilinx development tools, namely Work view, and is realized in a single FPGA chip with no external memory [8]. The benefits of this design are as follows

- 1. The whole system is implemented in only a single chip consequently the circuit is very compact.
- 2. Systems of FPGA chip are more reliable because they do not need any control software
- 3. Faster design and verification time, design change without penalty.

In this paper programming FPGA using Hardware Description Languages and coding are used to generate the Space Vector Modulation for the inverter circuit. The point to be noted here is that instead of writing the direct VHDL Codings firstly the M-File codings are written to generate the SVPWM pulses and then after by using the software converter VHDL coding are generated. Thereby the work requires less time and fast operation.

The MATLAB / SIMULINK environment is familiar to vast number of software programmers and since mfile coding is very much common to most of the programmers it becomes easier for individuals to work in this software. A very attractive high-level design/simulation tool is provided by FPGA and is called XILINX. It is a very flexible design tool, which allows Testing of a high-level structural description of the design and makes possible quick changes and corrections. The circuit description structure is very similar to the way the design could be implemented later. Therefore mapping tool allowing conversion of such a structure into VHDL code would save the designer's time, which otherwise has to be spent in rewriting the same structure in VHDL and probably making mistakes that will need debugging.



Figure- 6. Block Diagram of Overall system.



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#### Figure-7. MATLAB/SIMULINK diagram of SVPWM



Figure 8. Expansion of Each Block in Xilinx.



Figure 9.Schematic of the SVPWM techniques in the Xilinx.



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Figure 10. Output Wave form of SVPWM.



Figure 11. SVPWM Technique

Table1. Simulation Results of SVPWM for Output Line Voltage and Total Harmonic Distortion (THD) by Varying modulation index

Modulation Index (M.I)	Output Line Voltage (Peak) Volt	Total Harmonic Distortion(%THD)
0.4	192.70	154.07
0.6	318.10	105.69
0.8	442.90	78.56
0.9	552.30	53.62
1.0	567.90	49.15



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#### VII. RANDOM FREQUENCY PULSE WIDTH MODULATION (RFPWM)

In power electronic systems, pulse width modulation techniques operate at a fixed switching carrier frequency which produces unwanted effects as well as harmonic spikes [10, 11]. The significant importance of a power electronic system employing RFPWM is that its output harmonics are dispersed and distributed. This popular scheme can be achieved by many ways such as varying the switching number in a cycle, the carrier frequency or the slope of the triangular wave [12]. In the proposed method, a randomly chosen carrier frequency signal with the help of random generator is used instead of a fixed carrier frequency as in the case of SPWM to perform the PWM switching scheme. It is preferred for high switching frequencies, owing to its simple architecture. However if the modulation index is low then the performance of the power electronic system will greatly degrade.



Figure 12. Block Diagram of Random Carrier PWM Signal Generation

#### VIII. GENERATION OF RFPWM SIGNALS BY MODELSIM

The first and foremost aspect in generating sine PWM is to generate voltage-controlled oscillations. As the entire process is in digital format, it is not possible to generate the conventional analog sine wave [13,14]. Further, this sine wave serves as a reference signal for comparison. Hence, if we know the values of the voltage controlled oscillations at any instant, then the purpose could be served. In this scheme, the controlled sinusoidal oscillations are generated in the form of a look up table and the amplitude control block controls the voltage magnitude. The regular sampling has certain advantages when implemented using digital techniques [15, 16]. Let the clock frequency be 50MHz which is the set frequency that the sine wave generator receives. It's quite a common thing to generate sine wave of set frequency using the governing equation given by,  $V(t) = Vm \sin 2\pi ft$ . But in digital logic, the problem arises in describing the limits for t, the time for which the wave has to be generated and the period of oscillations. Hence, the methodology we have adopted for creating the lookup table is that the instantaneous values of sinusoidal oscillations are fragmented to 200 values at equal intervals. These values are stored as an integer array named as memory. Further instead of the factor  $2\pi ft$  it is multiplied with an offset value and an integer which would in turn point to the value stored in the sine wave array. The sine array is incremented in steps of one so that to represent a half cycle of the oscillation corresponding to 360°, it is essential to make 199 increments of the counter. Since we are in need of three phase sine wave, we need to have three sine wave generators, whose outputs are displaced by 120° each. That means, the output of the second generator must start from the initial value of zero when the first generator has swept an angle of 120 degrees. Similarly the third and second generators should follow the same fashion. This is achieved by correlating the relation between the angular displacement and the sine array. Initially the output of first sine wave generator alone is activated and the remaining two are maintained at zero output condition. We have 360 degrees of the sine wave corresponds to 199 increments of the counter. Hence, 120 degrees of the wave would correspond to 66



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increments of the counter. Therefore, at the 66th increment of the sine array of first generator, the output of second generator is activated. Similarly, at the 66th increment of the sine counter of the second generator, the output of third one is activated. Once they are activated in this manner, then throughout the process, they are all displaced by  $120^{\circ}$  or 66 counts.

The high frequency carrier chosen for comparison is of ramp in nature. This is also digitally generated. The frequency of the ramp is randomly chosen as 6 kHz and 9 kHz or any value greater than this can be chosen. Unlike the sine wave, the frequency of the ramp is not maintained constant for a RFPWM. The triangular wave and the sine wave are compared and whenever the magnitude of the sine wave is greater than that of the ramp, output will be high otherwise it is low. This pulse width modulation technique is described by VHDL and simulated using modelsim 6.3f. Since this method is flexible, an important advantage of VHDL is that it is technology independent [17]. The pulses which are obtained as output is fed to the three phase bridge inverter using HDL co -simulation block. The output of the three phase inverter is controlled by Random Frequency Pulse Width Modulation. The simulation model of the control circuit is shown in figure 1. Subsystem1 block generates pulses for the inverter as shown in figure 2. Powergui block given in the circuit measures the fundamental voltage and THD for various values of modulation index ranging from 0.2 to 1.2.

#### IX. SIMULATION AND EXPERIMENTAL RESULTS

The fundamental voltage and Total harmonic Distortion were tested on an experimental test bench on RFPWM technique and the performance is evaluated by connecting a three phase inverter to a 1hp-1500 rpm squirrel cage induction motor. Figure 3 shows the FFT analysis obtained by using the PowerGui block during the matlab-modelsim co simulation and figure 4 shows the modelsim output for the proposed RF-THIPWM. The control of fundamental voltage determines the difficulty of the implementation of a given PWM strategy. In the given RFPWM, a linear relationship exists between fundamental voltage and modulation index and therefore the implementation is simplified. Here the fundamental voltage is varied as a function of modulation index ranging from 0.2 to 1.2. The impact is much significant in the higher values of modulation index. The important sources of distortion in power electronic systems are: the type of modulation technique employed and the nonlinearities in the output voltage. Total Harmonic Distortion (THD) is a standard measure used to characterize the distortion in the output [18], [19].



Figure 13. Simulation Circuit for a three phase inverter using MATLAB



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Figure 15. Modelsim output for RF-THIPWM

Table 2 . Simulation Results of RFPWM for Output Voltage and Total Harmonic Distortion (THD) by varying modulation index

Modulation Index (M.I)	Output Voltage (Peak) Volt	Total Harmonic		
		Distortion(%THD)		
0.4	75.87	163.22		
0.6	111	123.49		
0.8	150.4	92.5		
1.0	190.2	68.43		
1.2	209.8	58.04		



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#### X. CONCLUSION

In this paper we discussed the harmonic analysis of VSI fed IM drives using the SVPWM and RFPWM techniques based on FPGA. The SVPWM switching pattern generated will reduce the harmonic content, provides efficient as well flexible control and reduces the total size of the system. This aims on one hand to prove the effectiveness of the SVPWM in the contribution in the switching power losses reduction. SVPWM is among the best solution to achieve good voltage transfer and reduced harmonic distortion in the output of an inverter. The RFPWM strategy is that it adopts a consistent approach for the entire range of modulation index and also eliminates lower order harmonics for any value of modulation index. In both the modulation technique is implemented in an FPGA by initially generating m-file through MATLAB/SIMULINK environment. The FPGA coding makes it easier in designing the vector modulation pattern generator using field programmable Array. Moreover the MATLAB/SIMULINK environment is familiar to vast number of software programmers and since m-file coding is very much common to most of the programmers it becomes easier for individuals to work in this software.

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