

A New ZCS PWM Full Bridge DC-DC Converter with ANN Controller for PMDC Drives

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ABSTRACT: A new soft switching pulse-width-modulated (PWM) fly back dc/dc converter with a simple auxiliary circuit for PMDC drives with ANN is proposed. This is achieved by using two very simple active auxiliary circuits one active, the other passive. The outstanding feature of the new converter is that it allows its main power switches to operate with zero current switching (ZCS) and with fewer conduction losses than conventional full-bridge converters. By adding this auxiliary circuit to the conventional pulse width modulation isolated fly back converter, all power semiconductor devices are soft switched. In addition, the proposed converter frequency is constant and has no additional current stress in the main switch in comparison with conventional ones. Simulation and experimental results justify the theoretical analysis.

I. INTRODUCTION

NEW techniques are proposed in order to decrease switching losses and to increase power density in dc-dc converters at high power and frequencies [1]–[4]. The applications of soft-switching methods are expanding. The most remarkable method in high-power isolated applications is Phase Shifted (PS) Zero Voltage Switching (ZVS) method, which provides all of the switches to operate with ZVS without any additional auxiliary switches. The parasitic capacitance energy is discharged by the leakage inductance, and the MOSFET turns on with zero voltage transition (ZVT). Insulated gate bipolar transistor (IGBT) is preferred over MOSFET at high voltage and high-power levels in industrial applications. Low R_{DS(on)} MOSFETs are quite expensive compared to the IGBTs with equivalent current and voltage ratings. The choice of IGBT over MOSFET is mandatory due to nonavailability of high voltage and high-current MOSFET devices in some applications. An external snubber capacitor is connected in parallel to each IGBT in order to decrease turn-off losses, in case the IGBT is used in the phase shifted full bridge (PSFB) pulse width modulation (PWM) converter [5]–[26]. When the ZVT condition is not provided at no load and at light loads, the parallel capacitors discharge through IGBT at turn on and this causes increase in switching losses and failure risk of the IGBTs. This condition causes problems at specially the lagging leg [5]–[26]. Capacitor discharge through IGBT restricts the use of high-value capacitor in parallel to IGBT. Therefore, the election of the parallel capacitor value is very important. The parallel snubber capacitor value should be selected according to the speed and the maximum current of the IGBT [5]. The performance of the converter decreases rapidly at high-current levels because of the turn-off switching losses. At the leading leg, the required energy for discharging the parallel capacitor is supplied from the load current, so the use of high-value capacitor in the leading leg has no drawback. In PSFB PWM dc-dc converters, some problems arise such as variation of duty cycle with load current, hard switching because of insufficient energy in leakage inductance at light loads, and high-voltage peaks and oscillations at the output diodes, and increment in the conduction losses because of the primary current flowing in the freewheeling interval. It is possible to encounter many studies in the literature about these converters and solution for the problems [5]–[26].

II. CIRCUIT DIAGRAM

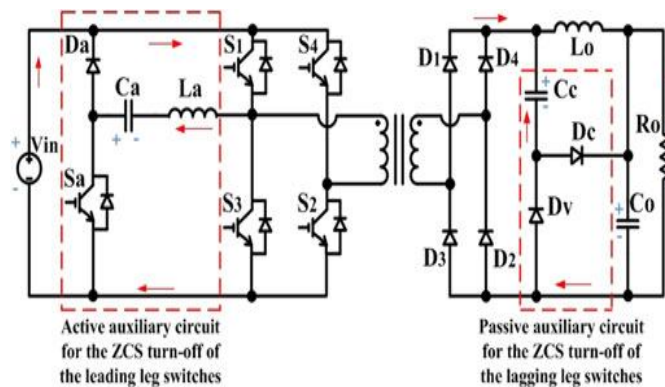


Fig.1.Circuit Diagram Of Dc-Dc Converter

A new ZCS-PWM full-bridge converter is proposed in this paper. The outstanding feature of the new converter is that it allows its main power switches to operate with ZCS and with fewer conduction losses than conventional full-bridge converters. This is achieved by using two very simple active auxiliary circuits—one active with a switch that can turn on and off with ZCS and one passive that consists of a few passive components. The paper presents the new converter and then discusses its operation, steady-state characteristics and design. Experimental results obtained from a converter prototype are presented to validate the converter’s performance and the concepts presented in the paper. A new ZCS-PsWM full-bridge converter is proposed in this paper. The outstanding feature of the new converter is that it allows its main power switches to operate with ZCS and with fewer conduction losses than conventional full-bridge converters. This is achieved by using two very simple active auxiliary circuits—one active with a switch that can turn on and off with ZCS and one passive that consists of a few passive components. The paper presents the new converter and then discusses its operation, steady-state characteristics and design. Experimental results obtained from a converter prototype are presented to validate the converter’s performance and the concepts presented in the paper.

III. CONVERTER OPERATION

The proposed converter is shown in Fig. 1. It operates like a ZVZCS-PWM converter except that the auxiliary circuit is activated whenever the main power switches in the leading leg to which it is attached are about to turn off. It should be noted that in this diagram, as in other circuit diagram present in this paper, the transformer leakage inductance is not shown as a separate element, but is assumed to be a part of the transformer. Equivalent circuit diagrams of the modes of operation that the proposed converter goes through during a half switching are shown in Fig. 2 and ideal converter waveforms are shown in Fig. 3.

It should be noted that in Fig. 3, a current waveforms such as I_{S1} shows the current flowing through a switch (positive part of the waveform) and its body diode (negative part of the waveform). Moreover, the I_{S3} waveform is also the waveform for I_{La} and I_{Ca} as $I_{S3} = I_{La} = I_{Ca}$ and V_{Ca} on the V_{Ca} waveform can be considered to be equal to the input voltage.

When the device is placed in sleep, Timer2 will not increment, and the state of the module will not change. If the CCP pin is driving a value, it will continue to drive that value.

When the device wakes-up, it will continue from this state. In [7], an auxiliary circuit which includes two MOSFETs and a series inductance is proposed. The inductance current is increased before the IGBT devices on the lagging leg are turned off. The ZVS conditions of the FB converter are improved, but the losses in the auxiliary circuit reduce the efficiency. The auxiliary circuit does not operate with soft switching. Main IGBTs are subjected to the current stress before turn off and this increases the switching losses in the turn-off process. The proposed method is not preferred due to low efficiency, high cost, and control difficulty.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

BLOCK DIAGRAM

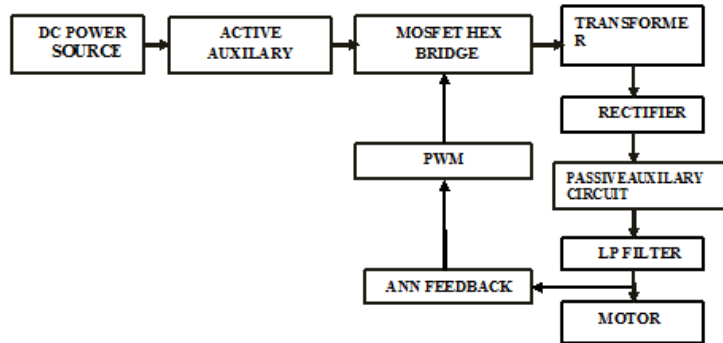


Fig-2 Block Diagram Of Dc-Dc Converter

Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches. The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace.

The longer the switch is on compared to the off periods, the higher the power supplied to the load is. The PWM switching frequency has to be much faster than what would affect the load, which is to say the device that uses the power. Typically switching have to be done several times a minute in an electric stove, 120 Hz in a lamp dimmer, from few kilohertz (kHz) to tens of kHz for a motor drive and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle. In Pulse Width Modulation (PWM) mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCPx pin is multiplexed with the PORT data latch, the corresponding TRIS bit must be cleared to make the CCPx pin an output.

IV. MAIN FEATURES AND DESIGN PROCEDURE

In this section, the design procedure of the proposed converter is given. The component values for implementing the converter are determined according to the design procedure. A. Selection of the Boundary Current I_a The boundary current level I_a . The proposed converter is shown in Fig 1

consists of a conventional PSFB PWM converter and an auxiliary circuit connected to the lagging leg. The auxiliary circuit contains two IGBTs with reverse recovery diodes and two capacitors C_{1A}, C_{2A} . At low output currents, converter operates as the conventional PSFB PWM converter. Low-valued snubber capacitors are connected at the lagging leg. These capacitors provide ZVS operation at light loads and improve the turn-off

behavior of the IGBT until a current level. In the proposed converter, auxiliary circuit is operated only at high-output currents. By means of the auxiliary circuit, high value capacitors are connected to the lagging leg and the turnoff performance of the lagging leg switches is improved. The IGBTs used in the auxiliary circuit operate under soft-switching conditions. The conduction loss of the auxiliary switches is very low because they conduct current for a very short time. The operation of the auxiliary circuit starts when primary current I_P is larger than boundary current level I_a .

V. EXPERIMENTAL RESULTS

An experimental prototype was built to confirm the feasibility of the proposed converter and to compare the efficiency of the converter with both auxiliary circuits (proposed) and without the active auxiliary circuit at the converter's primary side (just ZVZCS). The prototype has the following specifications: Input voltage $V_{in} = 400V$, output voltage $V_o = 380V$, maximum output power $P_o = 3 kW$, and switching frequency $f_{sw} = 80 kHz$. The prototype was implemented using the following component values: $L_a = 3 \mu H$, $C_a = 62 nF$, and $C_c = 3.3 \mu F$. The transformer ratio is 21/18, with $L_{lk} = 3.2 \mu H$ and the following devices were used for the IGBT switches in the prototype:

International Journal of Innovative Research in Science, Engineering and Technology

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IRG4PC50FDEPBF for $S1$ to $S4$ and STGB7NC60HDT4 for the auxiliary switch Sa Voltage and current waveforms of the leading leg switches ($S1, S3$) are shown in Figs. 8 and 9. The auxiliary circuit forces the current to flow through the antiparallel diodes of the switches to make the ZCS turn-off possible. It should be noted that the Fig. 10. Current and voltage waveforms in $S2$ ($I: 10 \text{ A/div}, V: 200 \text{ V/div}, t: 2.5 \mu\text{s/div}$). Fig. 11. Primary voltage waveform across the transformer ($V: 200 \text{ V/div}, t: 2.5 \mu\text{s/div}$). Notches in the current waveforms are due to the ZVZCS property of the converter. Voltage and current waveforms of $S2$ are shown in Fig. 10 to confirm the ZCS operation in the lagging leg as well. Fig. 11 shows the primary voltage across the transformer, which is a regular phase-shifted waveform. Finally, a comparative study was done on the proposed converter with and without the auxiliary circuit and presented in Fig. 12. It can be seen that the proposed converter is about 7% more efficient at full load when it has the auxiliary circuit. It should be noted that the reason for the declining efficiency curve of the ZVZCS converter is that the ZVZCS converter was implemented with IGBTs and two of the switches do not operate with a ZCS turn-off so that the turn-off losses of these switches worsen as the load is increased.

VI. SIMULATION RESULTS

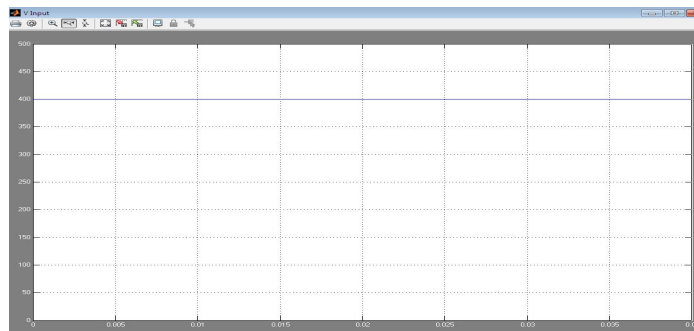


Fig .4 Input Voltage

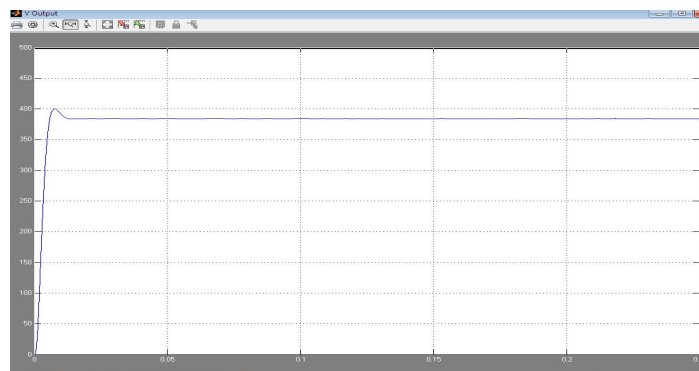


Fig .5 Output Voltage

VII. CONCLUSION

A new ZCS-PWM full-bridge converter is proposed in this paper. The outstanding feature of the new converter is that it allows its main power switches to operate with ZCS and with MOUSAVI AND MOSCHOPOULOS: NEW ZCS-PWM FULL-BRIDGE DC-DC CONVERTER WITH SIMPLE AUXILIARY CIRCUITS 1329 Fig. 12. Efficiency comparison results. fewer conduction losses than conventional full-bridge converters. This is achieved by using a very simple active auxiliary circuit and a ZVZCS technique so that the converter has all the advantageous features of ZVZCS converters but with ZCS operation for all the converter switches so that they can all be IGBT devices, which helps reduce component cost. The proposed converter does not have the drawbacks of previously proposed techniques for higher power dc-dc full-bridge converters with IGBTs, including resonant techniques, ZCS-PWM techniques with

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

active auxiliary circuits, passive techniques, ZVZCS techniques, and techniques that require the use of reverse blocking diodes. Experimental results obtained from a 3 kW, 80 kHz converter prototype confirm the feasibility of the converter and show that the active auxiliary circuit results in a maximum efficiency improvement of 7% compared to the conventional ZVZCS converter due to the elimination of leading leg turn-off losses by the active auxiliary circuit.

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