

A Single Phase Bridgeless Boost Converter for Power Factor Correction on Three State Switching Cells

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ABSTRACT: To Improve power quality in terms of power factor correction and total harmonics distortion using ac-dc converter. By reducing the total harmonics distortion at input ac and regulated dc output has several topologies based on classical converter here boost converter is used to improve power quality. Boost converter become popular by reducing electromagnetic interference levels and also operating in continuous conduction mode a bridge less boost converter based on three state-switching cells is introduces in this paper. Bridgeless boost converter is use of magnetic element with minimized size, weight, and volume is reduced by conduction losses.

KEYWORDS: AC-DC converter, Harmonics, Power Factor, Boost Converter, Three-State Switching Cell.

I. INTRODUCTION

To improve the electrical energy distribution and to provide agreement with the power quality standards, special rectifier structures have been currently used as front end energy processors. But the bridgeless converter continue to be very popular in several industrial and rural applications[1]. Modem Power Electronic loads such as variable speed ac and dc motor drives, uninterruptible power supplies in emergency and standby systems, magnet power supplies and high power induction heating equipment etc. controlled dc power with unidirectional and bidirectional power flow. The drawbacks include poor power quality in terms of injected current harmonics, resulting in voltage distortion and poor power factor at the input ac mains and slow varying rippled dc output at the load end, low efficiency, and large size of ac and dc filters[1]. The boost PFC circuit operating in continuous-conduction mode is, by far, the popular choice for medium and high-power applications. This is because the continuous nature of the boost converter's input current results in low conducted electromagnetic interference compared to other active PFC topologies such as buck-boost and buck converters [2]. The power rating increases as required to associate converters in series or parallel. High-power applications, interleaving of two boost converters is employed to improve the performance and reduce the size of the PFC.

A three-state switching cell (3SSC) can be obtained by the association of two two-state switching cells (2SSCs) interconnected to a center tapped autotransformer, from which a family of dc-dc converters can be derived. achieve high output voltage gain using the 3SSC and the dc-dc boost converter were performed. Two diodes and two capacitors are added, the extension to PFC applications with high efficiency is limited by the presence of increased number of components in the current path during each operating mode an isolated dc-dc boost converter was proposed in [3]. One coupled inductor, one transformer, and a single-phase diode bridge are added to the converter, resulting in a topology with increased number of components and reduced robustness. Within this context, this paper introduces a topological variation of the boost converter based on the 3SSC for PFC applications[3-4]. Four switches and two 3SSCs are used, making this converter suitable for high-current and high-power applications. Moreover, the following advantages can be addressed to the use of the three-state cell Inductors are designed for twice the switching frequency, with consequent reduction of size and weight the current through the switches is half of the input current, part of the

International Journal of Innovative Research in Science, Engineering and Technology

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input power is delivered to the load by the transformer instead of the main switches, consequently reducing conduction and commutation losses lower cost switches can be used due to the possibility of parallelism of any number of cells and the presence of the diode bridge is eliminated.

II. DESCRIPTION OF PROPOSED SYSTEM

We discuss the idea that led to the concept of the proposed techniques. The conventional boost converter is the former choice for PFC applications basically due to its simple structure. However as the power rating increases, the boost converter efficiency is compromised because conduction losses become less due to the current flowing through three semiconductor elements simultaneously in any operating stage.

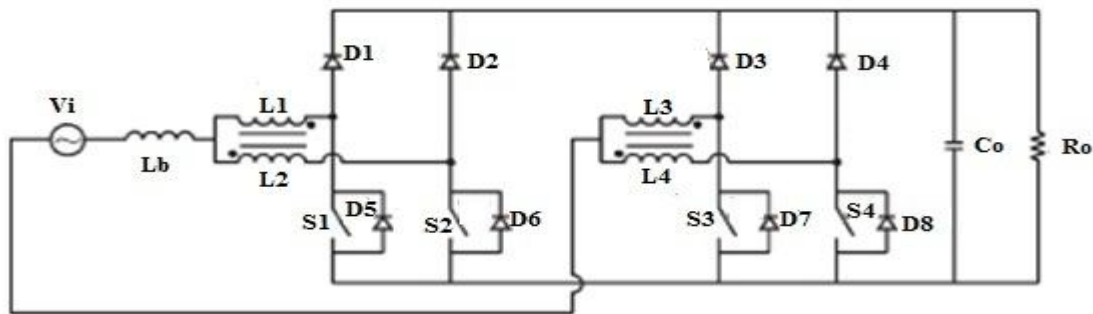


Fig.1. Proposed boost rectifier of 3SSSC

The aim is to increasing the efficiency of the conventional boost converter and single-phase bridgeless boost rectifiers also referred to as dual-boost converters were introduced in respectively. Conduction losses are then minimized by reducing the number of semiconductor devices that conduct current from the source to the load. However, it must be mentioned that this feature also eliminates the possibility of short circuit through one leg due to eventual malfunctioning of the main switches. The have also to be made between complexity and reduced conduction losses when considering the conventional boost converter or the aforementioned bridgeless topologies. The 2SSC is composed basically by the association of one controlled switch and one diode of course; the aforementioned bridgeless topologies employ two 2SSCs. If they are replaced by two 3SSCS instead, the topology shown in Fig. 1 will result, which is the scope of this work. the advantage of the proposed approach of the three state switching cell

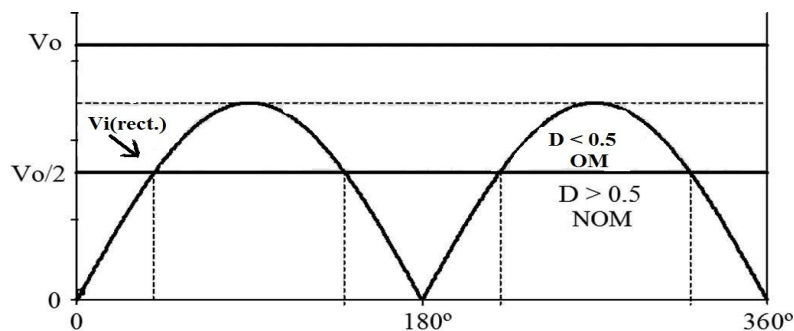


Fig.2. operating mode of Proposed boost converter

Two operating modes regarding the main switches can be obtained for the proposed techniques. If the duty cycle D is higher than 0.5 occurs, where two switches remain turned on at the same time. Otherwise, if $D < 0.5$, the converter operates while only one switch remains turned on. This situation is defined by the comparison between the

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

rectified line voltage V_i and the output voltage V_o as a function of the duty cycle, as shown in Fig. 2, for one period of the input voltage. It must also be mentioned that the input current ripple becomes null when $D = 0.5$, what represents the transition between OM and NOM

a. Operation in ($D < 0.5$)

CCM The converter operation can be defined according to four operating stages as shown in Fig.3. In order to describe the operating stages the positive half cycle the line voltage is considered. The behaviour of the converter during the negative half cycle is analogous the switches S_3 and S_4 , boost diodes D_3 and D_4 , and antiparallel diodes D_5 and D_6 are supposed to replace their respective counterparts S_1 and S_2 , D_1 and D_2 and D_7 and D_8 .

First stage: The switch S_1 is turned on switch S_2 is turned off. The current through the boost inductor is divided into two parts. The first one flows through L_2 and D_2 with energy being store to the load. The second one flows through L_1 and S_1 . Current sharing is maintained to the turn's ratio for L_1 and L_2 is the same. The current through L_b increases linearly. Windings L_1 and L_2 have the same impedance and the output voltages across V_o .

Second stage: Switch S_1 and S_2 is turned off. The voltage across inductor L_b is inverted. Here Diode D_1 is forward biased and D_2 remains conducting. The energy stored in L_b during then transferred to the load. The current flows through parallel Inductor L_1, L_2 , according to the same polarity. This stage when S_2 is turned on.

Third stage: This stage is similar to the first one, although switch S_2 is turned on and S_1 turned off. Diode D_1 keeps conducting and D_2 is reverse biased.

Fourth stage: This stage is similar to the second one.

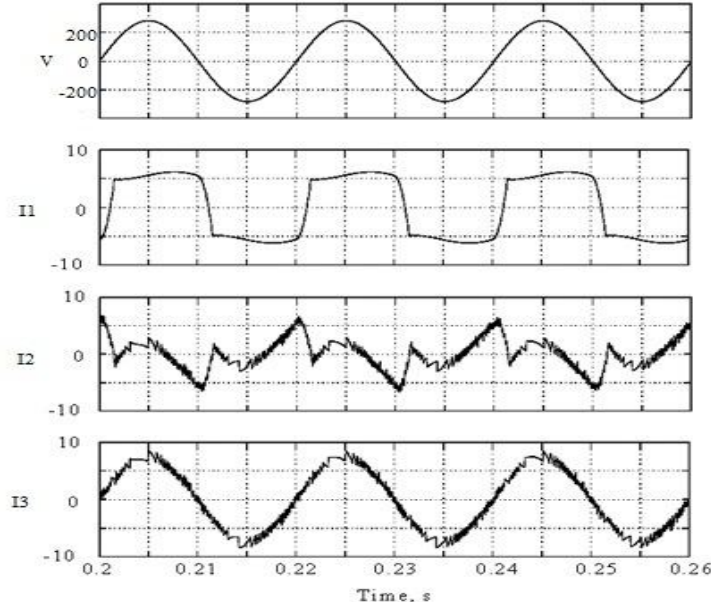


Fig.3.Theoretical waveform of continuous conduction mode

DCM This conduction mode occurs when the current through inductor L_b becomes null there will be no energy transfer from the input source to the load. The converter operation can be defined as to six operating stages.

First stage: They are identical to common conduction mode respectively the first and second stages

Third stage: Boost diodes D_1 and D_2 are reverse biased and main switches S_1 and S_2 are turned off. The current through L_b reaches zero, and energy transfer from the source to the load is increased. This stage finishes when S_2 is turned on.

Fourth stage : They are identical to the third and fourth stages respectively.

Sixth stage : This stage is identical to the third one.

CRM This mode is also called boundary conduction mode because it represents the operation between CCM and discontinuous-conduction mode. The analysis of the critical conduction mode is based on the study developed for the previous conduction modes.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

b. Operation in ($D > 0.5$)

CCM The converter operation can be defined according to four operating stages as shown in Fig.2. The operating stages, the positive half cycle of the line voltage is considered. The behaviour of the converter during the negative half cycle is analogous, although switches S_3 and S_4 , boost diodes D_3 and D_4 , and antiparallel diodes D_5 and D_6 are supposed to replace their respective counterparts, S_1 and S_2 , D_1 and D_2 , and D_6 and D_7 .

First stage : Initially during the positive half cycle of the line voltage, switch S_1 and S_2 is turned on. Boost diodes D_1 and D_2 are reverse biased. The current flow through boost inductor through L_1 and S_1 , and the remaining one flows through L_2 and S_2 . Considering the current flows through L_3 - D_7 and L_4 - D_8 . By adopting the same turns ratio for L_1 and L_2 , current sharing is maintained.

Second stage : Switch S_2 is turned off, and S_1 remains turned on. The voltage across the boost inductor is inverted. Diode D_2 is forward biased while D_1 is reverse biased.

Third stage: This stage is similar to the first one switch S_2 will be turned on while switch S_1 remains also turned on. Boost diodes D_1 and D_2 are also reverse biased.

Fourth stage: This stage is similar to the second one although switch S_1 is turned off while switch S_2 remains turned on. Diode D_1 is forward biased, whereas D_2 is reverse biased. In this way energy is transferred from the input source and the boost inductor to the load

DCM This conduction mode occurs when the current through inductor L_b becomes null during half of the switching period. The converter operation can be defined according to six operating stages as while the respective main theoretical waveforms are shown in Fig.3.

CRM The analysis of the CRM is based on the study developed for the previous conduction modes and is required the static characteristic of the converter operating is determined. The current through L_b is equal to zero for a single time instant. The current ripple through Inductor L_b .

III. BLOCK DIAGRAM

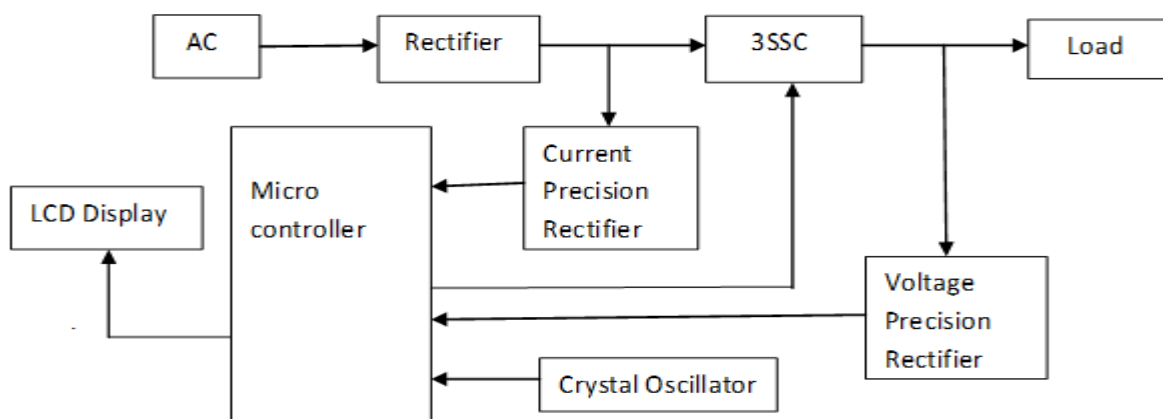


Fig.3. Block diagram of 3SSC

a. Three State Switching Cells

The Fig.4. show the block diagram of Three state switching cells. The current stress through each main switch is equal to half of the total output current, allowing the use of switches with lower current rating. Part of the input power, 50% is directly transferred to the load through the diodes and the coupled inductors (autotransformers) and not through the main switches. As a consequence conduction and switching losses are reduced. This is the main

difference between the functionality of this approach and that of the interleaved boost topology. The use of the 3SSC allows the parallel connection of switches and therefore in expensive power devices and drives can be used. Energy is transferred from the source to the load during most part of the switching period, which is a distinct characteristic of

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

the proposed converter since in other boost type converters, it only occurs during half of the switching period. The drive circuit of the main switches becomes less complex because they are connected to the same reference node.

B. DC link model

The line commutated inverter is a conventional phase-controlled converter operating with fixed maximum possible firing angle. Since the utility line voltage is fixed, the voltage at the dc terminals of the phase controlled bridge is also fixed[1]. The equation for the average current in the dc link can be written as

$$I_d = (V_o + V_{cd})/r_s \quad (1)$$

where

r, is the circuit resistance,

Vo and Vcd are the average voltages of rectified.

The dc link current id is inverted by the line commutated inverter and forced to the utility line, feeding the power generated by the HF rectified source in to the utility line. For continuous current operation,

C. Power quality Issues

Approximately 70 to 80 of all power quality related problem can be attributed to fault connection and wiring. Power Frequency disturbance electromagnetic interference, transient, harmonics and low power factor are related to the source of supply and load. Among these events, harmonics are the most dominated one. The effects of harmonics on PQ are described. According to the IEE standard harmonics power system be two different methods

- One is the limit of harmonics voltage that the utility can system at the point of common coupling.
- The another limits of harmonics voltage that the utility can supply any cost at point of common coupling.

A impact of power quality are usually divided into three board categories direct, indirect and social in survey power quality cost due to effects of voltage dips and swells, short interruption, long interruption, harmonics and transient, flickers and electromagnetic compatibility

IV. SIMULATION RESULT

The ac–dc boost-based topologies have been employed over the years for PFC applications, where low-distorted input currents and near-unity-PFC operation are desired is-sues. Moreover, several dedicated control techniques have also been proposed. typical strategies are hysteresis control, average-current-mode control peak current control. more recently, on-cycle control and self-control have also been employed.

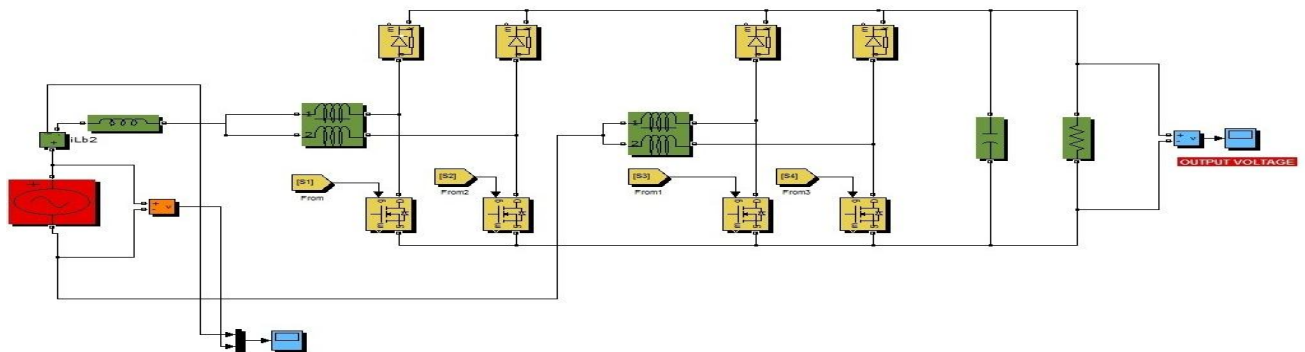


Fig.5.Simulation Diagram of 3SSC

The Fig.5 shows the voltage and current of Three state switching cells. To emulate the behaviour of a pure resistance average current-mode control is one of the most popular techniques mainly due to the availability of dedicated commercial and will be chosen for this work. An experimental type was built, whose picture is shown in Fig. 6 PFC. The experimental was evaluated over a wide load range, and the efficiency curve of the converter operating at

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

30 kHz .

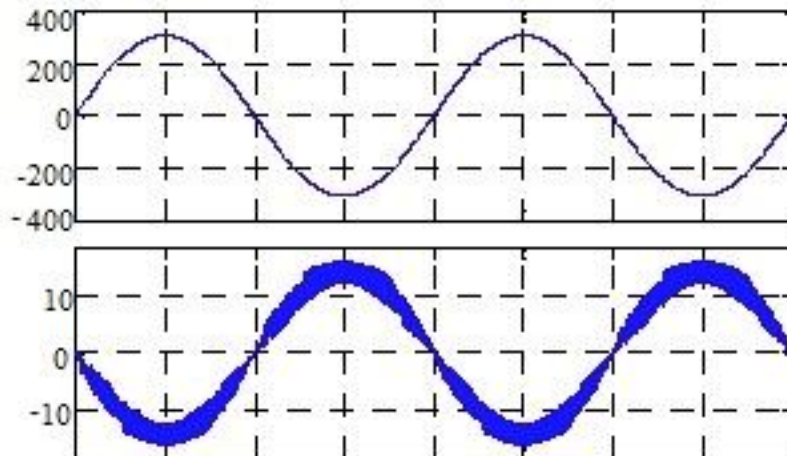


Fig.6.voltage and current vs time

First, one can see that the peak current through the switch is half that of the input current. Moreover, it is possible to notice that, depending on the input voltage half cycle, the current flows through either the main switch or the antiparallel diode. That is the MOSFETs operate at high frequency according to the pulse width modulation, while the diodes operate at low frequency. The same behaviour is expected for the remaining switches.

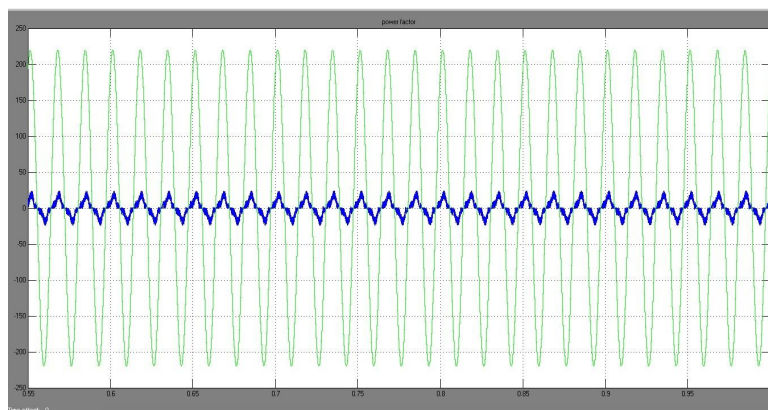


Fig.5.voltage vs time of output voltage

The fig .7 shows the output voltage energy transfer from the source to the load occurs during almost the entire switching period for the 3SSC topology. On the other hand, in the conventional boost converter, it does only occur during part of the switching period, namely, when the main switch is off and the output capacitor is charged. It certainly contributes to the reduction of the current peak in the switches, causing efficiency to increase. The efficiency is higher than 95% over the entire output power range, demonstrating the merit of the proposed converter. This is not observed in typical boost topologies that are not based on the 3SSC due to the aforementioned reasons.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 6, May 2015

V. CONCLUSION

Using Three State Switching Cells the bridgeless Single Phase boost converter are presented. In the bridgeless topology, the conventional boost converter are minimized the conduction losses become instead of three as Conduction boosts converter and two power semiconductor current flows. The current is distributed among semiconductors in the presents of three state switching cells. The voltage and current levels are decreased becomes the number of semiconductors are increased; switches and isolated drive are not required. The high power level and analogous to the interleaved boost converter applications are used here.

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