

# Implementation of Barrel Shifter using Adiabatic logic

Debika Chaudhuri, Rashmi Kumari

Department of Electronics & Communication Engineering, Modern Institute of Engineering & Technology,  
Hooghly, West Bengal, India

**ABSTRACT:** This paper represents the implementation of a barrel shifter in different adiabatic logic. Barrel shifter can be effectively used to perform the arithmetic shift, logical shift and circular shift operations. From the power, and delay comparison for a 4 bit Barrel shifter using ECRL, MECRL, and PFAL logic. From the table it is observed that the power consumption and the delay is minimum in PFAL logic.

## I. INTRODUCTION

For the rapid increase in the usage of electronics devices, it is necessary to find out an energy and area efficient integrated circuit design. For this researcher's develop a few VLSI logic design with low power consumption. Since power consumption is proportional as the square of the supply, voltage scaling is important. For past last few decades' adiabatic logic is used as effective energy recovery logic for low power applications. This paper put emphasizes on the design of a barrel shifter, following different adiabatic logic, using 2:1 MUX as the basic building block. The implemented structure can be widely used in arithmetic and logic units of processors as it is capable of rotating or shifting data in a single cycle. It is basically a combinational logic circuit having n inputs and n outputs along with the control inputs specifying shift between input and output. n number of n-bit MUX is required for the design and implementation of an n-bit barrel shifter. MUX based barrel shifter are designed using 4n:1 MUX trees, which are constructed by the basic building block of 2:1 MUX. As the power consumed by MUX trees is quite significant so it should be considered and so it is important to minimize power dissipation of MUX trees within low-power designs.

## II. DESIGNING OF MULTIPLEXER CIRCUIT

### A. MULTIPLEXER USING ECRL LOGIC

The advantage of ECRL is logic is achieved by eliminating large PMOS from each logic function and all functions are implemented using NMOS only while the PMOS serve as the pull-up devices only. ECRL circuit may be divided into two parts: One differential latching circuit realized by the cross-coupled PMOS transistors and one cascaded complementary logic array realized with a NMOS logic tree as shown in Figure 1.

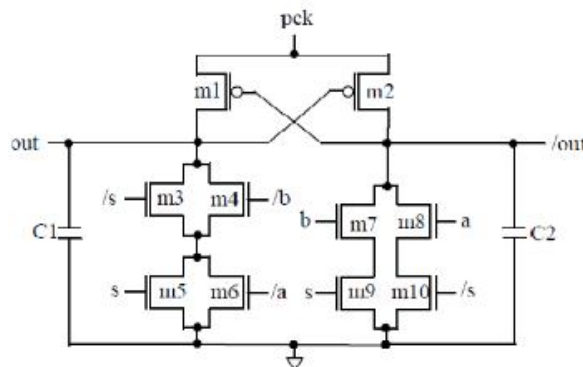


Fig.1 2:1 Mux Using ECRL Logic

**B. MULTIPLEXER USING MECRL LOGIC**

This is the modified version of ECRL logic and it is achieved by inserting two NMOS in addition with the ECRL logic to reduce the power consumption. This is shown in Figure 2.

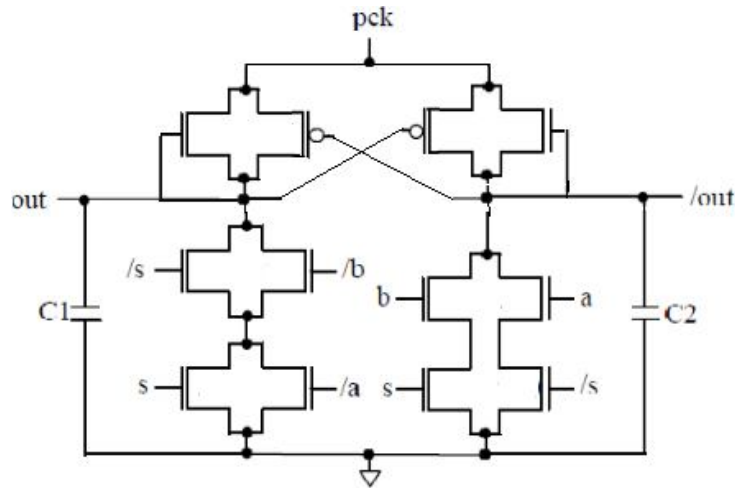


Fig.2 2:1 Mux Using MECRL Logic

**C. MULTIPLEXER USING PFAL LOGIC**

An adiabatic PFAL 2:1 MUX (Figure 3) can be implemented by the function  $F = (A) (/S) + (B) (S)$ . When the select (S) signal is low, it outputs the signal A and when the select (S) signal is high, it outputs the signal B.

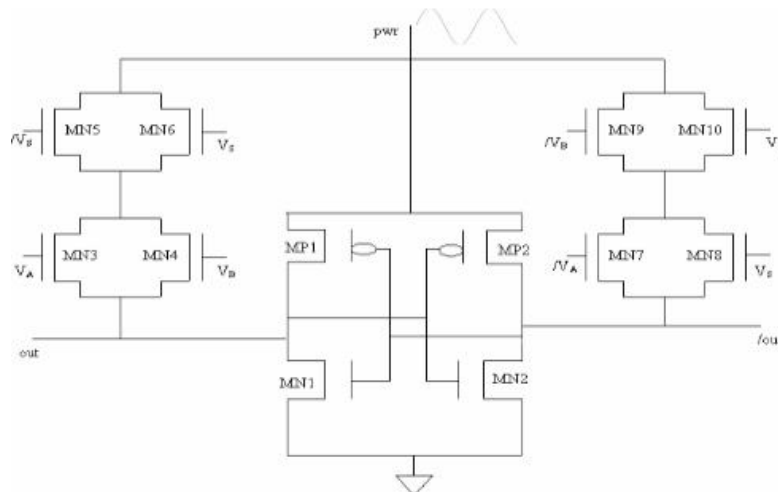


Fig. 3 2:1 Mux Using PFAL Logic

**III. BARREL SHIFTER**

Barrel shifter can be effectively used to perform the arithmetic shift, logical shift and circular shift operations. Figure 4 depicts a 4 bit logarithmic barrel shifter. For the elimination of the decoder circuitry, design simplification and less area requirement it is most effectively used in modern circuitry design.

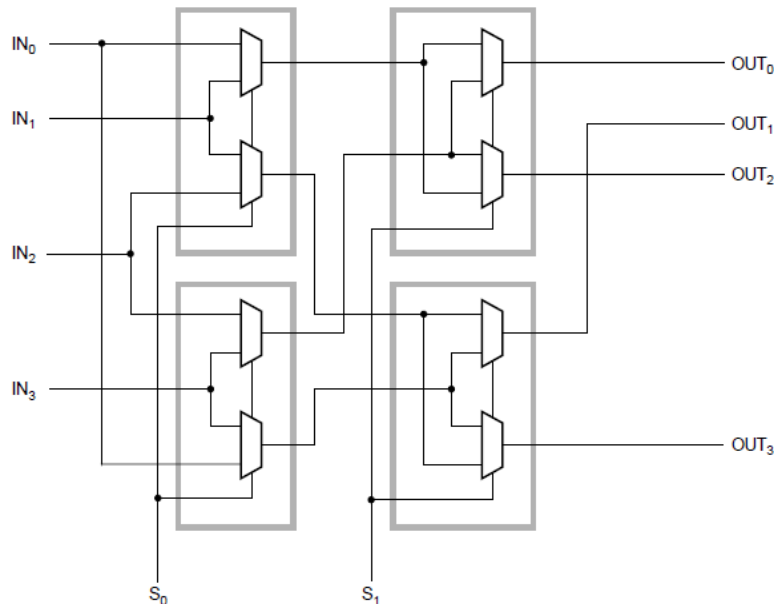


Fig.4 4 bit Barrel shifter

For a 4 input barrel shifter 4 data inputs, 4 data outputs and 2 control inputs are required. If the barrel shifter must be fully combinational, it is better to decompose it into 2-stages. A nbit Logarithmic Barrel Shifter contains  $\log_2(n)$  stage controlled by a control bit where the  $i$ th stage either shifts over  $2i$  bits or leaves the data unchanged. If the control bit is set to 1 then the input data will be shifted in the associated stage else remaining unchanged. The proposed work presents the designs of reversible bidirectional arithmetic and logical barrel shifter that can perform logical or arithmetic shifts and rotation.

#### IV. SIMULATION RESULTS

Table I gives the power, and delay comparison for a 4 bit Barrel shifter using ECRL, MECRL, and PFAL logic. From the table it is observed that the power consumption and the delay is minimum in PFAL logic.

TABLE I  
COMPARISON RESULT

ECRL		MECRL		PFAL	
Power in W	Delay in S	Power in W	Delay in S	Power in W	Delay in S
5.37E-05	5.39E-09	2.48E-05	5.31E-09	1.38E-05	4.77E-09

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