

Design of a Low Power Class AB Two-Stage Op-Amp with Symmetrical Slew Rate

V.V.S.Madhuri¹, D. Raja Ramesh²

M.Tech, Department of ECE, MVGR College of Engineering, Vizianagaram, A.P, India¹

Assistant Professor, Department of ECE, MVGR College of Engineering, Vizianagaram, A.P, India²

ABSTRACT: The operational amplifier is perhaps the most useful integrated device in existence today. It is widely used in analogue computers, simulation systems and in a variety of electronic applications such as filtering, buffering and comparison of signal levels. In this paper, the different schemes of power-efficient class AB two-stage op-amps using a current replication branch and adaptive loads were analysed. A CMOS class AB two-stage op-amp is proposed by modifying the existing power efficient class AB two-stage op-amps for low-power, optimum gain and symmetrical slew rate operation. In the proposed class AB two-stage op-amp power is significantly reduced. The circuits presented in this work are designed in 130nm technology by using mentor graphics backend tools with a supply voltage of 3.3V. Proposed class AB two-stage op-amp is compared with existing power efficient class AB two-stage op-amps and the results are discussed in detail.

KEYWORDS: Class AB operation, CMOS analog integrated circuits, Operational amplifiers, Symmetrical slew rate.

I. INTRODUCTION

The designing of op-amps puts new challenges in low power applications with reduced channel length devices. Advancements which have appeared recently through new techniques and technologies, give us multiple alternatives in implementations. Involvement of Design Automation (DA) tools in analog and mixed signal design is still not matured as it is in the digital design domain. Accommodation of short channel effects in DA for mixed-signal design is also a challenging task for EDA designers. Designing of two-stage op-amps is a multidimensional-optimization problem here optimization of one or more parameters may easily result into degradation of others. In single-stage op-amps achieves highly symmetrical slew rate by using different efficient schemes. A drawback of a single stage op-amp is that relatively low open-loop gain(AOL). Since the output cascading transistors is to increase the output resistances(R_{out}) would seriously limit the maximum output current and the slew rate enhancement factor. In the conventional class-A two-stage Miller-compensated op-amp fig. 1(a) is characterized by a highly asymmetrical slew rate with large positive slew rate and much lower negative slew rate. This lower negative-slew rate is due to the output transistor (MoN) acts as a dc current source with value $2I_B$ and increase the static power dissipation. To avoid this limitation many class AB two-stage op-amps have been reported. Most of them feature is relatively modest effective slew rate improvement and require additional complex circuitry, and non negligible additional static power dissipation or increased supply requirements. This decreases their current efficiency. In fig. 1(b) achieves class AB operation with additional small hardware. It consists of a large resistive R_{large} and small capacitor C_{bat} , this combination operates as an open battery that transfers ac variations taking place at the gate of MoP to the gate of MoN transistors. The output stage operates as a push-pull amplifier and provides dynamic class-AB operation with large positive and negative output currents. This does not increase power dissipation or supply requirements but operates only for dynamic changes with frequencies.

II. EXISTING CLASS AB TWO-STAGE OP-AMP

A. Op-Amp with Current Replication Branch

To achieve class AB operation, the output transistor can be transformed into an active amplifying device by simply adding a current replicating branch formed by M2R and MoNR as shown in fig.1(c). This transfers current variations I_A in M1-M2 to the output transistor MoN and increases the maximum positive output current by $2I_B$. The maximum negative current is still limited to a value of $2I_B$. The current replicating branch does not require additional compensation circuit. Since the node V_x with gain in the current replicating branch is gate to the drain of MoN, and at the higher frequencies miller compensation causes MoP to behave as low impedance load. This reduces the gain between the gate of MoN and the op-amps output terminal to closely a unity value. The current replicating branch has small dimensions reducing area and static power dissipation. In order to achieve large negative output currents, a non-linear adoptive load can be used. This modification is seen in another circuit.

B. Class AB Two-Stage Op-Amp Using Adaptive Loads

By using an adaptive load at the input side in the circuit we can achieve class AB operation efficiently. Two different alternatives are shown in fig. 1(d) and fig. 1(e). In both cases, the adaptive loads manoeuvre the large variation of output resistance of transistors between triode and saturation regions in quiescent conditions. In both schemes a current increase in I_A causes transistors to go in triode region and to develop large drain-source voltages. These changes cause large currents flow in the output transistors MoP and thanks to the current replicating branch, MoN.

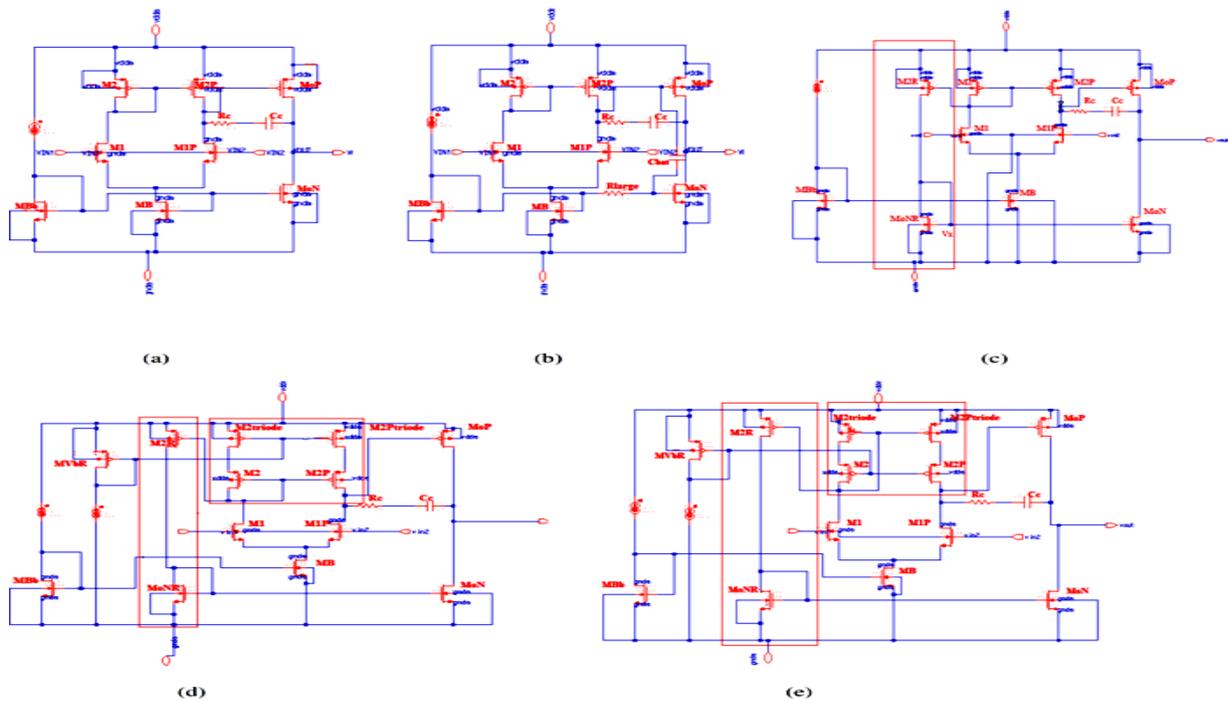


Figure 1: (a) Conventional two-stage Miller op-amp. (b) Free-class AB op-amp. (c) Push pull op-amp with current replication branch M2R, MoNR. (d) Class AB two-stage op-amp with current replicating branch using adaptive load II at the input stage. (e) Class AB two-stage op-amp with current replicating branch using adaptive load I at the input stage.

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A bias voltage with value $V_{b_{triode}} = V_{ss} + V_{gs} + V_{DSsat} = V_{TH} + 2V_{DSsat}$ is required at the gate of MoNR. Where $V_{DSsat} = V_{gs} - V_{th}$ is the minimum V_{ds} voltage to operate in saturation region. This $V_{b_{triode}}$ leaves a quiescent drain-source voltage for MoN_{triode} with value V_{DSsat} , which causes MoN_{triode} to operate at the boundary between the triode and saturation regions. The circuit of fig. 1(f) is denoted as operational amplifier with current replicating branch and adaptive loads.

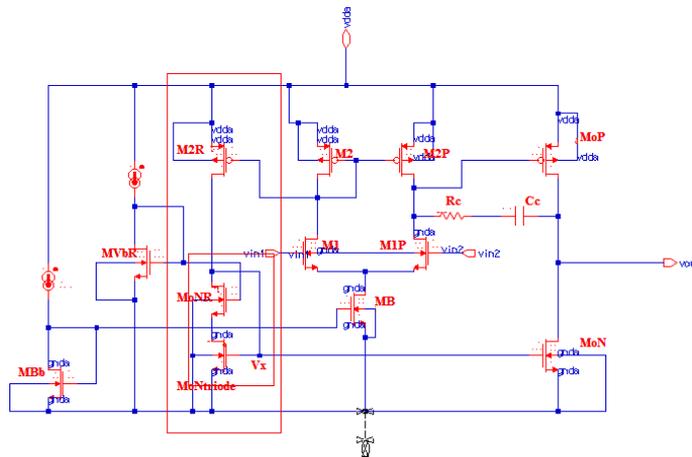


Figure 1(f): Class AB two-stage op-amp with current replicating branch sing adaptive load at the input stage.

III. PROPOSED CLASS AB TWO- STAGE OP-AMP

A CMOS class AB two-stage op-amp is proposed by modifying the existing power efficient class AB two-stage op-amps for low-power, optimum gain and symmetrical slew rate operation. To create low-impedance node, either the length of differential-pair transistor (NMOS) or load transistor (PMOS) is slitted. The compensation capacitor is connected to this low impedance node. In this topology, the differential-pair device NMOS is relaced with split-length device as shown in the fig. 2. To make node A, a low-impedance node, the transistors M_{1t} and M_{1P} must be kept in saturation region and transistors M_1 and M_{1P} must be kept in triode region.

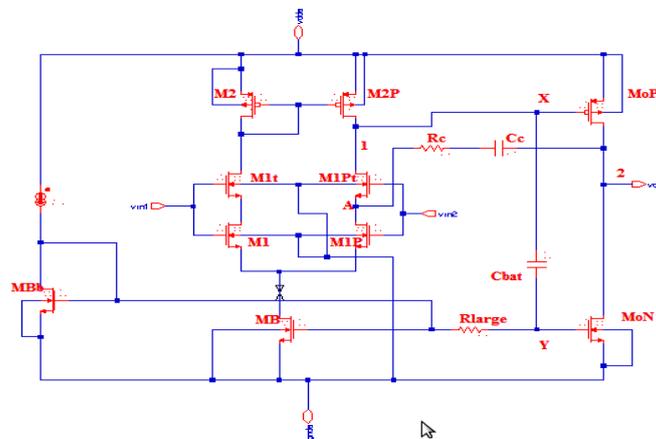


Figure 2: Proposed class AB two-stage op-amp.

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For class AB output stage, a resistor R_{large} which is always in cut-off region. For floating battery, a capacitor (C_{bat}) with small capacitance value is connected to the output of first stage to the gate NMOS of output stage. As the resistor R_{large} is in cut-off the capacitor C_{bat} cannot charge or discharge easily. Hence, the voltage variation transfer occurs from node X to node Y as shown in the above Figure. Thus this setup renders to class AB output stage of the op-amp.

IV. IMPLEMENTATION OF SAMPLE AND HOLD CIRCUIT USING DIFFERENT OP-AMPS

Sample-and-hold (S/H) circuits are critical in converting analog signals to digital signals. The behaviour of the S/H is analogous to that of a camera. Its main function is to "take a picture" of the analog signal and hold its value until the ADC can process the information. It is important to characterize the S/H circuit when performing data conversion. S/H circuits have four major components, they are input amplifier, energy storage device (capacitor), output buffer, and switching circuits are common to all S/H circuits. The energy-storage device, the heart of the S/H, is a capacitor. The input amplifier buffers the input by presenting high impedance to the signal source and providing current gain to charge the hold capacitor. In the hold mode, the switch is opened, and the capacitor retains the voltage present before it was disconnected from the input buffer. The output buffer offers high impedance to the hold capacitor to keep the held voltage from discharging prematurely.

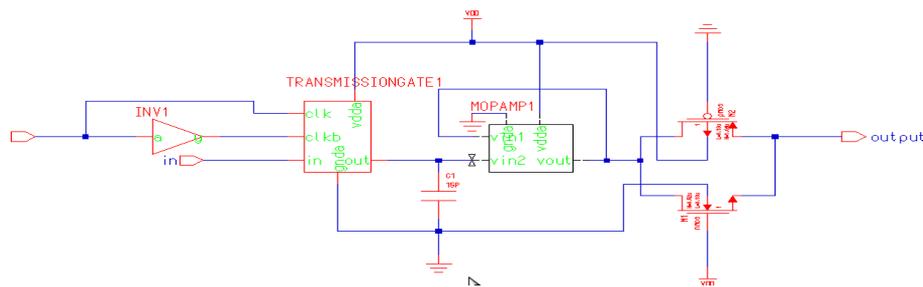


Figure 3: Implementation of sample and hold circuit using proposed op-amp.

As with op-amps, there are numerous S/H architectures, and we will examine a few of the most popular ones. The simplest S/H structure is shown in fig. 3, which is implemented by using an inverter, a transmission gate and proposed op-amp. The input signal is buffered by an amplifier and applied to the switch. The input buffer may either be open- or closed-loop and may or may not provide gain. The switch can be CMOS, FET, or bipolar (using diodes or transistors) and is controlled by the switch driver circuit. The signal on the hold capacitor is buffered by an output amplifier. This architecture is sometimes referred to as open-loop because the switch is not inside a feedback loop. Notice that the entire signal voltage is applied to the switch; therefore it must have excellent common-mode characteristics.

V. SIMULATION RESULTS

All the simulation are made using MENTOR GRAPHICS HEP1, Generic 130nm. All the schematic are drawn in the PYSIS schematic editor. Initially, from fig. 1(a) to 1(f), fig. 2 and fig .3 are designed in the schematic editor. The AC and transient response of the designed op-amp models is simulated. For sample and hold circuit transient analysis is performed.

A. AC Analysis.

In Ac analysis, an ac signal is applied to both the terminals of the input stage. With the help of AC analysis we can estimate several performance parameters like gain, slew rate, -3dB gain, gain bandwidth, phase margin etc. They are estimated using DC operating point.

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B. Transient Analysis.

1. Slew Rate: A step from ground to voltage supply is applied to the non-inverting terminal of the input stage with the unity feedback configuration. The slew rate simulation is carried out performing a transient analysis using a pulse waveform. This step response is used for calculation of positive and negative slew rate value for the op-amp. Slew rate (SR) is defined as the maximum rate of change of output voltage per unit of time and is expressed as volt per second.
2. Voltage Amplification: A transient simulation of the amplifier is an open loop gain configuration with the sinusoidal input at both the input terminal.

In order to compare the proposed op-amp with the existing op-amps, all circuits have been simulated in 0.13-nm CMOS technology with $V_{DD} = 3.3V$, fig. 5 shows the comparison of different op-amps in terms of number of transistors, power dissipation. Table summarises the performance of proposed class AB two-stage op-amp and Table 2 compares the performance of the proposed op-amp with the existing op-amps.

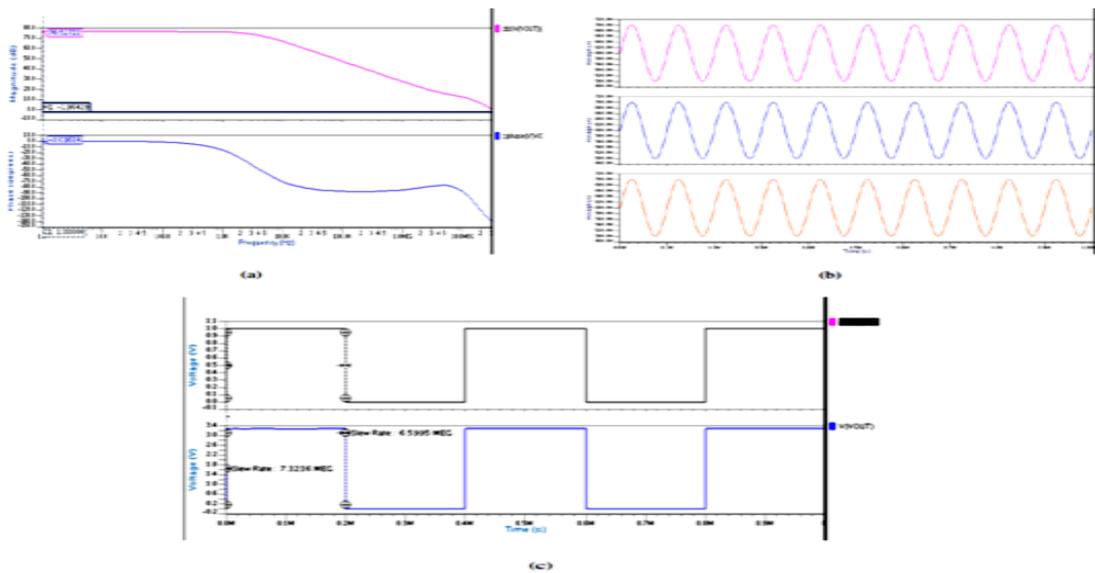


Figure 4: (a) AC analysis of proposed class AB two-stage op-amp. (b) Output and input signals of proposed class AB two-stage op-amp. (c) Slew rate for proposed class AB two-stage op-amp.

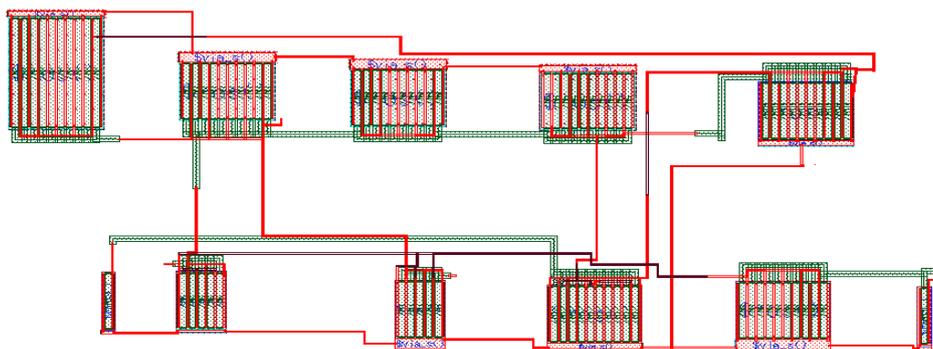


Figure 4(d): Layout of proposed class AB two-stage op-amp.

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TABLE 1: Performance of proposed class AB two-stage op-amp.

Specification	Value
Technology	130nm (CMOS)
Supply voltage(V)	3.3
Gain(dB)	76
Delay(ns)	10
SR ⁺ (V/us)	7.3
SR(V/us)	6.9
Power dissipation(Mw)	1.31
Offset voltage(V)	0.6
Number of transistors	10

TABLE 2: Comparison of different op-amps.

Specifications	Figure 1(a)	Figure 1(b)	Figure 1(c)	Figure 1(d)	Figure 1(e)	Figure 1(f)	Figure 2
Technology	130 nm	130 nm					
Supply(V)	3.3	3.3	3.3	3.3	3.3	3.3	3.3
Gain(dB)	74	74	75	76	76	74	76
PM(°)	59	-	60	55	55	-	-
Offset voltage(V)	0.59	0.59	0.6	0.6	0.6	0.59	0.6
-3db gain(dB)	71	71	72	73	73	71	73
SR ⁺ (V/us)	92	67	79	71	75	94	7.3
SR(V/us)	6.1	6.3	7.6	36	10.5	65.7	6.9
GB(MHz)	32	32	33	34	34	31	35
Transistors used	8	8	10	13	13	12	10
Delay(ns)	12.8	7.6	8.2	8.7	3.6	21.3	10
Power dissipation(mW)	1.38	1.38	1.46	1.86	2.32	2.21	1.31

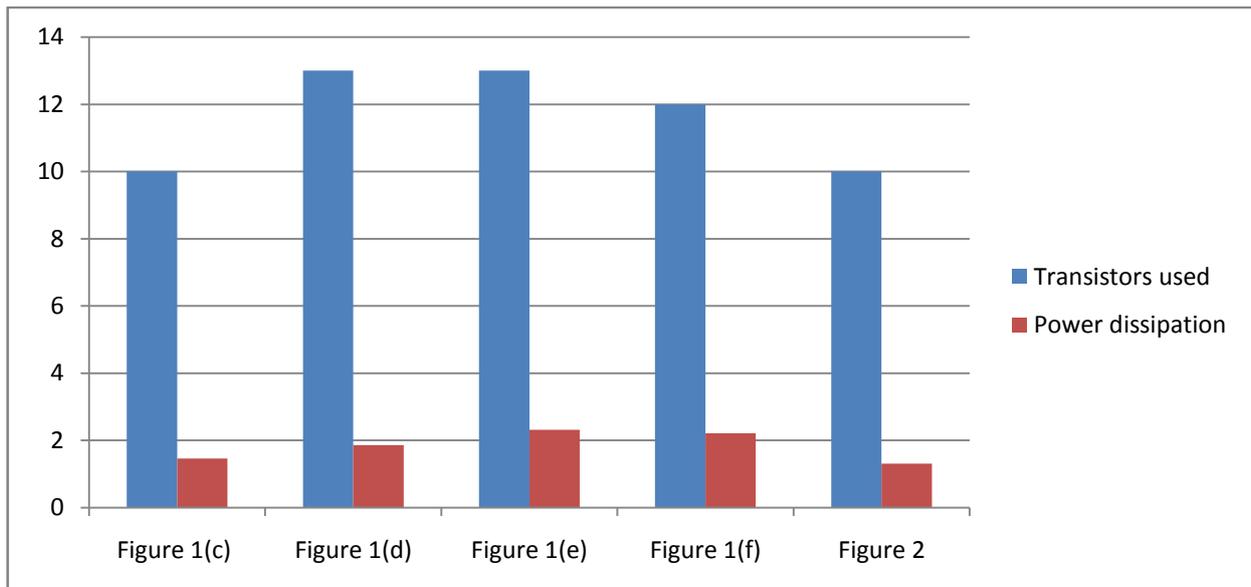


Figure 5: Comparison of different op-amps.

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The sample and hold circuit which is specified in fig. 3 is designed in the schematic editor and the transient response of the designed models are simulated for time period of 5ns.

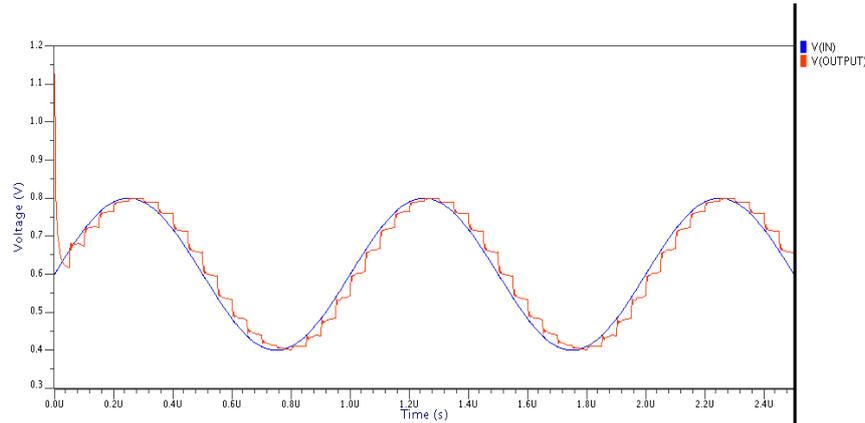


Figure 6: Output waveforms of S/H circuit implemented with proposed class AB two-stage op-amp.

The output waveform of S/H circuit which is implemented with the proposed class AB two-stage op-amp is shown in the fig. 6. Table 3 summarises the performance of S/H circuit using different op-amps

Table 3: Performance of S/H circuit using different op-amps

Circuits	Sample time(ns)	Hold time(ns)
S/H design using conventional two-stage Miller op-amp.	52.3	98.86
S/H design using free-class AB op-amp	56.2	101.32
S/H design using push pull op-amp with current replication branch	52.63	97.32
S/H design using class AB two-stage op-amp with current replication replicating branch using adaptive load II at the input stage	53.28	100.65
S/H design using class AB two-stage op-amp with current replication replicating branch using adaptive load I at the input stage	52.94	99.26
S/H design using class AB two-stage op-amp with current replication replicating branch using adaptive load at the input stage	52.22	100.73
S/H design using proposed class AB two-stage op-amp	53.32	104.44

VI. CONCLUSION

In this paper, different schemes of power-efficient class AB two-stage op-amps using a current replication branch and adaptive loads have been experimentally tested. Based on the class AB op-amp structure a new op-amp with low-power capability was proposed in order to achieve optimum gain and symmetrical slew rate. The circuits presented in this thesis are designed in 130nm technology by using mentor graphics backend tools with 3.3V supply voltage at 27°C temperature.

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