

### **Engineering and Technology**

(An ISO 3297: 2007 Certified Organization) Vol. 4, Special Issue 13, December 2015

# Analysis and Implementation of PV Cell based thirteen level Multilevel Inverter with Carrier PWM Technique

K.Eswaramoorthy<sup>1</sup>, S.Vijay<sup>2</sup>

Assistant Professor, Dept. of Electrical and Electronics Engineering, Sasurie College of Engineering, Tirupur,

Tamilnadu, India<sup>1&2</sup>

**ABSTRACT**: Currently, multilevel inverter configuration is paid more attention by the industries due to variable output voltage, low distorted waveform, and required low switching frequency. The various topologies of multilevel inverter arrangement are analyzed and implemented in literature with lower levels of output waveform. In order to reduce the distortion in the output waveform different PWM control strategies for multi level inverter are to be analyzed. In this paper PV solar array based input of thirteen-level inverter with a carrier based pulse width-modulated (PWM) control scheme. To verify the proposed techniques by simulation is done in *MATLAB / SIMULINK*.

**KEYWORDS:** multilevel inverter, multi carrier modulation system, pulse width-modulation (PWM), total harmonic distortion (THD).

#### I. INTRODUCTION

Power quality problems lead to unplanned downtime, wasted resources and higher energy costs, yet they can be easily detected in advance by measurement and monitoring, and cured by the application of the most appropriate mitigation techniques. Best of all, the effects can be avoided altogether by good design practices and by choosing the right equipment. If your installation is experiencing any of the following you could have a PQ problems are Computer lock ups, Equipment damage, Blackouts, Flicker, Overheating neutrals, Nuisance tripping, PFC overloading. Stable AC voltages at near nominal values and at near rated frequency subject to acceptable minor variations, free from annoying voltage flicker, voltage sags, frequency fluctuations. Near sinusoidal current and voltage wave forms free from higher order harmonics.

Harmonics in power systems can result in undesirable influence such as Capacitor heating/failure, Telephone interference, Rotating equipment heating, Relay misoperation, Transformer heating, Switchgear failure, Fuse blowing. The main sources of harmonics in power system are static power converters, arc furnaces, discharge lighting and any other load that requires non-sinusoidal current. In order to limit the harmonic current propagation in to the network, harmonic filters are placed close to the source of the harmonic currents. Harmonic filters provide low impedance paths to harmonic currents and thus prevent them from flowing into the power network. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy.

In multilevel voltage source inverters, various pulse width modulation (*PWM*) control schemes have been developed and analyzed so as to control the fundamental voltage and eliminate certain output lower order harmonics, via control of each pulse width. Some of these *PWM* techniques were implemented in real systems and some were published for theoretical interest. Multilevel converters achieve high voltage switching by means of a series of voltage steps, each of which lies within the rating of the individual power devices. One of the most important problems in controlling a multilevel voltage source inverter is to obtain a variable amplitude and frequency sinusoidal output employing simple control techniques.



### **Engineering and Technology**

(An ISO 3297: 2007 Certified Organization) Vol. 4, Special Issue 13, December 2015

#### II. MULTILEVEL INVERTER

Normally, the multilevel inverters (MLI) topologies are categorized based on their structure of power semiconductor devices and functions. The functions of MLI are modulation techniques, number of level output voltage and switching methods. Basic level of inverter configuration is two level and it further named based on their number of level output voltage. The types of MLI based on their configuration and devices are a).Neutral Point Clamped or Diode Clamped MLI, b).Capacitor Clamped or Flying Capacitor MLI and c).Cascaded H-bridge MLI.

The multilevel voltage output is obtained from diode clamped MLI by the series connection of capacitors . In three level diode clamped configuration can be obtain the voltage levels of  $V_{dc}/2$ , -  $V_{dc}/2$  and zero. The diode clamped configuration is not suitable for extended operation, because of more number of clamping diodes, reverse recovery characteristics of diodes and real power flow control problems.

The flying capacitor clamped MLI structure is requires more number of capacitors which is lesser number than the diode clamped configuration and it also provides the balanced the voltage levels. The harmonics are lower value due to efficient power flow control is achieved easily. This configuration is arranged with more number of storage capacitors or batteries which supplies the power during outages. The capacitor charge balancing can be achieved by appropriate selection of capacitors in a circuit. The main con of this configuration is switching frequency and switching losses are too high.

The cascaded H-bridge MLI configuration is achieved by DC sources are connected in series through the Hbridge configuration of power devices. The cons of above two configurations are overcome in this structure. The main advantages are easily implement renewable energy system and control with lesser number of switches. In general, the coupling transformer is no need for the MLI structure and soft switching methods are implemented in order to reduce the harmonics in output voltage.

Mostly, the real power controlling applications the cascaded H-bridge MLI configuration is implemented rather than diode clamped. The flying capacitor clamped MLI is not suitable for reactive power controlling techniques due to voltage balancing problems. So, the cascaded structure is widely used PV system, active power filters, UPFC, STATCOM, DVR etc.

#### **III. MODULATION TECHNIQUES**

The controlling of multilevel inverter is an important issue to improve their performance. To achieve the effective output various control techniques for the multilevel inverter are dealt by the researchers and divided into Pulse Width Modulation, Selective Harmonics Elimination and Optimized Harmonics Stepped Modulation. The modulation techniques mainly categorized as an open loop and closed loop controlling techniques. Open loop controlling methods are classified as Sinusoidal Pulse Width Modulation, Space Vector Modulation and Sigma- Delta modulation. Similarly, closed loop control techniques are classified as hysteresis controller, linear current controller, deat band current controller etc.

In this paper MLI structure in the input of the DC source converter, is collected by the PV array connected to a Cascaded H-bridge Multilevel Inverter. However the utilization of source with cascaded structure to obtain optimization of the PV energy conversion system. The firing signal is given to the input of gate in switches are generated by comparing an inverted sinusoidal waveform (low frequency, f) with two 180 out of phase triangular carriers (with frequency fs). This makes it possible to synthesize which are particularly suited for digital implementation and extent the number of level in output. To eliminate the oscillating components drawn by the non sinusoidal current component and keep the supply current as a sinusoidal waveform. As a result this increases the performance of multilevel inverter which is the target of our paper. The functional diagram of multilevel inverter with solar PV array as an input is shown in Fig. 1 and Fig. 2.



### **Engineering and Technology**

(An ISO 3297: 2007 Certified Organization)

#### Vol. 4, Special Issue 13, December 2015

The PI controller is implemented to control the input side voltage of inverter. The reference voltage is generated and the actual voltage output is required compared which it gives the highest value of the reference current depending on the error got from the reference and the required values. It removes the DC component steady state error in PV array to inverter output. In this paper the reference current is generated in time domain and it analysed generation of triggering pulses for multilevel inverter . This theory is extensively used as it simplicity of the calculations, and uses only algebraic calculation.



Fig. 1.Proposed Block Diagram.

Fig 1. the block diagram consists of input dc voltage or pv panel system, battery, Reference voltage and actual comparative pwm signal estimation system and driver circuit. PWM signal are generated for converter switches to drive the inverter circuit based on the error produced by reference signal and actual system variables. The carrier signals are generated at 2.5MHz frequency. The Fig 2. Shows that the proposed cascaded multilevel inverter with solar array input connected with a non linear load.



Fig 2. Solar Array with Cascaded Multilevel Inverter



### **Engineering and Technology**

(An ISO 3297: 2007 Certified Organization) Vol. 4, Special Issue 13, December 2015



Fig 3.Equivalent circuit diagram of PV Solar cell

$$I_{ph} = I + I_d + I_{sh} \tag{1}$$

$$V_{c} = \frac{AkT_{c}}{s} \ln\left(\frac{I_{ph} + I_{o} - I}{I_{o}}\right) - IR_{s}$$
<sup>(2)</sup>

The equation (1-2) is used to determine the output characteristics of a PV solar cell. Maximum voltage to current transfer linear characteristics of output are achieved by radiation received solar cell is uniform. Practically, non linear characteristics and are significantly influenced by solar radiation, temperature and load condition. To achieve harmonic free output voltage and to obtain amplitude of the fundamental waveform, up to (m-1) oscillation contents can be eliminated from the voltage wave form. Usually, by proper at low frequency operation individual firing angle is given to the input of gate, and filters circuits is used to cut out off the oscillations in the high-frequency operation. The output phase voltage number of levels are defined by m = 2s+1, where s is the number of separate dc sources. To obtain the 11 level phase voltage output waveform with help of 5 solar array input and 5 full bridges. The phase voltage

$$Va = Va1 + Va2 + Va3 + Va4 + Va5$$
 (3)

#### IV. SIMULATION RESULTS AND DISCUSSION

The proposed system is simulated in MATLAB/SIMULINK. It is valuable stating that the output voltage of the PV string arrays has to be selected based on the required nominal voltage and the minimum output harmonics distortion with balanced operation of each cell. The output voltage each level is equal when the power generated by all cell is equal. The effective switching scheme is implemented applied to the cascaded multilevel inverter switches to produce thirteen output voltage levels at 0.89 modulation index. The total harmonics distortion (THD) of inverter output voltage and Harmonic spectrum is as shown in the fig. and Fig 19 respectively. The simulated results of output voltage with appropriate current waveform shapes are in good physical shape within the limits of IEEE standards. The thirteen level ac output voltage waveform is obtained from the proposed system with the PV solar array input. A 120 V, 50 Hz ac voltage is obtained from the proposed system, at 0.89 modulation index. The THD analysis was conducted on 5 cycles of the ac output and the fundamental component value is 12 with THD is 3.58%.



### **Engineering and Technology**

(An ISO 3297: 2007 Certified Organization) Vol. 4, Special Issue 13, December 2015



Fig 4. Simulink model of Gate pulse generation circuit



Fig 5.Output voltage waveform of thirteen level MLI





### **Engineering and Technology**

(An ISO 3297: 2007 Certified Organization)

#### Vol. 4, Special Issue 13, December 2015

#### V. CONCLUSION

In this paper Control method of various multilevel inverter configurations have been analysed and discussed. The cascaded H-bridge multilevel inverter requires less number of devices and high efficiency than the other structures. The output voltage levels of distortion are verified with the thirteen level configurations with PV solar cell input as DC source. The output obtained from the simulations of cascaded H- Bridge MLI increased the output voltage fundamental value and also eliminated the harmonics in the output voltage.

#### REFERENCES

- [1]. S. Daher, Jurgen S., and F. L. M. Autunes, "Multilevel Inverter Topologies for Stand-Alone PV Systems," IEEE Transactionson Industrial Electronics, vol.55, no. 7, pp. 2703-2712, June, 2008.
- [2]. J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel Inverters A survey of Topologies, Controls and Applications," IEEE Transactions on Industrial Electronics, vol.49, no. 4, pp. 724-738, Aug., 2002.
- [3]. Y. H. Liao and C. M. Lai, "Newly-Constructed Simplified Single-Phase Multistring Multilevel Inverter Topology for Distributed Energy Resources," IEEE Transactions on Power Electronics, vol. 26, no. 9, pp. 2386-2392, Sept., 2011.
- [4]. I. Abdalla, J. Corda, and L. Z. Hang, "Multilevel DC-Link Inverter and Control Algorithm to Overcome the PartialShading," IEEE Transactions on Power Electronics, vol. 28, no. 1, pp. 14-18, Jan., 2013.
- [5]. Keith A. Corzine, Mike W. Wielebski, Fang Z. Peng, and Jin Wang, "Control of Cascaded Multilevel Inverters" on power electronics May 2004.
- [6]. L.M.Tolbert, F.Z.Peng and T.G.Habetler, "Multilevel converters for Large Electric Drives," IEEE Transactions on Industry Applications, vol. 35,no.5,pp.36-44, January/February 1999.
- [7]. Jose Rodriguez, Steffen Bernet and BinWu, "Multilevel voltage source converter topologies for Industrial medium voltage Drives," IEEE Transactions on Industrial Electronics, vol.54, no.6, pp.2930-2945, December 2007.
- [8]. Leon M Tolbert and Thomas G Habetler, "Novel Multilevel inverter Carrier based PWM method", IEEE Transactions on Industry Applications, Vol. 35, no.5, pp. 1098-1107, Oct. 1999.