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Design Approach of High Speed & Low CMD Floating Point Multiplier for FFT Processor: A Review

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ABSTRACT: FFT plays an important role in OFDM and DSB processing of the communication system. Of-late low power VLSI design is the enormous challenge for the ICs designers. Speed can be enhanced by the FFT processor of the DSP device. An essential element for constructing the FFT is floating point multiplier. In the previous research floating point multiplier has been designed by using CSA, look ahead carry adder and Vedic multiplication technique. But in this paper floating point multiplier is being constructed with high speed different cross multiplication technique along with Vedic multiplication technique. Generally floating point multiplier is prepared in the form of IEEE 754, 32 bit format. All the experiment and synthesis is done on the advanced XILINX 14.2i ISE 3E Spartan.

KEYWORDS: IEEE-754 floating point multiplier, FFT, CMD, advanced cradle to cradle VM, xilinx14.2i.

I. OBJECTIVE

Purpose of this research paper is to design a low combination path delay floating point multiplier for FFT processor. CMD must be low for high speed digital devices or digital signal processing. The amount of the CMD is always dependent on the number of circuit's elements. Both are proportional to each other. Regarding the multiplication technique, this is done by cradle to cradle Vedic multiplication technique.

II. INTRODUCTION

In the era of new advanced digital technology Fast Fourier Transforms is an important technique for communication and digital signal processing instead of DFT technique. FFT was proposed by Cooley and Tukey to speed up the time computation. Time complexity or the Order of the FFT is $O(\log_r N)$. Where notation O shows the order, r is radix and N is length of the sequence. At the time of designing fast Fourier transforms (FFT) cores, due to the use of multiplexers, memory, or ROMs, there is a substantial increase in power Consumption and area and combinational path delay. Regarding the increase speed and throughput, folding and pipelining methods have been approached by various existing designs. But the demerit of those architectures is the use of multipliers for twiddle multiplications. FFT is one of the most efficient ways to construct the Discrete Fourier Transform (DFT) due to its reduced usage of arithmetic units. DFT is one of those primary tools that are used for the frequency analysis of discrete time signals and to represent a discrete time sequence in frequency domain using its spectrum samples.

The analysis (forward way) and synthesis (inverse way) equations of an N point FFT are given below.

$$X[k] = \sum_{n=0}^{N-1} x[n]W_N^{kn}$$
$$x[n] = \frac{1}{N} \sum_{k=0}^{N-1} X[k]W_N^{-kn}$$

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There are so many ways to design the FFT processor like single memory architecture, dual memory, array architecture and pipeline architecture. Pipelining is the fast and low power consumption technique to design the fast FFT processor. Diagram shows the high speed processor for the FFT which is comprised with buffer memory and processor. This processor's speed can be enhanced by floating point multiplier.

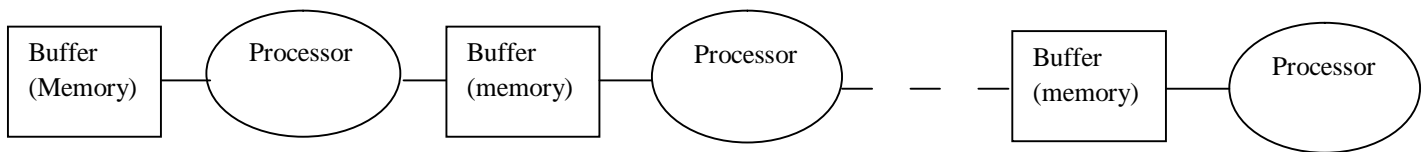
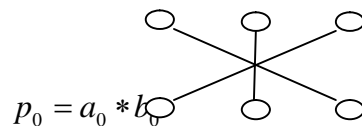


Fig.1. Pipeline architecture for FFT

III. CRADLE TO CRADLE MULTIPLIER

Cradle to cradle method is the best way to computation the multiplication of the binary bits. According to multiplication method number of partial products must be less as possible as. There are so many methods to reduce the partial products but Vedic mathematics is the best way. By using 2 bit multiplier 4, 8, 16, 32, 64 bit multiplier can be designed, this concept is also called cradle to cradle concept. And combinational path delay can be reduced by using this technique. In the same manner by using 3bit multiplier 6, 12, 24 bit multiplier can be constructed. For instance 3bit multiplication is going to be designed.

(a_2, a_1, a_0) & (b_2, b_1, b_0) then product bit will be $(p_5, p_4, p_3, p_2, p_1, p_0)$.



$p_1 =$ Fig.3.1 3 bit Vedic Multiplication

$$p_2 = a_2 * b_0 + a_0 * b_2 + a_1 * b_1 + c_1$$

$$p_3 = a_2 * b_1 + a_1 * b_2 + c_2$$

$$p_4 = a_2 * b_2 + c_3$$

According to above equations number of AND gate and adders can be counted. To design a 3 bit fast multiplier needs three half adder and three full adder. For the high speed and low path delay VLSI device number of gates must be in less counted.

Vedic mathematics is considered as the ancient Indian system of mathematics which is based on sixteen principles or Vedic mathematical formulae known as Sutras. The 'Vedic' word derived from the word 'Veda' which means the store house of all knowledge, this was reconstructed by Shri Bharati Krishna Tirtha. According to him it reduces the cumbersome mathematical calculations into simple ones and finds its applications in computing and DSPs. Multiplier is the key element building block for the FFT and other processor designing. There are so many techniques to design multiplier and types of multiplier but floating point multiplier is much better technique to define the FFT radix-2 design.

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IV. FLOATING POINT MULTIPLIER

Floating point multiplier operationally derived by IEEE-754 standard. Earlier that was used in computer for high speed operation and measurement was in FLOPS. Floating point is mathematical representation of the binary bits. Decimal number is converted in binary number then represent according to IEEE-754 standard. For instance number can be represented as

$$\text{significant} * \text{base}^{\text{exponent}}$$

$$1.3542 = 13542 * 10^{-4}$$

$$\text{sign.mantissa} * \text{base}^{\text{exponent}}$$

$$-9.5 = -1.0011 * 2^3$$

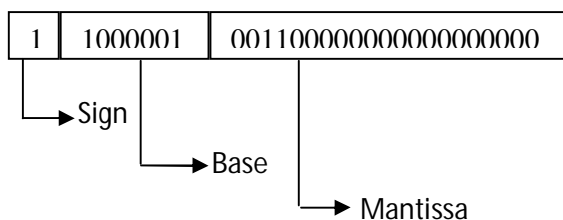


Fig.4.1 Parameters for FT Multiplier

Above block diagram shows the parameters for FT multiplier which is comprised with mantissa, base and sign bit number.

4.1 Parameter's Format

The length of the mantissa bit is 24 bit, 8 bit for base and 1 bit for sign. Regarding the format of floating point number the number in binary must be normalized, the integer part must always be equal to 1. On the other hand the exponent an integer value is not represented in 2 complement but in a biased representation, a bias of 127 is added to the exponent. As the value '0' can be normalized a special representation is reserved for, all bits to zero. Generally the values 0000000 and 1111111 from the exponent field are reserved for special cases and are not biased values. Here 00000000 is used for non normalized values and 11111111 are used for infinity and not a number.

4.2 Floating Point Multiplication

This method is completed in four steps, in the first step non signed multiplication of the mantissa; it must take account of integer part, implicit in normalization. The number of bits result is double the size of the operands that is 48 bits. In the second step normalized of the result; the exponent can be modified accordingly. In the third step addition operation will be performed. And finally in last step sign bit will be calculated.

Bellow diagram shows the multiplication of two floating point numbers. This format is the combination of 24 bit Vedic multiplier which is designed by using cradle to cradle bit multiplier architecture, 8 bit adder and XOR gate for sign bit.

For instance, a multiplication of 2 floating point numbers A and B, where

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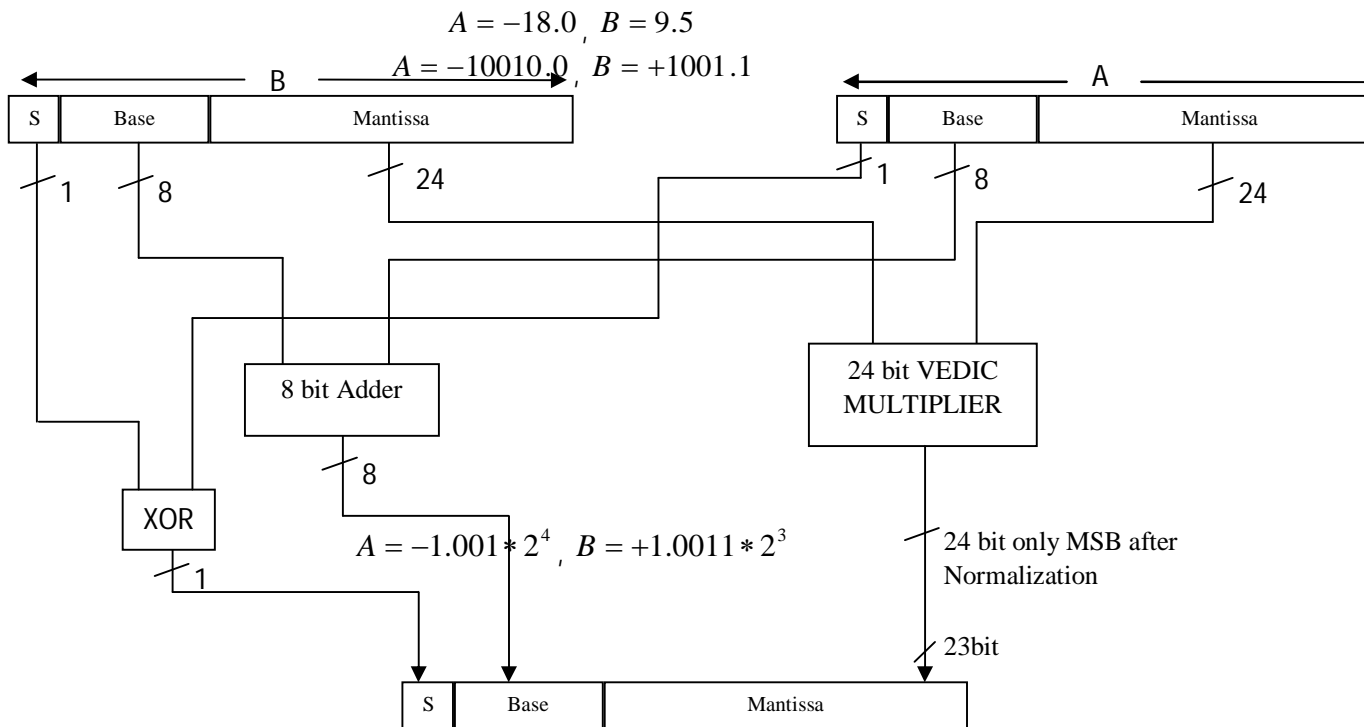


Fig.4.1 Floating Point Multiplier

$$A = 1.10000011.001000000000000000000000$$

$$B = 0.10000010.001100000000000000000000$$

Product output of the multiplier is in 48 bit, but only most significant bits are required. After normalization 1 bit of the most significant is neglected. So, remaining 23 bits will be the result of the mantissa bit. Here in this multiplier RCA adder is used. This is the type of the parallel adder in which full adders are connected in cascading form

V. SOFTWARE REQUIREMENT

In this research paper an advanced analysis tool is used name as XILINX 14.2i. XILINX is a software tool on which propagation delay, number of slices and look up table can be analyzed. The amount of each parameter must be less as possible as. Processing speed of the device of 14.2i is better than 6.2i, 9.2i and 10.1i. the device for circuit analysis is xc6lx20t-2ff323 Vertex 5.

Table.5.1: available parameters for circuit analysis.

Parameter	No of Slices	No of LUTs	No of IOBs
Value	12580	1263	172

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VI. RESULT ANALYSIS & FUTURE SCOPE

Research work is based on combinational path delay (CMD) and high speeds, both are opposite each together. All the calculation of partial products is computed by Vedic mathematics calculation and cradle to cradle multiplication method. Because of this technique propagation delay is reduced than to previous method.

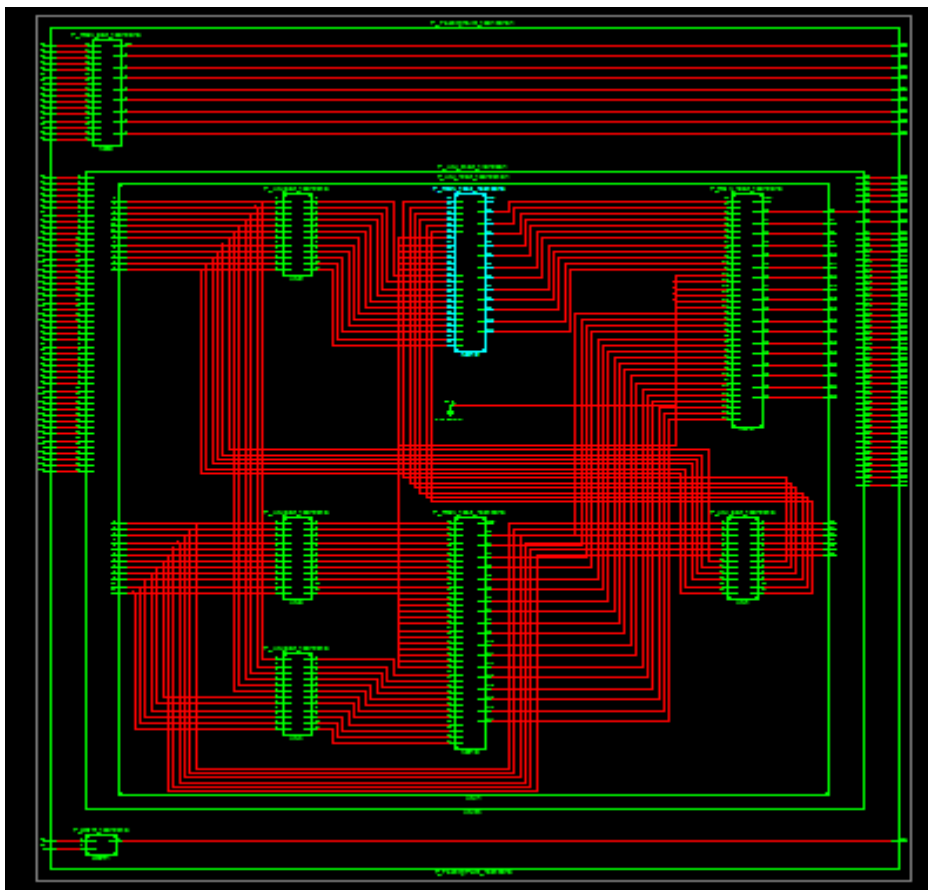


Fig.6.1 Snapshot of RTL schematic of floating point

Above diagram shows the register transistor logic diagram for 32 bit floating point multiplier.

Table.6.1 FT multiplier [Ref. 1] xc6s1x 100t-4fgg900

Floating point multiplier	No of Slices (63288)	CMD (ns)	No of IOBs (498)
Based on CSA	869	40.447	96
Based on Vedic multiplier	956	33.055	96

According to above result analysis table floating point multiplier designed by Vedic multiplication technique is better than CSA.

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Table 6.2 proposed result for fast floating point Multiplier (xc5vlx20t-2ff323).

Floating point multiplier	No of Slices (12480)		No of IOBs (172)		Propagation Delay
Proposed Cradle to cradle and Vedic technique	1263	10%	124	72%	23.342 ns

Above table shows the result for the fast Floating point multiplier which is key element of FFT processor. Further this type of fast multiplier can be used in DSP and image signal processing for reducing the noise from transmitted signal.

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