

Closed Loop Operation of Seven-Level PWM AC-AC Converter Fed to PMSM

Suresh Kakollu¹, Rambabu Saithana², Hanuman Dileep Batchu³, Lakshmi Prasanna Vemulapalli⁴

Assistant Professor, Department of EEE, Gudlavalleru Engineering College, Gudlavalleru, Andhra Pradesh, India¹

P.G. Student, Department of EEE, Gudlavalleru Engineering College, Gudlavalleru, Andhra Pradesh, India²

P.G. Student, Department of EEE, Gudlavalleru Engineering College, Gudlavalleru, Andhra Pradesh, India³

P.G. Student, Department of EEE, Gudlavalleru Engineering College, Gudlavalleru, Andhra Pradesh, India⁴

ABSTRACT: This paper proposes novel multilevel ac/dc/ac converters with reduced number of semiconductor devices to achieve light weight, efficiency, and better input current quality. The proposed three-phase front-end bidirectional seven-level (7L) rectifier and rear-end 7L inverter are constructed based on multiple-pole multilevel diode-clamped (M²DCC) approach, which consist a total number of 48 diode components clamped. Based on the M²DCC concept, the number of switching devices can be further reduced to construct a new unidirectional front-end rectifier (M²SCR). Comparative studies are conducted to analyze the performances of the two proposed front-end rectifiers with supportive mathematical derivations. Results obtained show that low current harmonic distortions of 5% and high power factor of 0.99 are achieved with small input inductors despite low-switching-frequency operation at 1 kHz. This seven level multiple pole ac/dc/ac converter is fed to permanent magnet synchronous motor (PMSM).

KEYWORDS: Seven-Level (7L) multiple-pole converter, reduce number of semiconductor devices, transformer less drive, permanent magnet synchronous motor (PMSM).

I. INTRODUCTION

Multilevel ac/dc/ac converters (which consist of frontend rectifier and rear-end inverter) for medium- to high power motor drives are widely employed in many industries. This configuration is favorable for many applications such as heat, ventilation, and air conditioning systems; pump/blower/traction drives; and even permanent-magnet synchronous generator wind turbine with grid connected. Due to the advantage of decoupling both front-end source and rear-end load through a dc link, simple control techniques can be implemented to achieve optimum performance.

The commonly used three-level (3L) ac/dc/ac drives can be configured based on a front-end unidirectional (such as Vienna rectifier) or a bidirectional (3L neutral-point-clamped rectifier) rectifier. Both of these 3L rectifier topologies require high switching frequency in order to mitigate the input current harmonic distortion. However, the output power efficiency is adversely affected. Besides that, the high insulation stress (large dv/dt and di/dt) produced is harmful for dynamic load applications [2].

Higher n-level (such as 5L and above) ac/dc/ac converter topologies offer an alternative solution to address the implications of high-switching-frequency operation. These higher n-level converters have the natural ability to achieve better efficiency with lower switching and conduction losses while operating at lower switching frequency [1], [3], [4]. Moreover, simple voltage balancing algorithms in [5]–[7] for 3L ac/dc/ac converters, as well as power factor correction techniques to achieve low input current distortion in [8]–[11], can be preserved for higher level pulse width modulation (PWM) converters as well.

Nevertheless, the realizing dc-link capacitor voltages are the greatest problem for higher n-level (with more than 3L output stepped voltage) diode-clamped converters. Thus, it results to poorer input and output performance. This unbalanced condition can be solved with the introduction of a multi winding transformer connected to multi pulse diode bridge rectifiers or an additional dc/dc balancing circuit in between front-end rectifier and rear-end inverter.

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Among the two solutions, an additional dc/dc voltage balancing circuit (see Fig. 1) proposed by Hatti *et al.* [12] would be more preferable than implementing a bulky and costly multi winding transformer.

Many classical configurations of high-power transformer less five-level (5L) ac/dc/ac drive have been experimented for the motor drive applications in [12]–[15] by the respective authors, but these would still require significant amount of active components. However, the future development of multilevel converters involves reducing the overall cost and size needed [1], [3]. The 5L ac/dc/ac drives based on the proposed multiple pole multilevel diode-clamped converter (M²DCC) approach presented in this paper (see Figs. 1 and 3) drastically reduce the number of power diodes required. Good overall performance is also achieved while operating at low switching frequency.

Two proposed combinations of 5L multiple-pole ac/dc/ac drives are the front-end bidirectional (5L-M²DCR, see Fig. 1) and unidirectional (5L M²SCR, see Fig. 3) rectifiers connected to the same rear-end (5L-M²DCI, see Fig. 1) inverter. To yield a fair analysis, the performances of both the proposed front-end rectifiers with the 5L-M²DCI are evaluated with the proposed power factor correction technique.

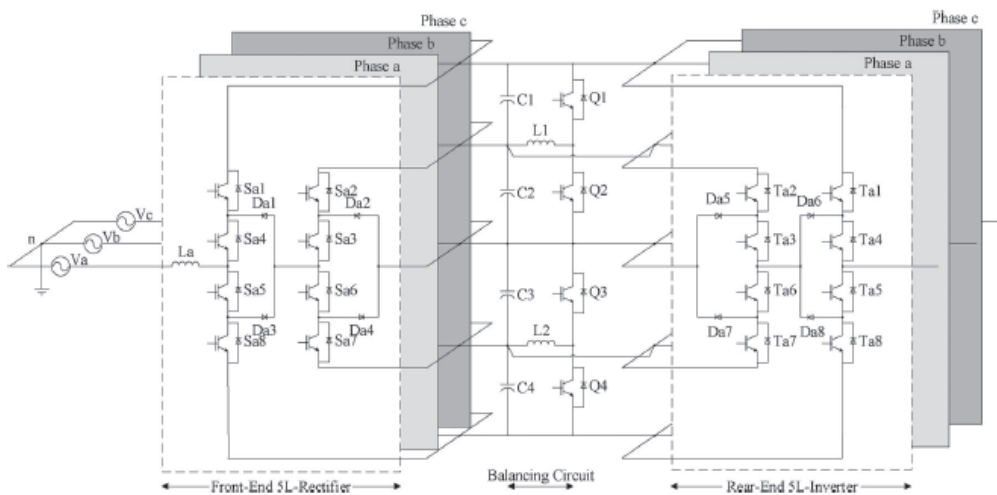


Fig. 1. Basic 5L bidirectional ac/dc/ac drive based on multiple-pole multilevel diode-clamped converter (5L-M²DCC) approach.

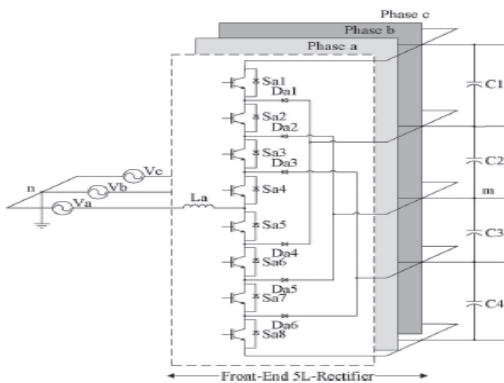


Fig. 2. Classical front-end 5L bidirectional rectifier (5L-MDCR).

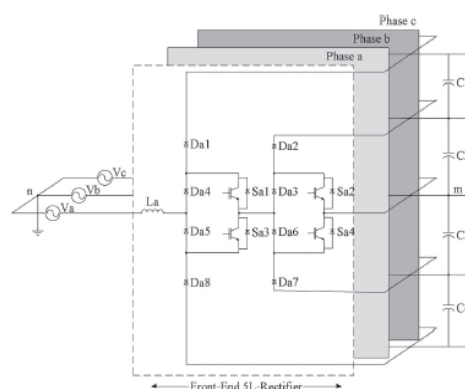


Fig. 3. Front-end 5L unidirectional rectifier (5L-M²SCR).

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II. RELATED WORK

The concept of Multi Level Inverters (MLI) do not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform with lower dv/dt and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and a more complicated controller for the inverter is needed.

However, the elementary concept of a multilevel inverter to achieve high power is to use a series of power semiconductor switches with several low voltage DC sources to perform power conversion by synthesizing a staircase voltage waveform. The switching algorithms of switches and commutation of them allow the addition of the capacitor voltages as temporary DC voltage sources, whereas the semiconductors should withstand limited voltages of capacitors.

III. OPERATING PRINCIPLES OF BASIC 5L AC/DC/AC TOPOLOGIES

This section presents the operating principles of three different 5L ac/dc/ac PWM converters based on the classical MDCC and the proposed M²DCC approaches. The derivation of the proposed M²DCR and M²SCR topologies are explained here, whereas the proposed M²DCI topology is detailed in [16].

A. Classical Bidirectional Front-End 5L-MDCR With Rear-End 5L-MDCI Topologies

The classical 5L-MDCC ac/dc/ac converter in [4], [12], and [13] is a back-to-back (BTB) configuration based on a frontend bidirectional rectifier (see Fig. 2) and a rear-end 5L diode-clamped inverter. A total of 16 insulated-gate bipolar transistors (IGBTs) and 12 diodes in each phase leg is required in this topology to synthesize the 5L input and output voltage waveforms (see Fig. 3 for the proposed front-end 5L unidirectional rectifier). The 5L voltage stepped waveform is obtained with the switching positions based on a single-pole circuit configuration, as shown in Fig. 4. It can be observed directly that the phase voltage levels are achieved across the point V_a to the neutral point m.

B. Basic Bidirectional Front-End 5L-M²DCR With Rear-End 5L-M²DCI Topologies

The basic 5L-M²DCC ac/dc/ac drive presented in Fig. 1 consists of a front-end bidirectional 5L-M²DCR and a rear-end 5L-M²DCI. This BTB topology requires only eight power diodes in each phase leg to achieve the same input and output quality as the classical 5L-MDCC. However, when the number of cells in this basic topology increases, a total number of 6(n-3) diode components are reduced. Hence, the 5L input and output voltage stepped waveforms are achieved with the proposed multiple-pole configuration according to the corresponding switching state listed in Table I.

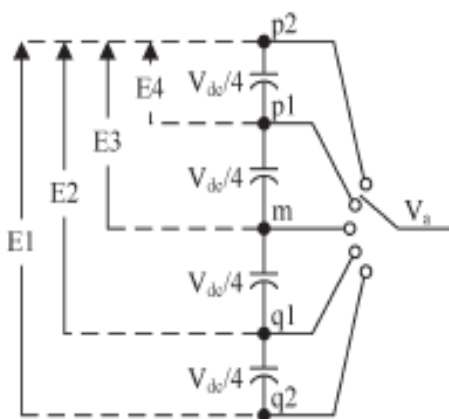


Fig. 4. Circuit diagram of per phase leg single-pole classical 5L-MDCC topology with switching position.

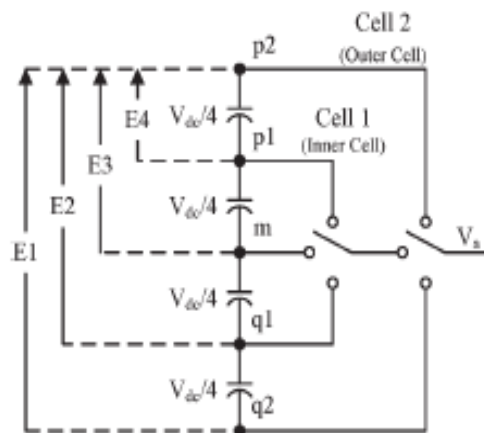


Fig. 5. Circuit diagram of per phase leg multiple-pole 5L-M²DCC topology with switching position.

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The 5L voltage stepped waveform of the M²DCC topology is achieved with the switching positions based on the multiple pole hierarchy, as shown in Fig. 5. The basic 5L-M²DCC topology is configured with two classical 3L-MDCC cells (Outer cell—Cell 2 and Inner cell—Cell 1) in each phase leg, which is constructed based on the multiple-pole concepts.

Table I
SWITCHING LOGIC FOR RESPECTIVE IGBT IN 5L-M²DCC TOPOLOGY

Vom Switch	Vdc/2 (Sector I)	Vdc/4 (Sector I & III)	0 (Sector I, III, IV & VI)	-Vdc/4 (Sector IV & VI)	-Vdc/2 (Sector V)
Sa1, Ta1	1	0	0	0	0
Sa2, Ta2	1	1	0	0	0
Sa3, Ta3	1	1	1	0	0
Sa4, Ta4	1	1	1	1	0
Sa5, Ta5	0	1	1	1	1
Sa6, Ta6	0	0	1	1	1
Sa7, Ta7	0	0	0	1	1
Sa8, Ta8	0	0	0	0	1

The switching logic followed for the 5L-M²SCR is as shown in the table-I. From the above table each switch is in on position in order to get a sector voltage defined in the table with low transition losses. The above table shows 0 and 1 which indicates switch is in off position and switch is in on position

C. Basic Unidirectional Front-End 5L-M²SCR With Rear-End 5L-M²DCI Topology

A bidirectional power flow in the front-end rectifier is not required for certain ac/dc/ac drive applications such as propulsion, compressor, or any non regenerative braking system. Thus, a proposed transformer less front-end unidirectional rectifier is reconstructed in Fig. 3 with the arrangement of the semiconductor devices in the bidirectional M²DCR configuration (see Fig. 1). Hence, the unidirectional 5L rectifier in Fig. 3 is named as multiple-pole multilevel switch-clamped rectifier (M²SCR) instead. Each phase leg of the proposed unidirectional 5L-M²SCR also requires two cells, as shown in Fig. 5, to achieve 5L input voltage stepped waveform. The states selection of the top and bottom diodes of a M²SCR is dependent on 1-Sa1 and 1-Sa2 for the outer cell and similarly for the inner cell. Hence, only two switching devices are required in each cell, with four series diodes connected to the terminals of the capacitors in the dc link.

D. General Characteristic of the Classical and Proposed 5L AC/DC/AC Converters

The front-end rectifier and the rear-end inverter of 5L ac/dc/ac drives are operated independently with same level-shifted PWM (LS-PWM). The LS-PWM requires a reference signal and a set of four 1-kHz triangular carriers to achieve the desired switching signals for the respective semiconductor switches. The switching function of the LS-PWM technique for the 5L rectifiers and inverters is expressed as

$$\begin{aligned}
 S_{a1}(t) &= T_{a1}(t) = 2m_a \sin \omega t - 1 \\
 S_{a2}(t) &= T_{a2}(t) = 2m_a \sin \omega t \\
 S_{a3}(t) &= T_{a3}(t) = 2m_a \sin \omega t + 1 \\
 S_{a4}(t) &= T_{a4}(t) = 2m_a \sin \omega t + 2
 \end{aligned} \tag{1}$$

where m_a is the ratio of two times the fundamental component of pole voltage to the dc-link voltage. Under the condition of steady state and balanced dc-link voltage, the general incremental output pole voltage equation is expressed as

$$V_{xm}(t) = \frac{V_{dc}(t)}{n-1} \left(\sum_{i=1}^{n-1} T_{xi} - \frac{n-1}{2} \right) \tag{2}$$

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Where, 'x' represents phase "a", "b" and "c;" and n is the number of voltage level. T_{xi} is the switching states of each switching device depicted in the inverter side. The voltage transfer ratios of the converters system between the dc bus voltage to the input and output voltage are defined as follows:

$$M_{x,rectifier}(t) = \frac{V_{dc}(t)}{V_{xL-L}(t)}, \quad M_{x,rectifier}(t) > 1 \quad (3)$$

$$M_{x,inverter}(t) = \frac{2V_{xm}(t)}{V_{dc}(t)}, \quad M_{x,inverter}(t) \leq 1 \quad (4)$$

Where $V_{xL-L}(t)$ is the line-to-line grid voltage, and $V_{xm}(t)$ is the output pole voltage referred to the inverter side. In general, high modulation index ($M_{x,rectifier}(t) > 1$) of the front-end rectifier is required to mitigate the input current distortion and achieve good voltage tracking due to its boosting effect in nature. Meanwhile, the rear-end inverter must be operated at the linear region ($M_{x,inverter}(t) \leq 1$) to prevent any high-order harmonic components incurred in the load. Thus, low switching frequency can be used for a 5L rectifier to achieve better power conversion efficiency and the ripple current is expressed in the following equation based on the previous ones, namely, equations (2),(3) and (4)

$$\Delta I_{Lx}(t) \approx \frac{k}{L_x f_s} \left\{ \frac{3V_{xL-L}(t) - 3\sqrt{3}V_{mn}(t)}{3\sqrt{3}} - \frac{M_{x,rectifier}(t)V_{xL-L}(t)}{n-1} \left(\sum_{i=1}^{n-1} S_{xi,d} - \frac{n-1}{2} \right) \right\} \quad (5)$$

k is the duty ratio of switching transition (see Fig 6), and this is expressed as

$$\begin{cases} 0 \leq [k = 2 \sin \omega t] \leq 1, & 0 \leq \omega t \leq \frac{\pi}{6} \\ 0 \leq [k = 2 (\sin \omega t - 1/2)] \leq 1, & \frac{\pi}{6} \leq \omega t \leq \frac{\pi}{2} \end{cases} \quad (6)$$

The critical input inductance value for front-end 5L-M²DCR can be estimated with the duty cycle and the switching states with respect to the sectors shown in figure 4.6. According to equation (5), the maximum peak value of the input ripple current is determined at $\omega t = 30^\circ$. Thus, the critical inductance value is estimated as follows

$$L_{x,max} \approx \frac{4(0.5V_{xn} - V_{mn}) - V_{dc}}{4\Delta I_{Lx} f_s} \quad (7)$$

Where, V_{xn} is the peak value of the grid phase voltage. The minimum capacitance value in the dc link can be estimated in equation (8) with the change of ampere-second ($\Delta A_{cap}sec$) and the switching state T_{a1} of the rear-end side. The expression of $\Delta A_{cap}sec$ is obtained by subtracting the peak value of the grid phase current with the average input current of the converter. Assume that all the dc-link capacitors are equal to C. Then

$$C \approx \frac{4\Delta A_{cap}sec}{\Delta V_{cap}} = \frac{4T_{a1}(I_a - I_{inv}(avg))}{\epsilon V_{dc} F_s} \quad (8)$$

where ϵ is the percentage value of the permissible ripple voltage content, and $I_{inv}(avg)$ is the average input current value of the rear-end 5L inverter.

IV. HIGH-POWER-FACTOR OPERATION OF THREE-PHASE 5L M²DCR AND M²SCR RECTIFIERS

A. Semiconductors Voltage and Current Stresses

Voltage and current stresses are the dominant factors considered in the converter design, so that the converter can achieve optimum performance with higher reliability. Proper selection of device rating for the proposed front-end rectifiers is determined based on the global stress analysis. The voltage and current stress expressions for the respective front-end rectifiers are derived with the switching function in equations (1) and based on the following factors: 1) high-power-factor operation; 2) current and voltage ripple free; 3) constant switching frequency; 4) balanced dc-link capacitors voltage; and 5) zero voltage dropped across boost inductors (L_x).

The maximum voltages across the power devices of unidirectional 5L-M²SCR and bidirectional 5L-M²DCR are respectively expressed in the following:

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$$\left\{ \begin{array}{l} V_{Da1} = \frac{3V_{dc}}{4} \\ V_{Da4} = V_{Sa1} = \frac{3V_{dc}}{8} \\ V_{Da2} = V_{Da3} = V_{Sa2} = \frac{V_{dc}}{4} \\ V_{Sa1} = \frac{3V_{dc}}{4} \\ V_{Sa4} = \frac{V_{dc}}{2} \\ V_{Sa2} = V_{Sa3} = V_{Da1} = V_{Da2} = \frac{V_{dc}}{4} \end{array} \right. \quad (9)$$

$$\left\{ \begin{array}{l} V_{Sa1} = \frac{3V_{dc}}{4} \\ V_{Sa4} = \frac{V_{dc}}{2} \\ V_{Sa2} = V_{Sa3} = V_{Da1} = V_{Da2} = \frac{V_{dc}}{4} \end{array} \right. \quad (10)$$

Since the maximum voltage stress expressions (9) and (10) are for the power devices in the upper phase leg, the respective complimentary power devices in the lower phase leg are also determined using the same expressions.

The average current stress is analyzed over one period of the fundamental frequency based on the assumed five factors (1)–(5). For simplification, the average current stress is approximated as follows based on respective switching functions in equations (1).

$$\begin{aligned} I_{Sa(\text{Outer Cell})}(t) &= I_{Da(\text{Outer Cell})}(t) \\ &= \frac{1}{2\pi} \int_0^{2\pi} I_a \sin(\omega t) S_{a(\text{Outer Cell})} d\omega t \\ I_{Sa(\text{Inner Cell})}(t) &= I_{Da(\text{Inner Cell})}(t) \\ &= \frac{1}{2\pi} \int_0^{2\pi} I_a \sin(\omega t) * \left[2 - \frac{4V_{am(1)}}{V_{dc}} \sin \omega t \right] S_{a(\text{Inner Cell})} d\omega t \end{aligned} \quad (11)$$

It is proved that, during the negative cycle of the conduction period, the reverse current through the semiconductor switches in the bidirectional 5L-M²DCR will be cancelled out from the current stress during the positive cycle period. Unlike the case for the unidirectional 5L-M²SCR, the current only flows through the diodes during the positive cycle conduction period. Hence, the final net average current stress of the 5L-M²DCR is found much lower compared with that of the 5L-M²SCR.

B. Unbalanced DC-Link Capacitor Voltages

The unbalanced dc-link capacitor voltages may disrupt the smooth operating system and affect the global reliability if the power converter is not adequately designed. This disastrous condition will damage the converter by overstressing the limited blocking voltage capability of the semiconductor devices. Although this undesirable condition can be typically resolved by disabling the rectifier/inverter operation when any fault condition occurs, the overall efficiency of the system may be greatly affected. The alternative solution to overcome this issue is to ensure that the power device ratings are properly selected during the design according to the worst case scenarios. The maximum voltage stress across the semiconductor switches in the proposed 5L rectifiers under unbalanced condition is V_{dc} , unlike in the classical 5L rectifiers, which will be experiencing $2V_{dc}$ (twice the dc-link voltage). As a result, it is essential to have series-connected switches for the classical 5L rectifiers, but these additional switching devices can be avoided for the proposed 5L topologies.

C. SRF Current Control Scheme

The Basic control algorithm with power factor correction technique is shown in figure 6. Two control loops, i.e., synchronous-reference-frame (SRF) current control and constant switching frequency modulation, are implemented to regulate the dc-link voltage and mitigate the current distortions. Due to the simplicity of the control strategy, low-cost integrated control circuit can be designed. The balancing control for the dc–dc balancing circuit is presented in [5] and [6].

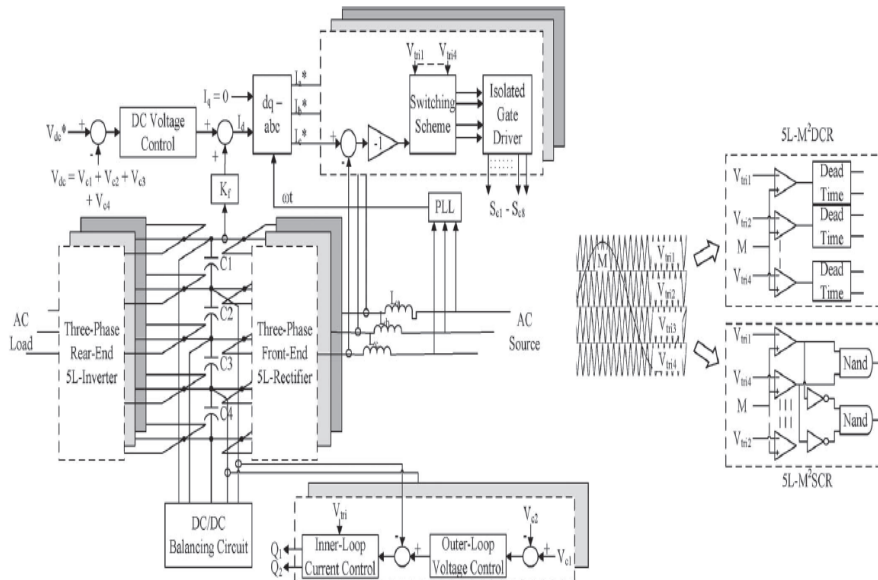


Fig. 6. Basic front-end rectifier controller for the 5L ac/dc/ac converter

The unity power factor controller for the front-end 5L rectifiers (M^2DCR or M^2SCR) designed in figure 6 is based on the SRF current control with the LS-PWM technique. The detailed analyses of the outer-loop dc-link voltage control and the inner-loop current control are both presented in [23]. SRF controller provides a good dynamic response to achieve high quality input sinusoidal current with constant unity power factor performance.

The open-loop transfer function of the dc-link voltage control under steady-state condition is written as follows to achieve a stable control system:

$$L(S) = \frac{K_p S + K_I}{s} \cdot \frac{L_x I_d}{C_{eq} V_{dc}} \cdot \frac{\left(\frac{\sqrt{3} V_p}{L_x I_d}\right) - S}{S + \left(\frac{I_{dc}}{C_{eq} V_{dc}}\right)} \quad (12)$$

I_d is the peak value of the reference current, which is obtained from the summation of I_{dc} (output of dc voltage control) and feed forward current (output of K_f). The feed forward current control loop under steady-state condition is derived based on the power balanced principle, which is expressed in the following

$$K_f = \frac{V_{dc}}{\sqrt{3} V_p} \quad (13)$$

V. PROPOSED SEVEN LEVEL MULTIPLE POLE PWM AC-AC CONVERTER FED TO PMSM

A. Permanent Magnet Synchronous Machine

The permanent-magnet synchronous machine (PMSM) drive has emerged as a top competitor for a full range of motion control applications. For example, the PMSM is widely used in machine tools, robotics, actuators, and is being considered in high-power applications such as vehicular propulsion and industrial drives. It is also becoming viable for commercial/residential applications. The PMSM is known for having high efficiency, low torque ripple, superior dynamic performance, and high power density. These drives often are the best choice for high-performance applications and are expected to see expanded use as manufacturing costs decrease.

The PMSM is sometimes referred to as a permanent-magnet AC (PMAC) machine or simply as a PM machine. In some instances it is referred to as a brushless DC (BDC) machine because by appropriate control it can be made to have input/output characteristics much like a separately excited brush-type DC machine.

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The use of permanent magnets in the rotor facilitates efficiency, eliminates the need for slip rings, and eliminates the electrical rotor dynamics that complicate control (particularly vector control). The permanent magnets have the drawback of adding significant capital cost to the drive, although the long term cost can be less through improved efficiency. The PMSM also has the drawback of requiring rotor position feedback by either direct means or by a suitable estimation system.

A permanent magnet synchronous motor (PMSM) is a motor that uses permanent magnets to produce the air gap magnetic field rather than using electromagnets. These motors have significant advantages, attracting the interest of researchers and industry for use in many applications.

Basically, a PMSM machine can be looked at as a transformer with a moving secondary, where the coupling coefficients between the stator and rotor phases change continuously with the change of the rotor position. As presented above, the machine model can be described by differential equations with time-varying inductances which are functions of the rotor position. However, such a model tends to be very complex because of the time varying inductance coefficients and associated inductance matrix.

In the 1920s, R. H. Park presented a new theory for such ac electric machine analysis to eliminate the difficulty with the time-varying parameters/inductances, which is usually called the d-q Park's transformation, or the two-reaction theory. Through this method, the variables in the three-phase stationary reference frame will be transformed to constants in the synchronously rotating reference frame, which is also called d-q reference frame. The voltage transformation can be written as follows:

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos(\frac{2\pi}{3} - \theta) & \cos(\frac{2\pi}{3} + \theta) \\ \sin \theta & \sin(\frac{2\pi}{3} - \theta) & \sin(\frac{2\pi}{3} + \theta) \\ 0.5 & 0.5 & 0.5 \end{bmatrix} \quad (14)$$

$$V_d = R_s i_d + \frac{d\lambda_d}{dt} - \omega_e \lambda_q \quad (15)$$

$$V_q = R_s i_q + \frac{d\lambda_q}{dt} + \omega_e \lambda_d \quad (16)$$

$$\lambda_d = L_d i_d + \lambda_{pm} \quad (17)$$

$$\lambda_q = L_q i_q \quad (18)$$

Where, L_d is the d-axis inductance, L_q is the q-axis inductance, and λ_{pm} is the amplitude of flux linkage due to the permanent magnet. According to a dynamic equivalent circuit of a PMSM in the d-q frame can be drawn as shown in figure 7.

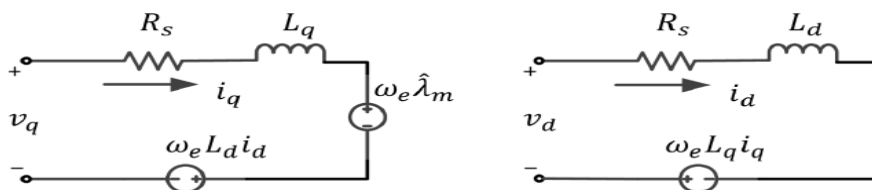


Fig. 7. Equivalent circuit of a PMSM.

In the d-q frame, the input power of a PMSM can be written as:

$$P_{in} = \frac{3}{2} (V_d i_d + V_q i_q) \quad (19)$$

Assuming the motor losses are negligible, then the input power equals the output power, P_{out} of the motor, which can be represented as follows

$$P_{out} = \frac{3}{2} \omega_e (\lambda_{pm} i_q + (L_d - L_q) i_d i_q) \quad (20)$$

Since the output power is a product of the motor mechanical speed time the developed/output torque, the output torque can be obtained as:

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$$T_e = \frac{P_{out}}{\omega_m} = \frac{p}{2} \frac{3}{2} (\lambda_{pm} i_q + (L_d - L_q) i_d i_q) \quad (21)$$

B. Seven Level Multiple Pole PWM AC-AC Converter

In this paper the work is extended to seven level multiple pole PWM AC-AC converter. For obtaining seven levels output at the inverter side two more switches and two more diodes are added in each pole for every phase at both rectifier side and inverter side of five level multiple pole PWM AC-AC converter.

The controlling circuit for five level multiple pole PWM AC-AC converter is extended to control triggering pulses for seven level multiple pole PWM AC-AC converter.

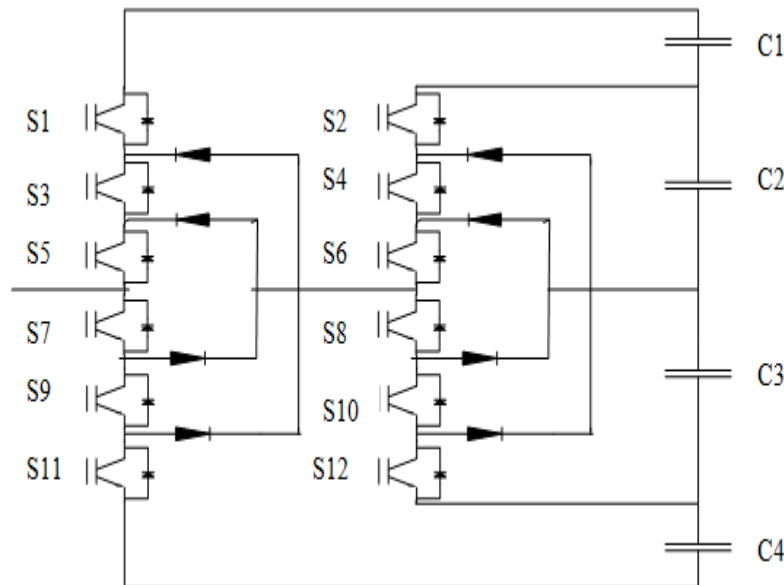


Fig. 8. Seven Level Multiple Pole Diode Clamped Inverter

In seven level multiple pole diode clamped converter 12 IGBT switches and 8 clamping diodes are used. In overall 72 IGBT switches and 48 clamping diodes utilised. But in classical method 60 clamping diodes are required. So 12 diodes are saved.

C. Control Theory

The front-end rectifier and the rear-end inverter of seven level of 7L ac/dc/ac converter are operated independently with same Level- shifted PWM (LS-PWM). The LS-PWM requires a reference signal and a set of six 1-kHz triangular carriers to achieve desired switching signals for the respective semiconductor switches.

Under the condition of steady state and balanced dc-link voltage, the general incremental output pole voltage equation is expressed as

$$V_{xm}(t) = \frac{V_{dc}(t)}{n-1} \left(\sum_{i=1}^{n-1} T_{xi} - \frac{n-1}{2} \right) \quad (22)$$

Where, ‘x’ represents phase “a,” “b,” and “c;” and n is the number of voltage level. T_{xi} is the switching states of each switching device depicted in the inverter side. High modulation index ($M_{x,rectifier}(t) > 1$) of the front-end rectifier is required to mitigate the input current distortion and achieve good voltage tracking due to its boosting effect in nature.

Meanwhile, the rear-end inverter must be operated at the linear region ($M_{x,inverter}(t) \leq 1$) to prevent any high-order harmonic components incurred in the load There are two control loops in this to regulate the dc-link voltage

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and mitigate the current distortions. They are synchronous reference frame (SRF) current control and constant switching frequency modulation.

The PI controller which is used as DC voltage control is to estimate peak value of reference current and to regulate the dc-link capacitor voltage. SRF controller provides a good dynamic response to achieve high quality input sinusoidal current with constant unity power factor performance.

VI. SIMULATION RESULTS

The operation of the proposed bidirectional 7L-M²DCR has been evaluated with the power factor control under various load conditions. Figs. 9 and 10 show the unity power factor operation under two different types of loading effect. However, the proposed unidirectional 7L-M²SCR topology can only achieve unity power factor without any reversal power capability with same performance obtained in Fig. 9.

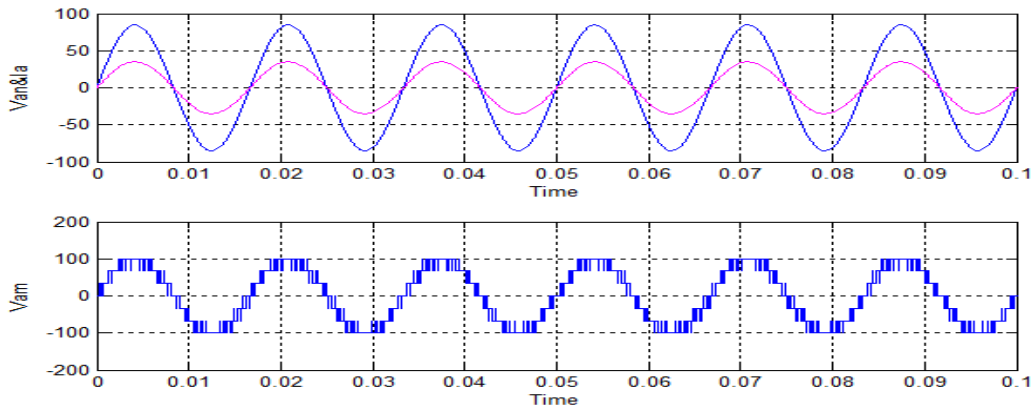


Fig. 9. Simulation result for rectifying mode

The reversal power capability with the current shaping in Fig. 10 is achieved by connecting a dc source (i.e., fuel cell and solar) across the dc link, in order to validate the bidirectional power flow of the proposed 7L-M²DCR. Since the power factor of the 7L-M²DCR topology can be controlled to achieve leading/lagging performance, as shown in Figs. 11 and 12, hence it is known as a four-quadrant multilevel rectifier. With such inherent performances, it is concluded that the 7L-M²DCR can be applicable for reactive power compensator applications with power factor control capability, The speed and torque wave forms of PMSM are shown in Figs.13,14,15 and 16.

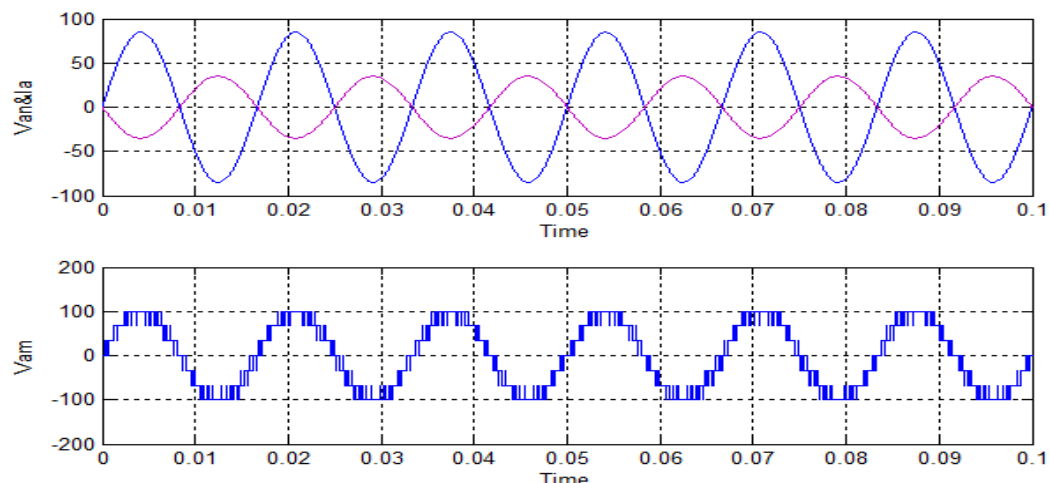


Fig. 10. Simulation result for inverting mode

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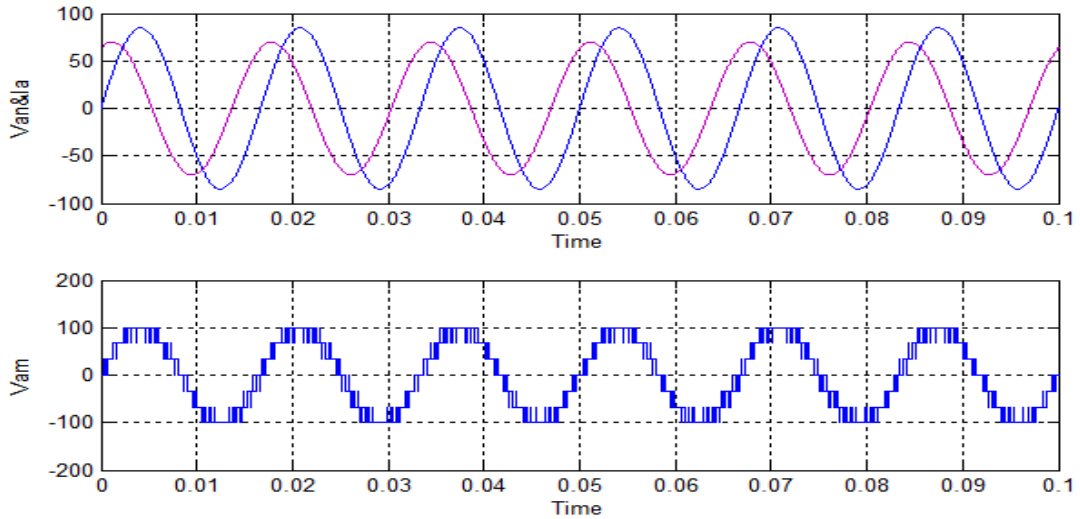


Fig. 11. Simulation result for capacitive load

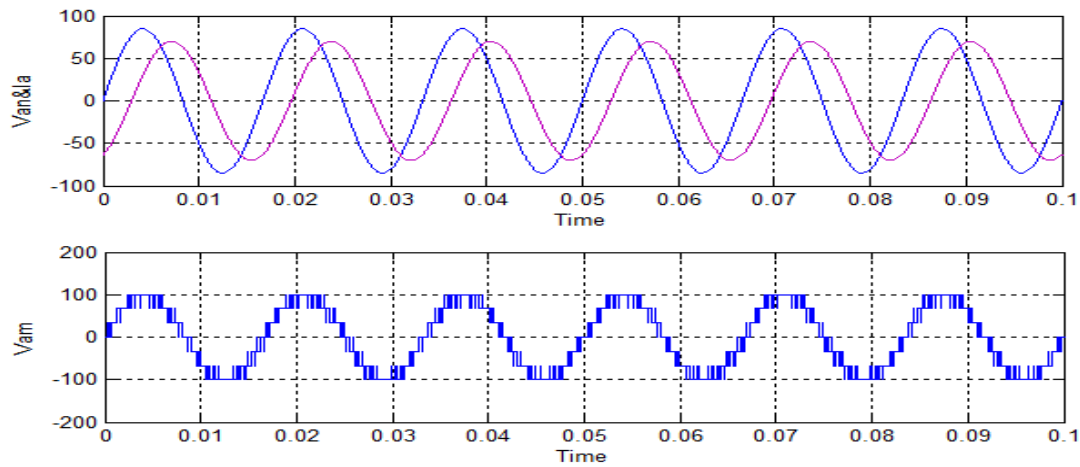


Fig. 12. Simulation result for inductive load

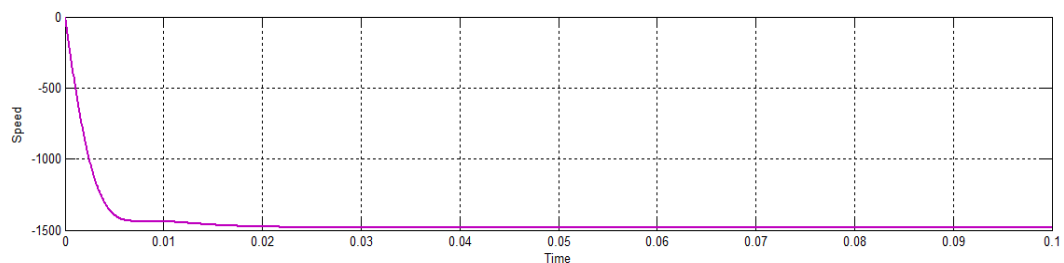


Fig. 13. Speed waveform of PMSM for rectifying mode

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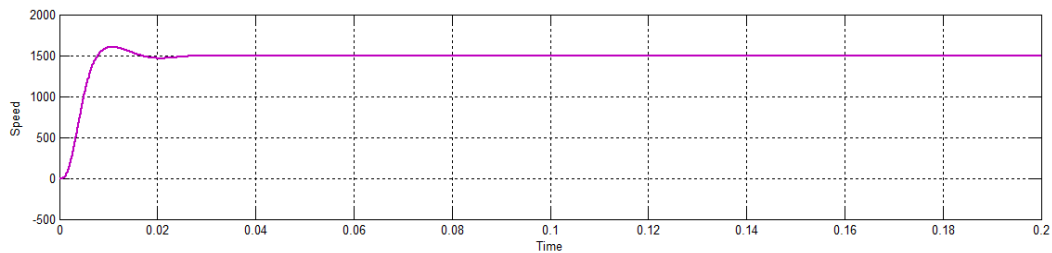


Fig. 14. Speed waveform of PMSM for inverting mode

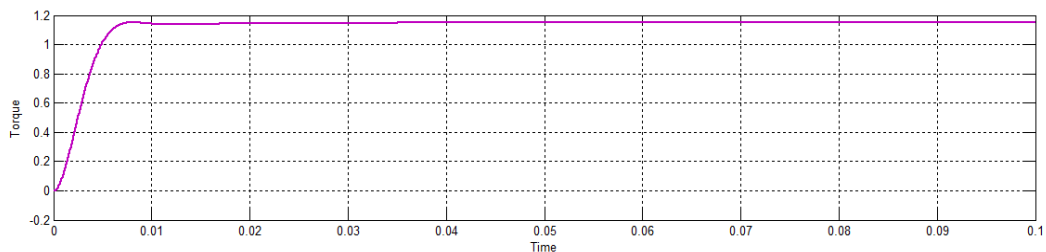


Fig. 15. Torque waveform of PMSM for rectifying mode

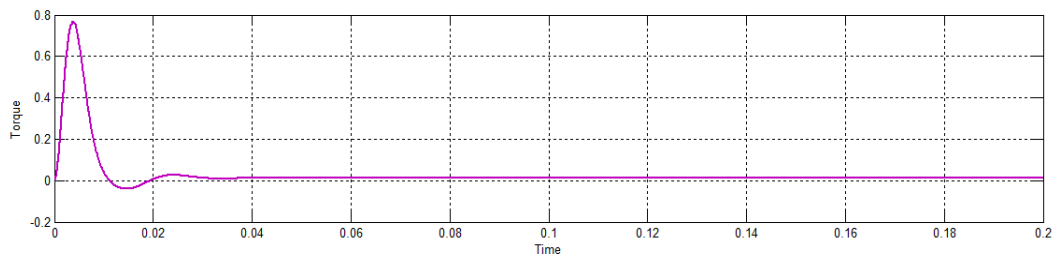


Fig. 16. Torque waveform of PMSM for inverting mode

VII. CONCLUSION

A new generation of front-end bidirectional 7L-M²DCR topologies has been introduced in this paper to reduce the number of semiconductor devices compared with the conventional converters. Excellent performance and low input current distortion with high power factor is achieved with low operational switching frequency of 1 kHz without the aid of any bulky LC passive filter. In addition to that, the reduction of component counts allows the proposed converters to achieve low voltage/current stress and low switching losses. This is at the small cost of having an additional voltage balancing circuitry in the dc link to balance the capacitor voltages. Thus, alternative dc-link balancing strategies such as modulation schemes or control algorithms can be implemented to replace the additional balancing circuit. These will provide a more cost-effective and energy-efficient solution for a higher level ac/dc/ac drive and can particularly be suitable for renewable energy conversion where high efficiency is paramount.

Permanent Magnet Synchronous Motor is connected at output side of inverter in seven level multiple pole PWM AC-AC diode clamped converter. The speed and torque variations are observed. PMSM rotates with synchronous speed in both inverting and rectifying modes. But the PMSM acts as motor in inverting mode and acts as generator in rectifying mode.

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